The dual-core P5020 and single-core P5010 processors are Freescale’s first offerings with a 64-bit core, the e5500. With frequencies scaling to 2.2 GHz, large caches and high per-cycle efficiency, these products target applications that require high single-threaded performance.

The P5 platform leverages architectural features pioneered in the P4 platform, including the three-level cache hierarchy for low latencies, hardware hypervisor for robust virtualization support, data path acceleration architecture (DPAA) for offloading packet handling tasks from the core and the CoreNet switch fabric which eliminates internal bottlenecks. This enables architectural compatibility from the P5 platform to the P4 platform and also to the P3 platform, which uses the same architecture.

As a highly integrated device with integrated memory controllers—XAUI, SGMII, PCI Express® and Serial RapidIO® interconnects—the P5 platform fills a need in the embedded market for single-chip solutions with high single-threaded performance that fit within a 30W power budget.

The P5 processors use the same 1295-pin package as the P4 and P3 processors and all the products in these three families are pin compatible. The P5020 processor can run in either 64-bit or 32-bit mode, providing support for legacy software while easing the migration to 64-bit processing. Between the architectural similarity and pin compatibility, developers can leverage the same software and printed circuit board (PCB) across many applications with a variety of process requirements, ranging from a low-power mid-range mixed control- and data-plane (P3 platform), to high-performance data path performance (P4 platform) to high-performance control plane (P5 platform).

**Key Features**

- e5500 core: Targeted at 2 GHz and capable of scaling up to 2.2 GHz, this 64-bit core enables flat addressing of up to 64 GB, simplifying management of large data sets such as routing tables, statistics and storage data. The IEEE Std. 754™ FPU double precision floating point unit supports 2x to 4x the performance of its predecessor, the e500mc. The improved core architecture yields 3.0 DMIPS/MHz, a 20 percent efficiency gain over the e500mc.
- Three-level cache hierarchy: The low-latency 32 KB L1 instruction and data cache is augmented by a low-latency 512 KB private backside L2 cache per core. The L2 is 8-way set associative and ECC protected. A shared 2 MB CoreNet platform cache (L3) facilitates core-to-core communications and minimizes accesses to main memory.
- Hypervisor: The e5500 supports a hardware hypervisor designed to enable each core to run its own operating system completely independent of the other core. The hypervisor facilitates resource sharing and partitioning in a dual-core environment, and provides protection in the event that one core, driven by malicious or improperly programmed code, tries to access an area it does not have permission to read or write. It also allows the sharing and partitioning of various I/Os across both cores and ensures that incoming memory mapped transitions are written only into appropriate ranges of the memory map.
- DPAA: This offloads the cores from the need to perform common packet-handling tasks. For instance, the DPAA will extract headers from incoming packets, police them, classify them and manage their data buffers. The work is assigned to cores with a three-level scheduling hierarchy, which can also facilitate sharing of packet workload over both cores.
- Application-specific acceleration: The RAID5/6 block calculates parity for network attached storage and direct attached storage applications. The security block runs common crypto algorithms used in wireless and networking applications. The pattern-matching engine searches for text strings in packets for anti-virus/anti-spam applications. The RapidIO Message Manager implements efficient Type 9 and 11 messaging.

**Target Applications**

- Control plane: With similar requirements in both networking and wireless infrastructure, control plane applications best fit on processors that derive their performance from a fewer number of higher performance cores, as this minimizes the need to rework legacy code.
- Storage: The P5020 and P5010 offer a RAID 5/6 accelerator for use in storage area networks (SAN) and network attached storage (NAS). The RAID 5/6 accelerator performs the parity calculation using a configurable Galois field (GF) polynomial and supports a data integrity field (DIF), making it ideal for use in high-performance, high-reliability storage applications.
- Aerospace, defense, industrial: Complex calculations characterize all three of these applications. The high-performance floating point unit combined with 64-bit data transfers results in a high computational capacity that still remains within a tight thermal budget. Dual Serial RapidIO ports support redundant backplanes.
**Features**

Dual 64-bit e5500 cores, built on Power Architecture® technology

- Initially offered at 2 GHz and scalable to 2.2 GHz
- Each with 512 KB backside L2 cache
- Supports up to 64 GB addressability (36 bit physical addressing)

**Memory controller**

- Dual DDR3, 3L up to 1.3 GHz
- 32/64-bit data bus w/ECC

**High-speed interconnects**

- 4 x PCI Express 2.0 controllers
- 2 x Serial RapidIO 1.3/2.1 controllers
- 2 x SATA 2.0 at 3 Gbps
- 2 x USB 2.0 with PHY

**CoreNet switch fabric**

- Dual 1 MB shared CoreNet platform cache (L3) w/ECC

**Ethernet**

- 5 x 10/100/1000 Ethernet controllers or 4x 2.5 Gbps SGMII
- 1 x 10 Gigabit Ethernet controllers
- All with classification, hardware queuing, policing, buffer management, checksum offload, QoS, lossless flow control
- IEEE® 1588
- Up to 1 x XAUI, 4 x SGMII or 2.5 Gbps SGMII, 2 x RGMII

**Data path acceleration**

- SEC 4.2: public key accelerator, DES, AES, message digest accelerator, random number generator, ARC4, SNOW 3G F8 and F9, CRC, Kasumi
- PME 2.1: searches for 128 byte text strings in 32 KB patterns in 128 million sessions
- RapidIO messaging: Type 9 and 11
- RAID5/6 engine

**Device**

- 45 nm SOI process technology
- 1295-pin FCPBGA package, 37.5 mm x 37.5 mm

**Enablement**

- Enea®: Real-time operating system support
- Green Hills®: Complete portfolio of software and hardware development tools, trace tools and real-time operating systems
- Mentor Graphics®: Commercial grade Linux® solution
- CodeSourcery: Tool chain support for new core technology
- WindRiver®: Simics® model of core technology to enable early 64-bit development
- Power.org™: Supports the Power Architecture core technology using the new ISA v2.06
- Development System: Four PCI Express slots, one Serial RapidIO slot, one XAUI slot, one SGMII slot, SATA disk, Aurora debug port

**Learn More:**

For current information about Freescale products and documentation, please visit freescale.com/QorIQ.