Datasheet

BL54L15µ Series

Version 0.4

Revision History

Version	Date	Notes	Contributor(s)	Approver
0.1	02 Oct 2024	Preliminary release.	Raj Khatri	Jonathan Kaye
0.2	18 Oct 2024	Updated table4 external antenna list to Added antenna Ezurio iFlexPIFA Mini EFG2401A3S-10MH4L to External Antenna Integration with BL54L15µ RF trace pin variant (453-00224) Change Mag Layers EDA-8709-2G4C1-B27-CY antenna gain from 2dBi to 2.32dBi.	Raj Khatri	Jonathan Kaye
0.3	5 Nov 2024	Updated height of module to 1.75 mm.	Dave Drogowski	Jonathan Kaye
0.4	20 Nov 2024	Updated power supply voltage to 1.7 – 3.6 V.	Dave Drogowski	Jonathan Kaye

Contents

1 Overview and Key Features

Experience a new pinnacle of performance, efficiency, and security with our new BL54L15µ series, built on Nordic Semiconductor's powerful **nRF54** silicon. Elevating what you know and love from the nRF52 series, this next generation redefines Bluetooth LE and 802.15.4 solutions. Unleashing enhanced processing power, expanded memory, and innovative peripherals, the BL54L15µ is the ultimate choice for low power connectivity, in the smallest footprint.

Powered by **Nordic's nRF54L15** (WLCSP 300um) SoC, our ultra compact BL54L15µ modules deliver secure and robust Bluetooth LE and 802.15.4 with flexible programming via the Nordic SDK, Zephyr RTOS and Canvas Software Suite.

Featuring a **128MHz ARM Cortex M33** and **128MHz RISC-V coprocessor**, supported by 1.5 MB non-volatile memory and 256 KB RAM, the BL54L15µ modules offer double the processing power (vs prior BL654 – nRF52840). The BL54L15µ series brings out all nRF54L15 hardware features and capabilities including up to **+8 dBm** transmit power, **1.7V – 3.6V** supply considerations, and **NFC A-Tag** implementation.

It's further enhanced with state-of-the-art security and is designed for PSA Certified level 3. It supports services such as Secure Boot, Secure Firmware Update, Secure Storage plus protection from physical attacks.

Note: BL54L15µ hardware provides all functionality of the nRF54L15 chipset used in the module design. This is a hardware datasheet only – it does not cover the software aspects of the BL54L15µ. This is to acknowledge that information in this datasheet is referenced from the nRF54L15 datasheet.

1.1 Features and Benefits

- **Nordic nRF54L15** – 2.4 x 2.25mm WSCLP with 32 GPIOs utilized.
- **Multi-protocol support:** Bluetooth 5.4 LE, 802.15.4 (Thread/Matter)
- **Cortex M33** processor core: 128 MHz ARM Cortex M33
- **RISC-V** co-processor core: 128 MHz VPR
- **Memory:** 1.5MB non-volatile memory, 256 KB RAM
- **High Speed Peripherals**: - HS-SPI/UART, software defined peripherals on 128 MHz VPR, GPIO - 1x 64 MHz Port, 1.7 – 2.6V, 11 GPIOs
- **Low Leakage Peripherals:** 2x QDEC, 7x Timer, Global RTC, 2x WDT, NFC A-Tag, TEMP, I2S, COMP, 3x PWM, LPCOMP, 14-bit 8CH ADC, 5x TWI/SPI/UART, GPIO (2x 16 MHz Port (P0, P1), 20 GPIO's, 1.7-2.6V, 32 GPIO)
- **Antenna choice** – integrated pre-certified **Chip antenna** or external antenna support via **Trace Pad**
- **Ultra-small footprint** (6.3 mm x 7.9 mm x 1.75 mm)
- **Extended** Industrial **Temperature Rating** (-40° to +105 °C)
- **Development choice:** Zephyr RTOS, Nordic nRF Connect SDK & Canvas
- **Bluetooth LE**: Peripheral/Central, 2 Mbps (high throughput), LE Coded (long range), AoA/AoD, Mesh
- Firmware Over the Air **(FOTA)** via MCUboot and Zephyr
- **Hostless operation** – Multi Core MCU reduces BOM
- **Fully featured development kits** to jump start Bluetooth LE development
- Mechanically same form factor as **BL652 Series**

1.2 Application Areas

- Building Automation
- Security
- Medical Peripherals
- Industrial Sensors

2 Specification

2.1 Specification Summary

Categories/Feature	Implementation
Wireless Specification	
Bluetooth®	Bluetooth 5.4 – Single mode • GATT client/server – Any adopted/custom services • Central/Peripheral roles • Bluetooth LE mesh • 2M PHY • LE Coded PHY • LE Advertising Extensions • LE secure connections • Data packet length extensions • LE privacy v1.2 • LE ping • DTM Firmware (Test Modes)
IEEE 802.15.4-2006 PHY	2405–2480 MHz IEEE 802.15.5-2006 radio transceiver, implementing IEEE 802.15.5-2006 compliant • 250kbps, 2450MHz, O-QPSK PHY • Channels 11-26. Channel 11 2405MHz and CH26 2480MHz. • Clear channel assessment (CCA) • Energy detection (ED) scan • CRC generation
Nordic proprietary 1Mbps, 2Mbps, 4Mbps modes radio	2402–2480 MHz Nordic proprietary 1Mbps and 2Mbps modes radio transceiver • 1Mbps nRF proprietary mode (ideal transmitter) • 2Mbps nRF proprietary mode (ideal transmitter) • 4Mbps nRF proprietary mode (ideal transmitter)
Frequency	2.402 - 2.480 GHz for BLE (CH0 to CH39) 2.405 - 2.480 GHz for IEEE 802.15.4-2006 PHY (CH11 to CH26)
Raw Data Rates	1 Mbps BLE (over-the-air) 2 Mbps BLE (over-the-air) 125 kbps BLE (over-the-air) 500 kbps BLE (over-the-air) 250 kbps IEEE 802.15.4 802.15.4-2006 (over-the-air) Nordic proprietary 1Mbps, 2Mbps and 4Mbps modes (over-the-air)
Maximum Transmit Power Setting	+8 dBm Conducted 453-00001 (Integrated antenna) +8 dBm Conducted 453-00044 (External antenna)
Minimum Transmit Power Setting	-8 dBm (to +8dBm in <1dB steps)
Receive Sensitivity (≤37byte packet for BLE)	BLE 1 Mbps (BER=1E-3) -98dBm typical BLE 2 Mbps -TBDdBm typical BLE 125 kbps -106dBm typical BLE 500 kbps -TBDdBm typical IEEE 802.15.4-2006 250kbps -102dBm typical
Link Budget (conducted)	TBD dB 106dB @ BLE 1 Mbps TBD dB 114dB @ BLE 125 kbps

NFC	
NFC-Type A Listen mode compliant	**Based on NFC forum specification:** 13.56 MHz, Date rate 106 kbps, NFC Type2 and Type 4 emulation **Modes of Operation:** Disable, Sense, Activated **Use Cases:** Touch-to-Pair with NFC, NFC enabled Out-of-Band Pairing
Security	Designed for PSA Certified Level 3 with Secure Boot, Secure Firmware Update, and Secure Storage. Integrated tamper sensors detect attacks and take action, and cryptographic accelerators are hardened against side-channel attacks.

Host Interfaces and Peripherals	Applications Core (High Performance)	Software defined peripheral Core (ultra-low power)
Total		32 x multifunction I/O lines
Two co-processors	Arm Cortex-M33 with DSP, FPU, TrustZone support. 1524KB non-voltaile RRAM 256KB RAM L1 cache 128MHz clock Uses voltage and clock frequency scaling	RISC-V CPU (VPR) fast lightweight peripheral processor (FLPR) dedicated for software defined peripherals 16MHz clock
GPIO		Up to 32 multifunction GPIO's
	64MHz 1.7-3.6V GPIO port	16MHz 1.7-3.6V GPIO port P1.00-P1.15; P0.00-P0.04
ADC (14-bit)	14-bit 20KS/s with oversampling 12-bit 250KS/s 10-bit 2MS/s AIN0-AIN7 pins upto 8 programmable gain channels	
Global RTC (GRTC)		Implements full real time clock and calendar as shared system time. Can run in System OFF mode. Ultra low power, 1us resolution, 52bits wide, uses 16MHz clock, 32.76kHz when other power modes.
RTC		2x low power runs off LFCLK
High Speed SPI/UART	1 x	
SPI/UART/TWI		4x
PWM		3x 4channel PWM
I2S		1x I2S (Inter-IC sound interface)
PDM		1x PDM (Pulse code modulation interface) for digital microphones
TIMER		7x Timer (32bit)
QDEC		2x QDEC (Quadrature decoder)
COMP		1x COMP (comparator)
LPCOMP		1x LPCOMP (low power comparator)
TEMP		1x Temperature sensor Temperature range equal to operating temperature range
WDT		2x WDT (Watchdog timer)

NFC A-Tag	1x
Wakeup pins	21
External optional 32.768 kHz crystal	Not needed for normal radio operation. Optionally, connect +/-20ppm accuracy crystal for more accurate protocol timing. Fit associated load capacitor for crystal or use nRF54L15 internal load capacitor, which is configurable as TBD pF to TBD pF in TBDpF steps on pins XL1, XL2.
Security	Designed for PSA Certified Level 3 with Secure Boot, Secure Firmware Update, and Secure Storage. Integrated tamper sensors detect attacks and take action, and cryptographic accelerators are hardened against side-channel attacks.

Zephyr RTOS	**Via SWD (JTAG) 2 wire interface**
Programmability Options	**Nordic nRFConnect SDK:** Software/Support available from Nordic directly https://devzone.nordicsemi.com/ **Zephyr RTOS:** Software/Support available from https://www.zephyrproject.org/ **Canvas SW Suite**: Software/ Support available from https://www.ezurio.com/canvas/software-suite
FW upgrade	Via SWD (JTAG) 2 wire interface or UART
Supply Voltage	Normal Voltage Mode (VDD, VDDM_nRF): 1.7V-3.6V (Internal DCDC convertor or LDO)
Power Consumption	
Active Modes Peak Current (for maximum Tx power +8dBm) – Radio only	TBD mA peak Tx (with DCDC)
Active Modes Peak Current (for Tx power -8dBm) – Radio only	TBD mA peak Tx (with DCDC)
Active Modes Average Current	Depends on many factors, see section TBD
Ultra-low Power Modes	System ON Idle: TBD uA (wake on any event) System OFF: TBD uA (wake on reset)
Antenna Options	
Internal	Chip antenna – on-board (**453-00223 variant)**
External	Connection via *off module* IPEX MHF4 (**453-00224 RF trace pin variant)**
Physical	
Dimensions	7.9mm x 6.3mm x 1.75mm Pad Pitch – 0.65 mm Pad Type – Two rows of pads (LGA - Land Grid Array).
Weight	<1 gram
Environmental	
Operating	-40 °C to +105 °C
Storage	-40 °C to +105 °C
Miscellaneous	
Lead Free	Lead-free and RoHS compliant
Warranty	One-Year Warranty
Development Tools	
Development Kit	Development kit per module SKU (453-00223-K1 and 453-00224-K1 respectively)
Development Tools	Nordic nRFConnect - Android and iOS applications UART firmware upgrade Tools and utilities
Bluetooth®	Full Bluetooth SIG Declaration ID
FCC/ISED/CE/MIC/RCM/UKCA	All BL54L15µ Series

3 Hardware Specifications

3.1 Block Diagram and Pin-out

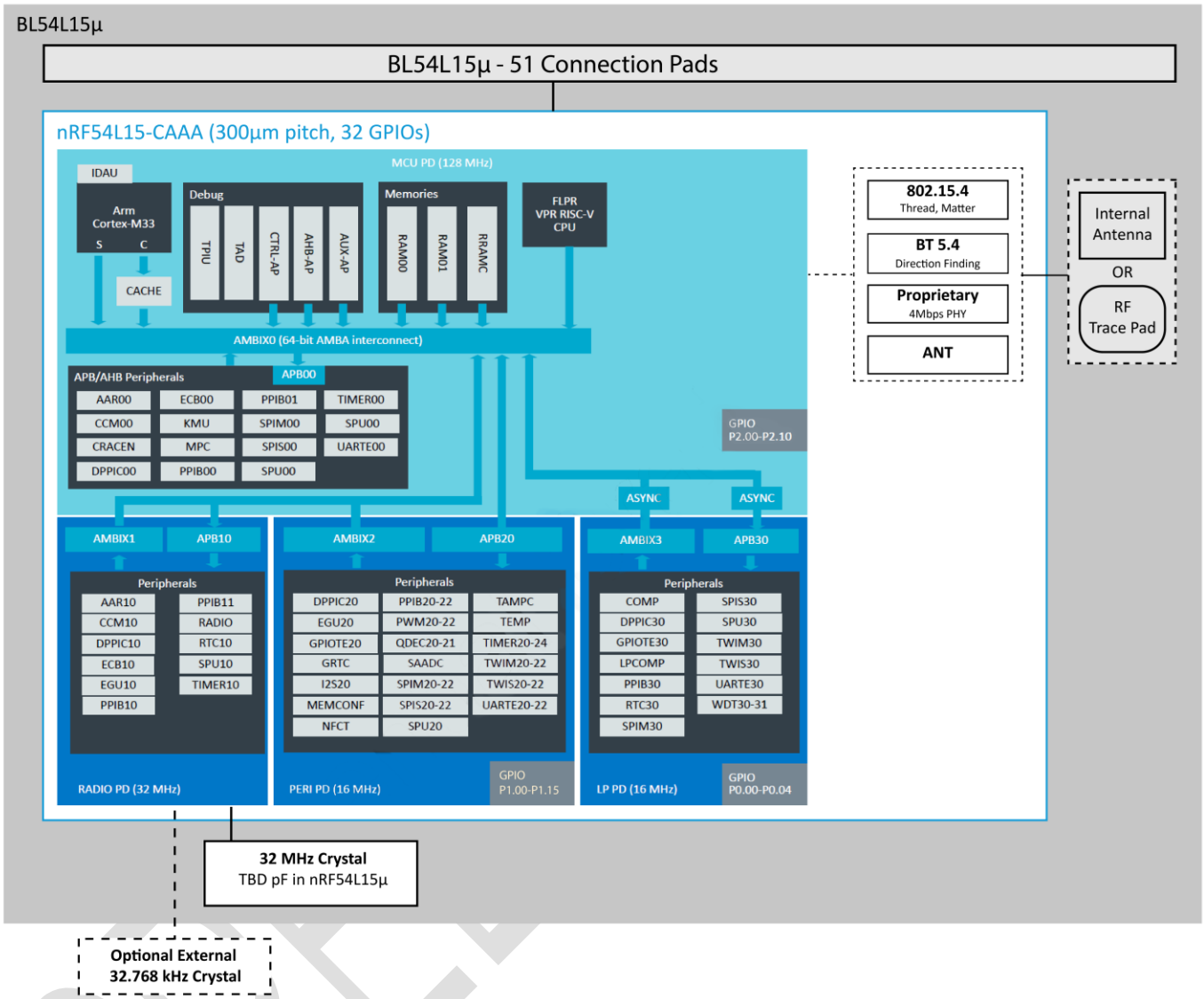


Figure 1: BL54L15µ HW block diagram

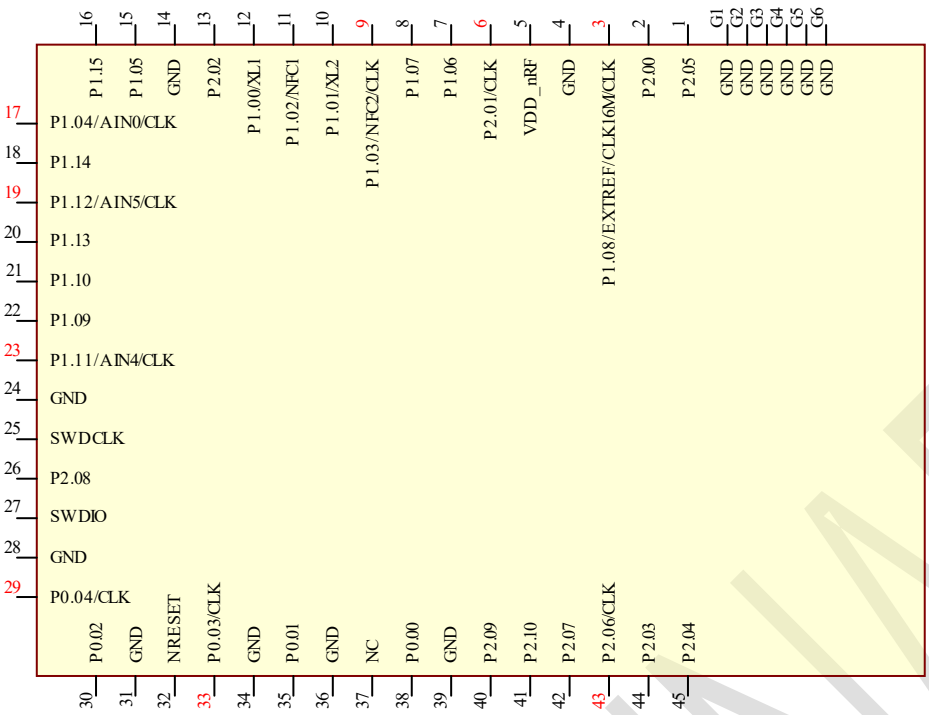


Figure 2: Top view - Schematic symbol for 453-00223 BL54L15µ Module (Nordic nRF54L15-CAAA) – Chip Antenna variant

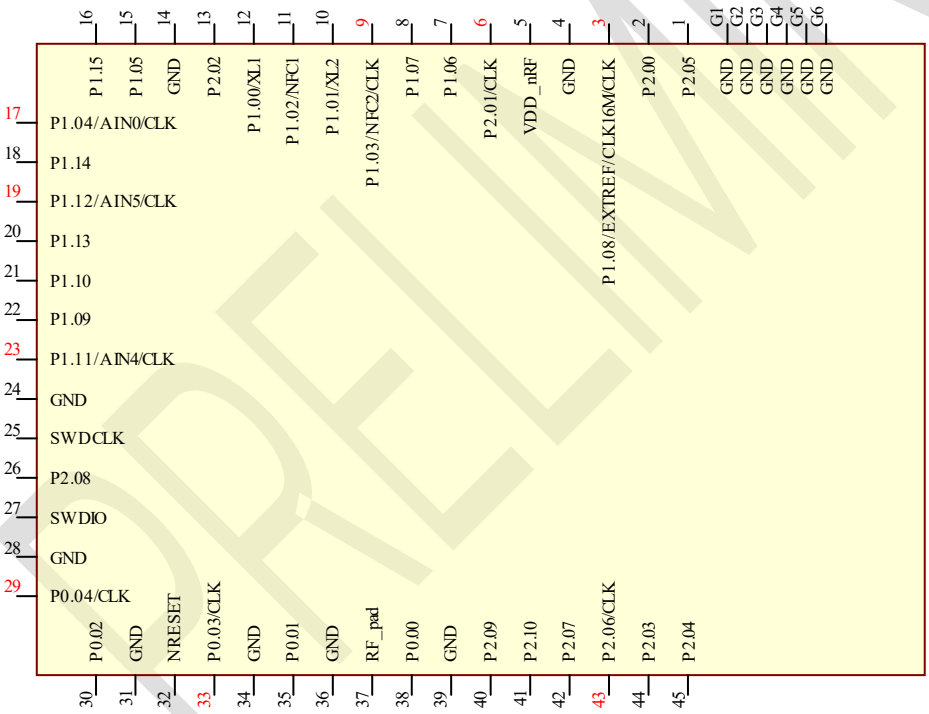


Figure 3: Top view - Schematic symbol for 453-00244 BL54L15µ Module (Nordic nRF54L15-CAAA) – RF Trace pin variant

3.2 Pin Definitions

Table 1: Pin definitions

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15-CAAA 300um WLCSP, 32 GPIOs	nRF54L15-CAAA 300u pitch WLCSP, 32GPIOs Name	Description	Example usage
1	P2.05	G5	P2.05/SPI.CS	General purpose I/O SPIM CS UARTE RTS QSPI CS	Clock pin SPIM00/SPIM20 UARTE00/UARTE20 FLPR
2	P2.00	G6	P2.00/SPI.DCX	General purpose I/O SPIM DCX UARTE RXD QSPI D3	 SPIM00/SPIM20 UARTE00/UARTE20 FLPR (QSPI)
3	P1.08/GRTCHFOUT/EXTREF	F7	P1.08/CLK16M/TAMPC.EXT/EXTREF	General purpose I/O GRTC HF clock output External reference for SAADC	Clock pin
4	GND		VSS		
5	VDD_nRF	G3	VDD	In Normal Voltage mode is an input 1.7V-3.6V, connect external supply of 1.7V-3.6V to pin11(VDD_nRF)	
6	P2.01	G7	P2.01/SPI.SCK	General purpose I/O SPIM SCK SPIS SCK QSPI SCK	Clock pin SPIM00/SPIM20 SPIS00/SPIS20 FLPR
7	P1.06/ASO[1]/AIN2	D7	P1.06/AIN2/TAMPC_ASO[1]	General purpose I/O Analog input TAMPC active shield output	 TAMPC
8	P1.07/ASI[1]/AIN3	E7	P1.07/AIN3/TAMPC_ASI[1]	General purpose I/O Analog input TAMPC active shield input	 TAMPC
9	P1.03/NFC2	D5	P1.03/NFC2	General purpose I/O Dedicated pin for NFC input	Clock pin
10	P1.01/XL2	C6	P1.01/XL2	General purpose I/O Connection for 32.768kHz crystal	Ezurio Devkit: Optional 32.768kHz crystal pad XL2, XL1 and associated 9pF load capacitor inside nRF54L15-CAAA chipset.
11	P1.02/NFC1	C7	P1.02/NFC1	General purpose I/O Dedicated pin for NFC input	

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15-CAAA 300um WLCSP, 32 GPIOs	nRF54L15-CAAA 300u pitch WLCSP, 32GPIOs Name	Description	Example usage
12	P1.00/XL1	C5	P1.00/XL1	General purpose I/O Connection for 32.768kHz crystal	Ezurio Devkit: Optional 32.768kHz crystal pad XL2, XL1 and associated 9pF load capacitor inside nRF54L15-CAAA chipset.
13	P2.02/SWO	F6	P2.02/SPI.MOSI	General purpose I/O SPIM MOSI SPIS MISO UARTE TXD QSPI D0 Serial wire output (SWO)	 SPIM00/SPIM20 SPIS00/SPIS20 UARTE00/UARTE20 FLPR Trace
14	GND		VSS		
15	P1.05/ASI[0]/AIN1	E6	P1.05/AIN1/TAMPC_ASI[0]	General purpose I/O TAMPC active shield input RADIO DFEGPIO Analog input	 TAMPC RADIO
16	P1.15	B6	P1.15	General purpose I/O	
17	P1.04/ASO[0]/AIN0	D6	P1.04/ TAMPC_ASO[0]/AIN0	General purpose I/O TAMPC active shield output Analog input	Clock pin TAMPC
18	P1.14/RADIO[5]/AIN7	B5	P1.14/AIN7	General purpose I/O RADIO DFEGPIO Analog input	 RADIO
19	P1.12/ASI[3]/RADIO[3]/AIN5	A3	P1.12/AIN5/TAMPC.ASI[3]	General purpose I/O TAMPC active shield input RADIO DFEGPIO Analog input	Clock pin TAMPC RADIO
20	P1.13/RADIO[4]/AIN6	B4	P1.13/AIN6	General purpose I/O RADIO DFEGPIO Analog input	 RADIO
21	P1.10/ASI[2]/RADIO[1]	C3	P1.10/TAMPC.ASI[2]	General purpose I/O TAMPC active shield input RADIO DFEGPIO	 TAMPC RADIO
22	P1.09/ASO[2]/RADIO[0]	B3	P1.09/TAMPC.ASO[2]/RADIO[0]	General purpose I/O TAMPC active shield output RADIO DFEGPIO	 TAMPC RADIO
23	P1.11/ASO[3]/RADIO[2]/AIN4	C4	P1.11/AIN4/TAMPC.ASO[3]	General purpose I/O TAMPC active shield output RADIO DEGPIO Analog input	Clock pin TAMPC RADIO
24	GND	-	VSS		

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15-CAAA 300um WLCSP, 32 GPIOs	nRF54L15-CAAA 300u pitch WLCSP, 32GPIOs Name	Description	Example usage
25	SWDCLK	E3	SWDCLK	Serial Wire Debug clock input for debug and programming	
26	P2.08/TRACEDATA[1]	D4	P2.08/TRACEDATA[1]/SPI.MOSI	General purpose I/O Trace data SPIM MOSI SPIS MISO UARTE TXD	 Trace SPIM00/SPIM21 SPIS00/SPIS21 UARTE00/UARTE21
27	SWDIO	F2	SWDIO	Serial Wire Debug IO for debug and programming	
28	GND	-	VSS		
29	P0.04/GRTCLFCLKOUT	D3	P0.04/GRTC_CLKOUT32K	General purpose I/O GRTC PLF clock output	Clock pin GRTC
30	P0.02	E2	P0.02	General purpose I/O	
31	GND	-	VSS		
32	nRESET	D2	nRESET	Pin RESET with internal pull-up resistor (13k Ohms). System Reset (Active Low).	
33	P0.03/GRTCPWM	E1	P0.03/GRTC_PWMOUT	General purpose I/O GRTC PWM output	Clock pin GRTC
34	GND	-	VSS		
35	P0.01	F1	P0.01	General purpose I/O	
36	GND	-	VSS		
37	RF_pad or NC	D1			RF pad active on BL54L15µ RF pin variant 453-00224. NC on BL54L15µ Integrated antenna variant 453- 00223.
38	P0.00	G1	P0.00	General purpose I/O	
39	GND	-	VSS		
40	P2.09/TRACEDATA[2]	F3	P2.09/TRACEDATA[2]/SPI.MISO	General purpose I/O Trace data SPIM MISO SPIS MOSI UARTE CTS	 Trace SPIM00/SPIM21 SPIS00/SPIS21 UARTE00/UARTE21
41	P2.10/TRACEDATA[3]	G2	P2.10/TRACEDATA[3]/SPIM.CS	General purpose I/O Trace SPIM CS UARTE RTS	 Trace SPIM00/SPIM21 UARTE00/UARTE21
42	P2.07/TRACEDATA[0]/SWO	E4	P2.07/TRACEDATA[0]/SWO/SPI.DCX	General purpose I/O Trace data Serial wire output (SWO) SPIM DCX UARTE RXD	 Trace Trace SPIM00/SPIM21 UARTE00/UARTE21
43	P2.06/TRACECLK	F4	P2.06/TRACECLK/SPI.SCK	General purpose I/O SPIM SCK SPIS SCK Trace clock	Clock pin SPIM00/SPIM21 SPIS00/SPIS21 Trace

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15-CAAA 300um WLCSP, 32 GPIOs	nRF54L15-CAAA 300u pitch WLCSP, 32GPIOs Name	Description	Example usage
44	P2.03	E5	P2.03	General purpose I/O QSPI D2	 FLPR
45	P2.04	F5	P2.04/SPI.MISO	General purpose I/O SPIM MISO SPIS MOSI UARTE CTS QSPI D1	 SPIM00/SPIM20 SPIS00/SPIS20 UARTE00/UARTE20 FLPR
G1	GND	-	VSS		
G2	GND	-	VSS		
G3	GND	-	VSS		
G4	GND	-	VSS		
G5	GND	-	VSS		
G6	GND	-	VSS		

Pin Definition Notes:

Note 1 **GPIO**	**GPIO = General Input or Output (GPIO level voltage tracks VDD pin). AIN =Analog input.** If GPIO is selected as an input, ensure the input is not floating (which can cause current consumption to drive with time in low power modes (such as System ON Idle), by selecting the internal pull up or pull down. **Must connect all GND pads to host board PCB GND plane.**
Note2 **Clock for serial interfaces or trace**	Some peripherals (SPI, TWI, PDM, I2S, TRACE, GRTC) have clock signals. Dedicated clock pins have been optimized to ensure correct timing relationship between clock and data signal for these peripherals. Pins that can be used as clock signals are shown with pin name in red colour. The peripheral data signal must be configured to use pins close to the clock pin. This ensures that the internal paths from the peripheral to the pin have the same delay, so that the data and clock signals reach the pins at the same time. For high-speed signals, the printed circuit board (PCB) layout must use short PCB traces of identical length. This makes sure any delays are kept to a minimum and it assures close to identical delay and clock path.
Note 3 **Dedicated pins**	UARTE20/21: Can use any pin son GPIO port P1. Can be connected across power domains to dedicated pin on P2. SPIM00: Has dedicated pins on GPIO port P2. For 32MHz operation, the pins must be configured using extra high drive E0/E1 configuration. SPIM20/21: Can use any pin son GPIO port P1. Can be connected across power domains to dedicated pin on P2. SPIS20/21: Can use any pin son GPIO port P1. Can be connected across power domains to dedicated pin on P2. TRACE: Has dedicated pins on GPIO port P2. For 32MHz operation, the pins must be configured using extra high drive E0/E1 configuration. GRTC: Has dedicated pins for clock and PWM output. TAMPC: Has dedicated pins for active shield inputs and outputs. FLPR: Uses dedicated pins on GPIO port P2 for emulated peripherals such as QSPI. RADIO: Uses dedicated pins on GPIO port P1 for antenna switch control (DFEGPIO for direction finding). NFC: Uses dedicated pin listed in pin definitions table1.
Note 4 **SWDIO / SWCLK / nRESET / VDD / GND**	Customer MUST bring out SWDIO, SWCLK, nRESET, VDD, GND for programming purposes.
Note 5 **GPIO P2.15**	P2.15 GPIO is only available on the BL54L15µ which uses nRF54-CAAA(300um pitch) which as 32 GPIO's.
Note 6 **RF_PAD**	RF_pad (pin37) is for the BL54L15µ RF pad variant (453-00224) module only. If using the BL54L15µ module RF pad variant (453-00224), customer MUST copy the 50-Ohms GCPW RF track design, MUST add series 2nH RF inductor (Murata LQG15HN2N0B02# or Murata LQG15HS2N0B02) and RF connector IPEX MHF4 Receptacle (MPN: 20449-001E) detailed in 50-Ohms RF Trace and RF Match Series 2nH RF inductor on Host PCB for BL54L15µ RF pad variant (453-00224)

3.3 Electrical Specifications

3.3.1 Absolute Maximum Ratings

Absolute maximum ratings are the extreme limits for supply voltage and voltages on digital and analogue pins of the module are listed below; exceeding these values causes permanent damage.

Table 2: Absolute maximum ratings

Parameter	Min	Max	Unit
VDD_nRF	TBD	TBD	V
Voltage at GND pin	TBD	0	V
I/O pin voltage			
Voltage at GPIO pin (at VDD≤3.6V)	TDB	TBD	V
NFC antenna pin current (NFC1/2)	-	TBD	mA
Radio RF input level	-	TBD	dBm
Environmental			
Storage temperature	-40	+105	°C
MSL (Moisture Sensitivity Level)	-	4	-
ESD (as per EN301-489)			
Conductive		4	kV
Air Coupling		8	kV
Flash Memory (Endurance) (Note 2)	TBD		Write/erase cycles
Flash Memory (Retention)	TBD years at TBD °C		years at TBD °C

Absolute maximum Ratings Notes:	
Note 1	The absolute maximum rating for VDD pin (max) is TBD V for the BL54L15µ.
Note 2	Wear levelling can be implemented by customer.

3.3.2 Recommended Operating Parameters

Table 3: Power supply operating parameters

Parameter	Min	Typ	Max	Unit
VDD_nRF (independent of DCDC) supply range	1.7		3.6	V
VDD Maximum ripple or noise (See Note 1)	-	-	10	mV
Time in Power-on reset after supply reaches minimum operating voltage, depend on supply rise time.				
VDD supply rise time (0V to 1.7V)² 10uS	-	TBD	TBD	mS
VDD supply rise time (0V to 1.7V)² >10mS	-	TBD	TBD	mS
Operating Temperature Range	-40	+25	+105	°C

Recommended Operating Parameters Notes:	
Note 1	This is the maximum VDD_nRF ripple or noise (at any frequency) that does not disturb the radio.
Note 2	The on-board power-on reset circuitry may not function properly for rise times longer than the specified maximum.
Note 3	BL54L15µ power supply: **Normal Voltage Mode** – Connect external supply voltage (within range 1.7V-3.6V) to VDD_nRF pin.

3.4 Clocks

3.4.1 HFXO - 32MHz crystal oscillator and nRF54L15 internal load capacitor TBD pF mandatory setting

The BL54L15µ module contains the 32 MHz crystal, but the load capacitors to create 32MHz crystal oscillator circuit are inside the nRF54L15 chipset. Customer MUST set the internal nRF54L15 capacitors to TBD pF (for proper operation of the 32 MHz crystal circuit).

The 32 MHz crystal inside the BL54L15µ module is a high accuracy crystal (±15 ppm at room temperature) that helps with radio operation and reducing power consumption in the active modes.

3.4.2 LFCLK – Low Frequency clock source

There are four possibilities (see figure 5) for the low frequency clock (LFCLK) and options are:

LFRC (32.768kHz RC oscillator): The Internal 32.768 kHz RC oscillator (LFRC) is fully embedded in nRF54L15 (and does not require additional external components) with an accuracy ±250 ppm (after calibration of LFRC at least every eight seconds using the HFXO as a reference oscillator).

LFXO (32.768kHz crystal oscillator): For higher LFCLK accuracy (greater than ±250ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used. To use LFXO, a 32.768kHz crystal must be connected between the XL1 and XL2 pins and the load capacitance between each crustal terminal and ground. Optionally internal (to nRF54L15) capacitor of maximum TBDpF in TBDpF steps are provided on pins XL1 and XL2.

Low frequency (32.768 kHz) external source: The 32.768 kHz oscillator (LFXO) is designed to work with external sources

LFSYNTH (32.768kHz Synthesised clock) from HFCLK (LFSYNTH): The LFCLK can be synthesised from the HFCLK source. LFSYNTH depends on the HFCLK to run. The accuracy of the LFCLK clock with LFSYNTH as a source assumes the accuracy of the HFCLK. If high accuracy is required, the HFCLK must generated from the HFXO. Using the LFSYNT clock removes the requirement for an external 32.768kHz crystal but the increases the average power consumption as the HFCLK will turned on in the system.

3.4.3 Other Internal Clocks

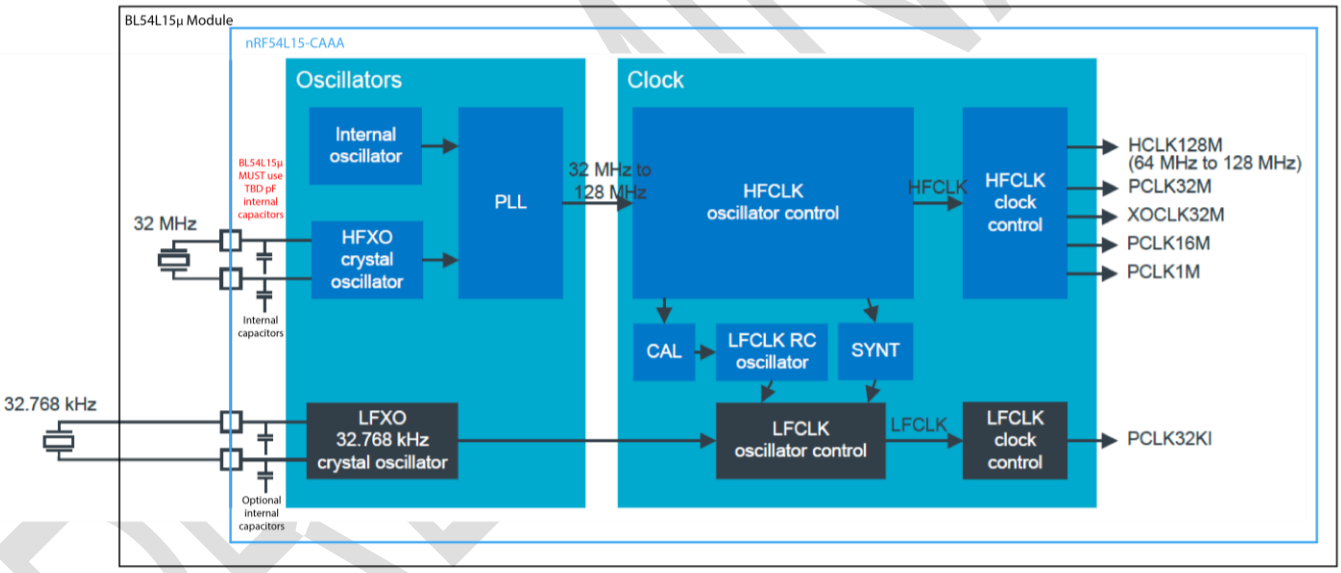


Figure 4: nRF54L15 Clock System Overview (adapted from Nordic)

3.5 BL54L15µ Power Supply

The BL54L15µ module power supply internally contains the following main supply regulator stage (Figure 5):

- VREGMAIN – Connected to the VDD_nRF pin

Normal voltage mode power supply mode is entered when the external supply voltage (1.7V-3.6V) is connected to VDD_nRF pin. See Figure 5.

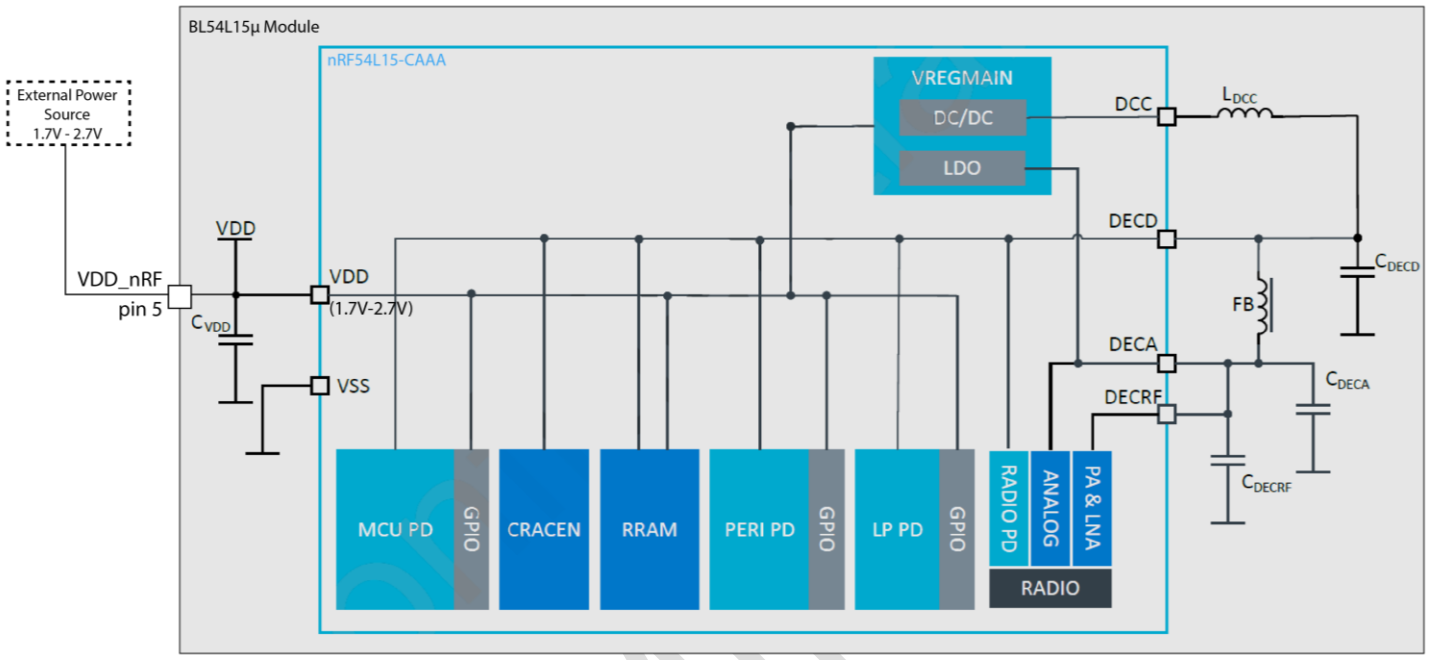


Figure 5: BL54L15µ power supply block diagram (adapted from Nordic) for Normal Voltage Mode

4 Mandatory SW requirements related to hardware

4.1 32MHz crystal internal load capacitor setting of TBD pF

MANDATORY. BL54L15µ module contains the 32 MHz crystal but the load capacitors to create 32 MHz crystal oscillator circuit are inside the nRF54L15-CAAA chipset. Customer MUST set the internal nRF54L15 capacitors to TBD pF (for proper operation of the 32 MHz crystal circuit in the BL54L15µ module).

5 Hardware Integration Suggestions

5.1 Circuit

The BL54L15µ is easy to integrate, requiring one mandatory external 10uF capacitor on customers board and apart from that those components which customer require for development and in your end application.

The following are suggestions for your design for the best performance and functionality.

Checklist (for Schematic):

- **BL54L15µ power supply:**
  Normal voltage mode power supply mode is entered when the external supply voltage (1.7V-2.7V) is connected to VDD_nRF pin(pin5).

  External power source should be within the operating range, rise time and noise/ripple specification of the BL54L15µ. Add decoupling capacitors for filtering the external source. Power-on reset circuitry within BL54L15µ series module incorporates brown-out detector, thus simplifying your power supply design. Upon application of power, the internal power-on reset ensures that the module starts correctly.
- **AIN (ADC) and GPIO pin IO voltage levels**
  BL54L15µ GPIO voltage levels are at VDD. Ensure input voltage levels into GPIO pins are at VDD also (if VDD source is a battery whose voltage drops). Ensure ADC pin maximum input voltage for damage is not violated.
- **AIN (ADC) impedance and external voltage divider setup**
  If you need to measure with ADC a voltage higher than 3.6V, you can connect a high impedance voltage divider to lower the voltage to the ADC input pin.
- **SWD**
  This is REQUIRED for loading firmware. MUST wire out the SWD two wire interface on host design. Five lines should be wired out, namely SWDIO, SWDCLK, nRESET, GND and VDD.
- **UART and flow control (CTS, RTS)**
  Required if customer requires UART.
- **TWI (I2C)**
  It is essential to remember that pull-up resistors on both SCL and SDA lines are required, the value as per I2C standard. BL54L15µ (nRF54L15-CAAA) can provide 13K Ohms typical pull up values internally. For other values, fit external pull-up resistor on both SCL and SDA as per I2C specification to set speed. The I2C specification allows a line capacitance of 400pF.
- **QSPI, High Speed SPI, High speed TWI (I2C, 1Mbps) and Trace**
  High-Speed SPI, TWI and Trace come on dedicated GPIO pins only. Other lower speed SPI and TWI can come out on any GPIO pins.
  For all high-speed signal, the printed circuit board (PCB) layout must ensure that connections are made using short PCB traces.
- **GPIO pins**
  If GPIO is selected as an input, ensure the input is not floating (which can cause current consumption to drive with time in low power modes (such as System ON Idle), by selecting the internal pull up or pull down.
- **NFC antenna connector** To make use of the Ezurio flexi-PCB NFC antenna (part # 0600-00061), fit connector:
  - Description – FFC/FPC Connector, Right Angle, SMD/90d, Dual Contact,1.2 mm Mated Height
  - Manufacturer – Molex
  - Manufacturers Part number – 512810594

  Add tuning capacitors of 300 pF on NFC1 pin to GND and 300 pF on NFC2 pins to GND if the PCB track length is similar as development board.
- **nRESET pin (active low)**
  Hardware reset. Wire out to push button or drive by host.
  By default module is out of reset when power applied to VDD pins (13K pull-up inside BL54L15µ (nRF54L15-CAAA)).
- **Optional External 32.768kHz crystal**

  If the optional external 32.768kHz crystal is needed, then use a crystal that meets specification and add load capacitors (either inside nRF541L15-CAAA or discrete capacitors outside BL54L15µ (nRF54L15-CAAA) whose values should be tuned to meet all specification for frequency and oscillation margin.
- **BL54L15µ module RF pad variant (453-00224)**

  RF_pad (pin37) is for the BL54L15µ RF pad variant (453-00224) module only. If using the BL54L15µ module RF pad variant (453-00224), customer MUST copy the 50-Ohms GCPW RF track design, MUST add series 2nH RF inductor (Murata LQG15HN2N0B02# or Murata

LQG15HS2N0B02) and RF connector IPEX MHF4 Receptacle (MPN: 20449-001E) Detailed in the following section:
Error! Reference source not found.

5.2 PCB Layout on Host PCB - General

Checklist (for PCB):

- MUST locate BL54L15µ module close to the edge of PCB (mandatory for the 453-00223 for on-board chip antenna to radiate properly).
- Use solid GND plane on inner layer (for best EMC and RF performance).
- All module GND pins MUST be connected to host PCB GND.
- Place GND vias close to module GND pads as possible.
- Unused PCB area on surface layer can flooded with copper but place GND vias regularly to connect the copper flood to the inner GND plane. If GND flood copper is on the bottom of the module, then connect it with GND vias to the inner GND plane.
- Route traces to avoid noise being picked up on VDD supply and AIN (analogue), GPIO (digital) traces and high-speed traces.
- Ensure no exposed copper is on the underside of the module (refer to land pattern of BL54L15µ development board).

5.3 PCB Layout on Host PCB for the 453-00223

5.3.1 Antenna Keep-out on Host PCB

The 453-00223 has an integrated chip antenna and its performance is sensitive to host PCB. It is critical to locate the 453-00223 on the edge of the host PCB (or corner) to allow the antenna to radiate properly. Refer to guidelines in section ***PCB land pattern and antenna keep-out area for the 453-00223***. Some of those guidelines repeated below.

- Ensure there is no copper in the antenna keep-out area on any layers of the host PCB. Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.
- For best antenna performance, place the 453-00223 module on the edge of the host PCB, preferably in the edge center.
- The BL54L15µ development board (453-00223-K1) has the 453-00223 module on the edge of the board (not in the corner). The antenna keep-out area is defined by the BL54L15µ development board which was used for module development and antenna performance evaluation is shown in Figure 6, where the antenna keep-out area is 3mm wide, 5mm long; with PCB dielectric (no copper) height ~1.75mm sitting under the 453-00223 chip antenna module.
- The 453-00223 chip antenna is tuned when the 453-00223 is sitting on development board (host PCB) with size of 113mm x 63.5mm x1.75mm.
- A different host PCB thickness dielectric will have small effect on antenna.
- The antenna-keep-out defined in the 6.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00223 section.
- Host PCB land pattern and antenna keep-out for the BL54L15µ applies when the 453-00223 is placed in the edge of the host PCB preferably in the edge center. Figure 6 shows an example.

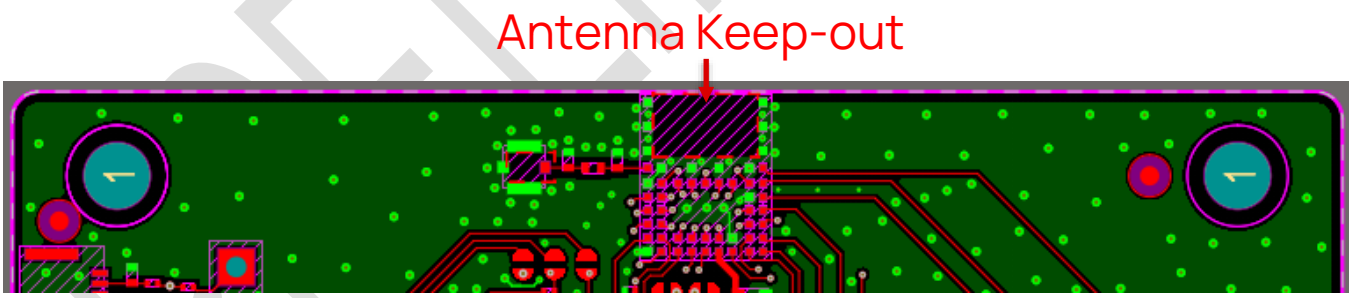


Figure 6: Chip Antenna keep-out area (shown in red) of the BL54L15µ development board for the 453-00223 module.

Antenna Keep-out Notes:	
Note 1	The BL54L15µ module is placed on the edge, preferably edge centre of the host PCB.
Note 2	Copper cut-away on all layers in the *Antenna Keep-out* area under the 453-00223 on host PCB.

5.3.2 Antenna Keep-out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40 mm top/bottom and 30 mm left or right.
- Metal close to the 453-00223 Chip antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. The amount of that degradation is entirely system dependent, meaning you will need to perform some testing with your host application.
- Any metal closer than 20 mm will begin to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that you test the range with a mock-up (or actual prototype) of the product to assess effects of enclosure height (and materials, whether metal or plastic) and host PCB ground (GND plane size).

5.4 50-Ohms RF Trace and RF Match Series 2nH RF inductor on Host PCB for BL54L15µ RF pad variant (453-00224)

To use an external antenna requires BL54L15µ module variant with RF trace pad (453-00224) and 50-Ohm RF trace (GCPW, that is Grounded Coplanar Waveguide) from RF_pad (pin37) of the module (BL54L15µ 453-00053) to RF antenna connector (IPEX MHF4) on host PCB. On this RF path, MUST use 2nH series RF inductor. BL54L15µ module GND pin36 and GND pin3 used to support GCPW 50-Ohm RF trace.

Checklist for SCH

- MUST fit 2 nH RF inductor (L1) in series. RF inductor part number is Murata LQG15HN2N0B02# or Murata LQG15HS2N0B02# with 0402 body size.
  https://www.murata.com/en-eu/products/productdetail.aspx?partno=LQG15HN2N0B02%23
  https://www.murata.com/en-eu/products/productdetail.aspx?partno=LQG15HS2N0B02%23
- MUST fit RF connector IPEX MHF4 Receptacle (MPN: 20449-001E), https://www.i-pex.com/product/mhf-4-smt#!

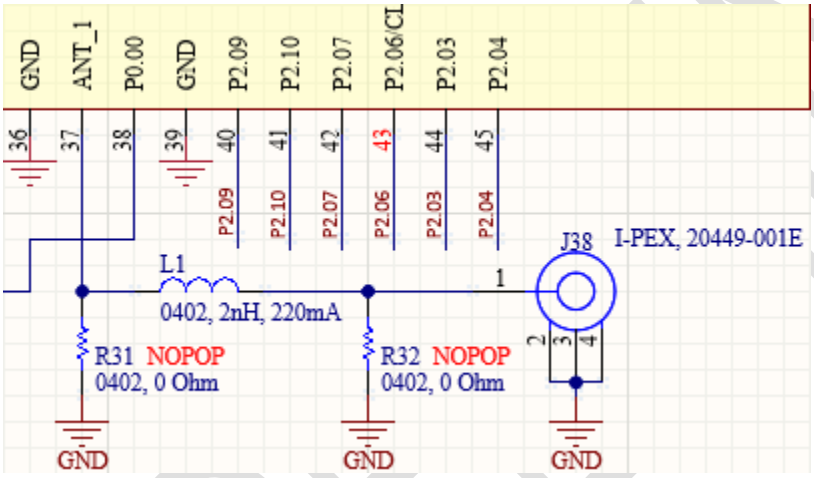
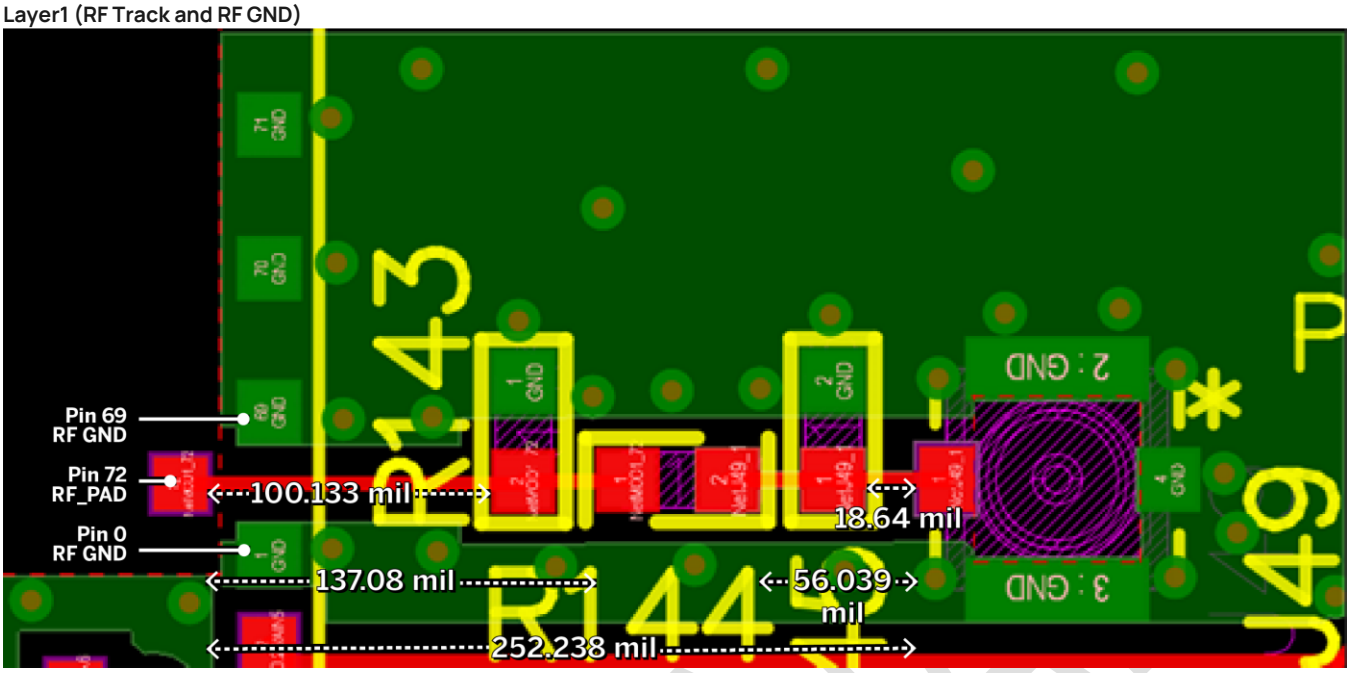


Figure 7: BL54L15µ RF trace pad variant (453-00224) Host PCB 50-Ohm RF trace schematic with series 2nH inductor, RF connector

Layer1 (RF Track and RF GND)



Layer2 (RF GND) and Layer2 copper cut-out under RF connector

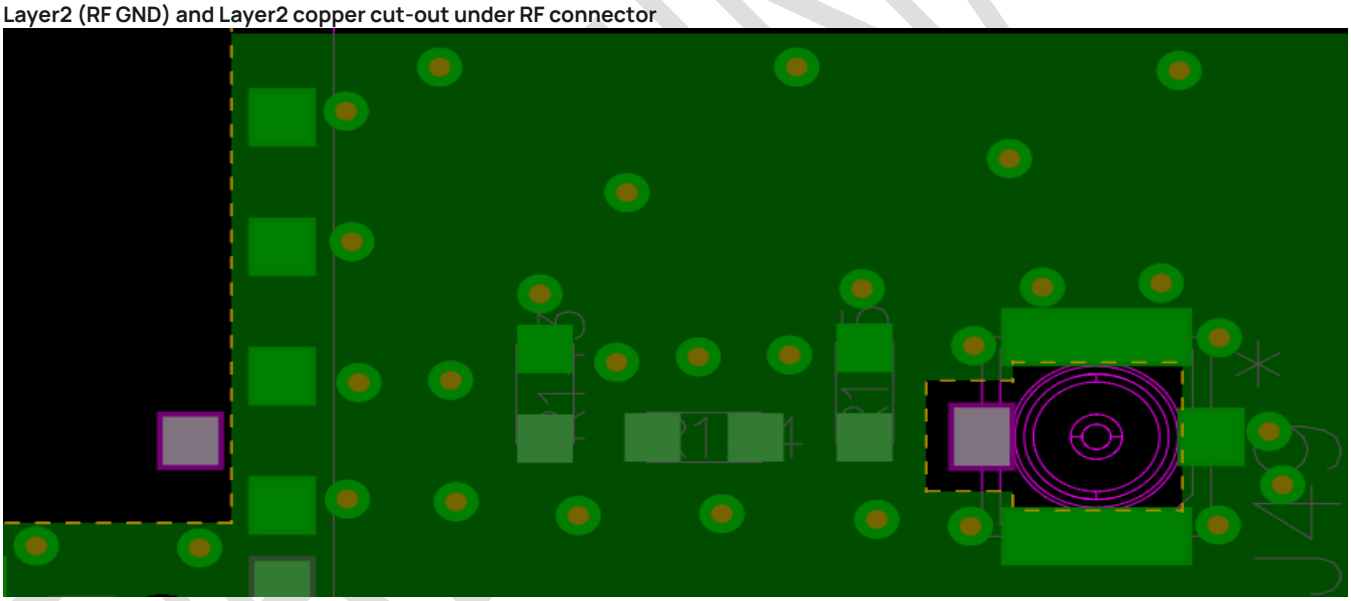
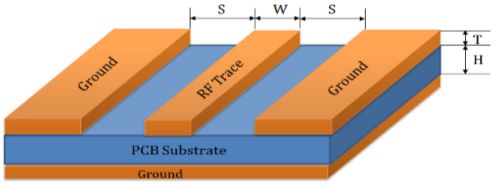


Figure 8: 50-Ohm RF trace design (Layer1 and Layer2) on BL54L15µ development board (or host PCB) for use with BL54L15µ RF trace pin variant (453-00224) module

Checklist for PCB:

▪ MUST use a 50-Ohm RF trace (GCPW, that is Grounded Coplanar Waveguide) from RF_pad (pin72) of the module (BL54L15µ 453-00224) to RF antenna connector (IPEX MHF4) on host PCB.

▪ To ensure regulatory compliance, MUST follow exactly the following considerations for 50-Ohms RF trace design and test verification:



	Thickness	Dielectric	
	mil	Constant Er	
Solder Mask	0.4	3.5	Stack up for 50 Ohms GCPW RF track.
Layer1 Copper 0.5 oz+plating (Note1)	1.3		
Prepreg (2113)	3.8	4.1	
Layer2 Copper 1 oz	1.2		
Core 0.6 mm	23.62	4.52	
Layer3 Copper 1 oz	1.2		
Prepreg (2113)	3.8	4.1	
Layer1 Copper 0.5 oz+plating	1.3		
Solder Mask	0.4	3.5	

Figure 9: BL5340 development board PCB stack-up and L1 to L2 50-Ohms Grounded CPW RF trace design

Note 1: The plating (ENIG) above base 0.5 oz copper is not listed, but plating expected to be ENIG.

- The 50-Ohms RF trace design MUST be Grounded Coplanar Waveguide (GCPW) with
  - Layer1 RF track width (W) of 6.0 mil and
  - Layer1 gap (G) to GND of 10 mil and where the
  - Layer1 to Layer 2 dielectric thickness (H) MUST be 3.8 mil (dielectric constant Er 4.1).
  - Further the Layer1 base copper must be 0.5-ounce base copper (that is 0.7 mil) plus the plating and
  - Layer1 MUST be covered by solder mask of 0.4 mil thickness (dielectric constant Er 3.5).
- The 50-Ohms RF trace design MUST follow the PCB stack-up shown in Figure 9. (Layer1 to Layer2 thickness MUST be identical to the BL5340 development board).
- The 50-Ohms RF track should be a controlled-impedance trace e.g., ±10%.
- The 50-Ohms RF trace length MUST be identical (as seen in Figure 8) (252.238mil) to that on the BL54L15µ development board from BL54L15µ module RF pad (pin37) to the RF connector IPEX MHF4 Receptable (MPN: 20449-001E).
- Place GND vias regularly spaced either side of 50-Ohms RF trace to form GCPW (Grounded coplanar waveguide) transmission line as shown in Figure 8 and use BL5340 module GND pin1 and GND pin69.
- Cut away copper on Layer2 GND layer under the RF connector IPEX MHF4 Receptable, as seen in Figure 8. This is to reduce RF detuning the 50Ohms of the RF connector (J49) when it sits on the PCB.
- Cut away copper on Layer2 GND layer under the BL5340 module RF pad (pin72), identical to the BL54L15µ development board as seen in Figure 8.
- Use spectrum analyzer to confirm the radiated (and conducted) signal is within the certification limit.

5.5 External Antenna Integration with BL54L15µ RF trace pin variant (453-00224)

Please refer to the regulatory sections for FCC, ISED, CE, MIC, UKCA and RCM details of use of BL54L15µ with external antennas in each regulatory region.

The BL54L15µ family has been designed to operate with the below external antennas (with a maximum gain of 2.32 dBi). The required antenna impedance is 50 ohms. See Table 4. External antennas improve radiation efficiency.

Table 4: External antennas for the BL54L15µ RF trace pin variant (453-00224)

Manufacturer	Model	Ezurio Part Number	Type	Connector	Peak Gain	
					2400-2500 MHz	2400-2480 MHz
Ezurio (Laird Connectivity)	NanoBlue	EBL2400A1-10MH4L	PCB Dipole	IPEX MHF4	2 dBi	-
Ezurio (Laird Connectivity)	FlexPIFA	001-0022	PIFA	IPEX MHF4	-	2 dBi
Mag.Layers	EDA-8709-2G4C1-B27-CY	0600-00057	Dipole	IPEX MHF4	2.32 dBi	-
Ezurio (Laird Connectivity)	mFlexPIFA	EFA2400A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	iFlexPIFA Mini	EFG2401A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	Ezurio NFC	0600-00061	NFC	N/A	-	-

6 Mechanical Details

6.1 BL54L15 Mechanical Details

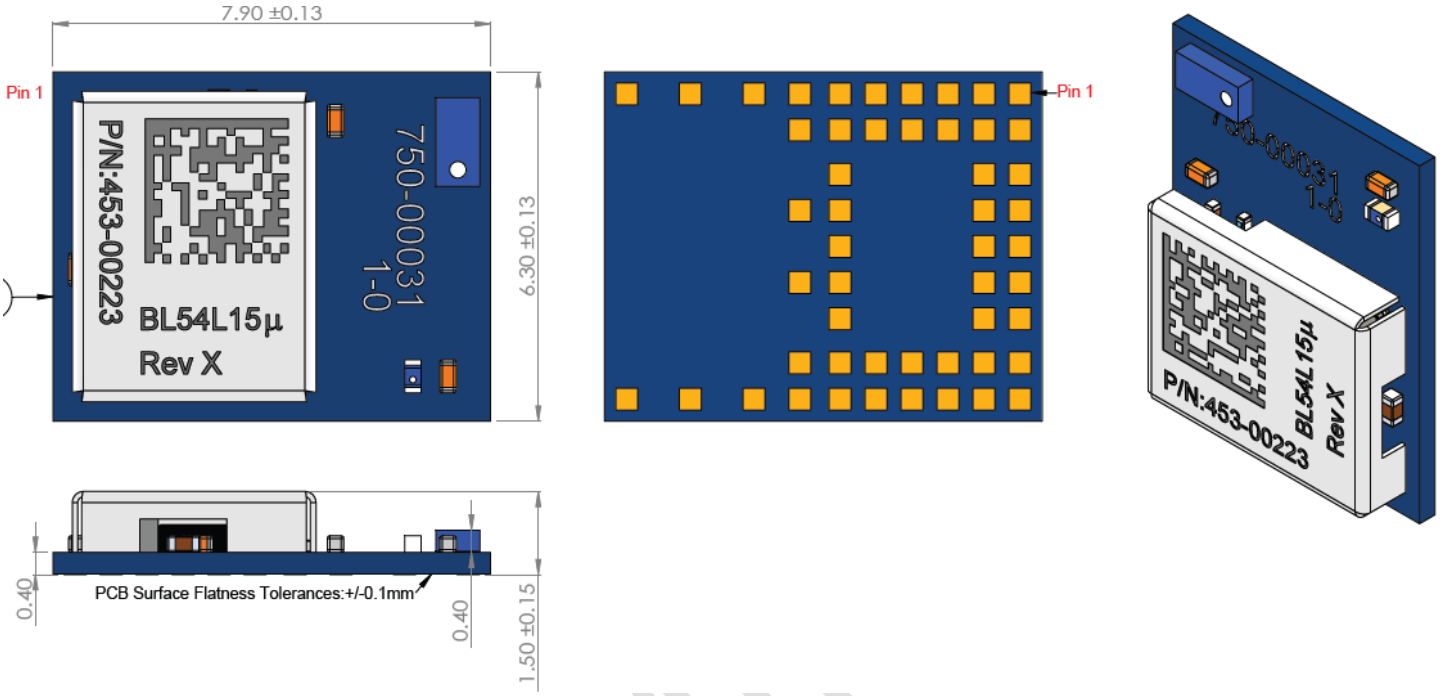


Figure 10: Mechanical Details – Internal Antenna variant (453-00223)

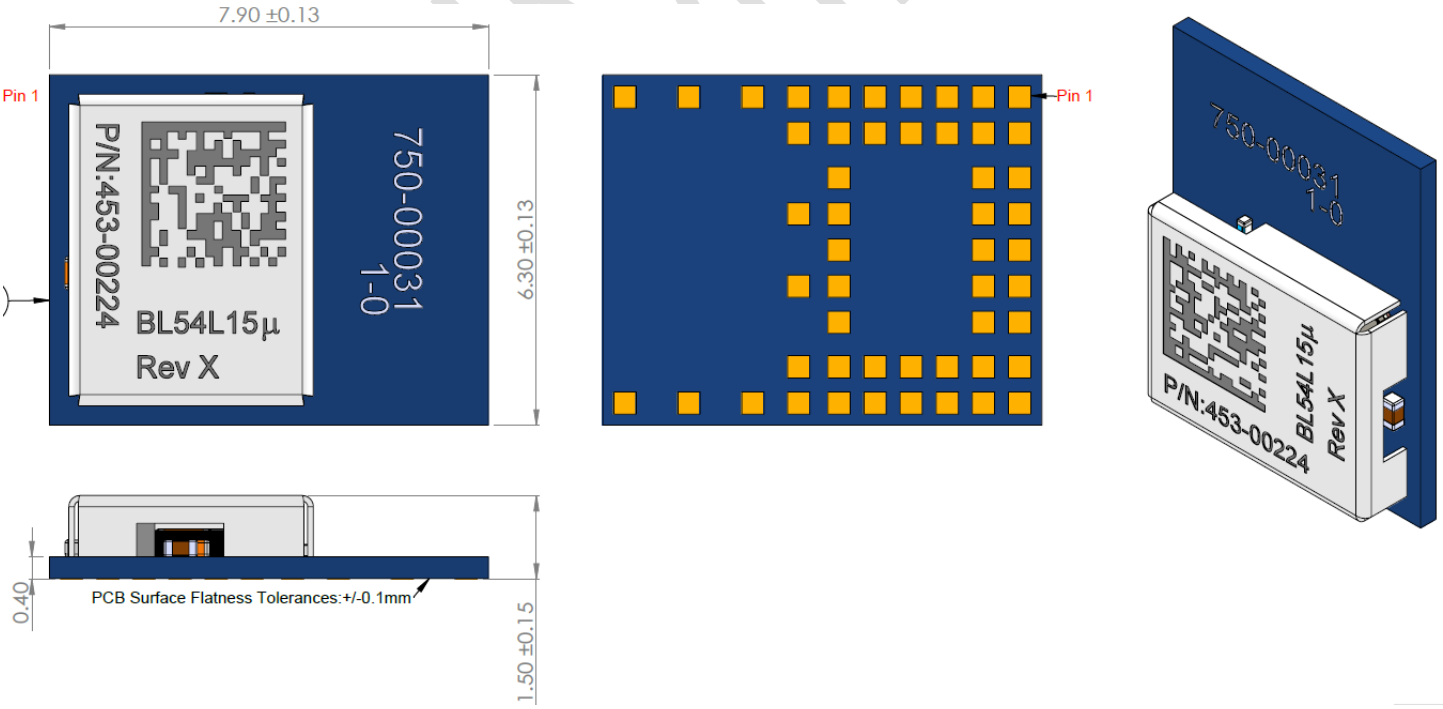
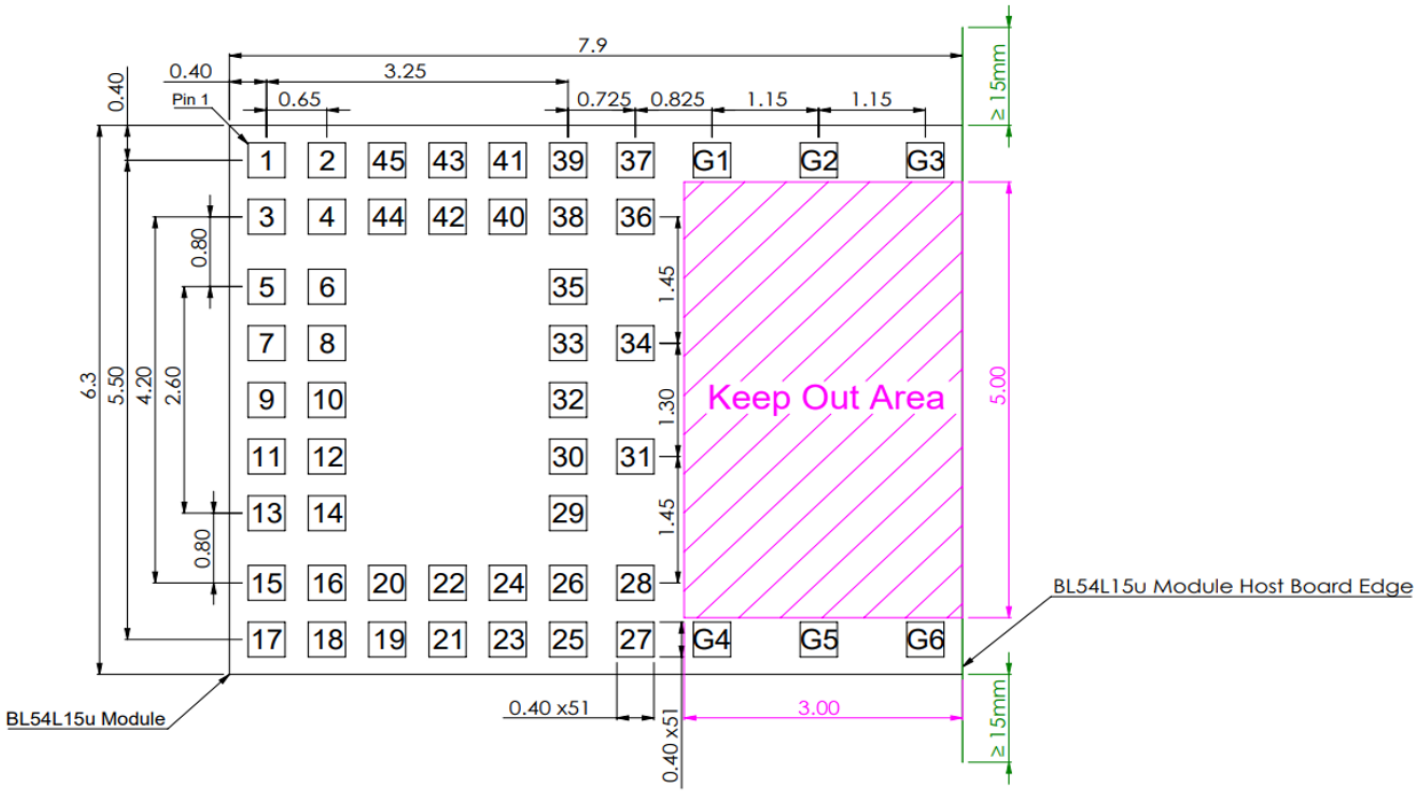


Figure 11: Mechanical Details – RF Trace pin variant (453-00224)

3D models for BL54L15µ Module, RF Trace Pin (453-00224) and BL54L15µ Module, Chip Antenna (453-00223) on the BL54L15µ product page – https://www.ezurio.com/product/BL54L15µ-series-bluetooth-le-80215-4-nfc

6.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00223

PCB footprint - BL54L15µ (DXF and Altium format) and SCH Symbol - BL54L15µ (Altium format) can be found on the BL54L15µ product page – https://www.ezurio.com/product/BL54L15µ-series-bluetooth-le-80215-4-nfc



All dimensions are in mm.

Figure 12: Land pattern and Keep-out for the 453-00223

Host PCB Land Pattern and Antenna Keep-out for the 453-00xxx Notes:	
Note 1	Ensure there is no copper in the antenna 'keep out area' on any layers of the host PCB. Also keep all mounting hardware or any metal clear of the area (Refer to 5.3.2) to reduce effects of proximity detuning the antenna and to help antenna radiate properly.
Note 2	For the best on-board chip antenna performance, the module 453-00223 MUST be placed on the edge of the host PCB and preferably in the edge centre and host PCB, the antenna "Keep Out Area" is extended (see Note 4).
Note 3	BL54L15µ development board has the 453-00223 placed on the edge of the PCB board (and not in corner) for that the Antenna keep out area is extended down to the corner of the development board, see section 6.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00223.
Note 4	Ensure that there is no exposed copper under the module on the host PCB.
Note 5	You may modify the PCB land pattern dimensions based on their experience and/or process capability.

7 Ordering Information

Part Number	Product Description
453-00223R	Module, BL54L15µ, (Nordic nRF54L15), Chip antenna, Tape/Reel
453-00224R	Module, BL54L15µ, (Nordic nRF54L15), RF Trace Pin, Tape/Reel
453-00223C	Module, BL54L15µ, (Nordic nRF54L15), Chip antenna, Cut Tape
453-00224C	Module, BL54L15µ, (Nordic nRF54L15), RF Trace Pin, Cut Tape
453-00223-K1	Development kit, Module, BL54L15µ (Nordic nRF54L15), Chip antenna
453-00224-K1	Development kit, Module, BL54L15µ (Nordic nRF54L15), RF Trace Pin

8 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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