Datasheet

BL54L15µ Series

Version 1.1

Revision History

Version	Date	Notes	Contributor(s)	Approver
0.1	02 Oct 2024	Preliminary release.	Raj Khatri	Jonathan Kaye
0.2	18 Oct 2024	Updated table4 external antenna list to Added antenna Ezurio iFlexPIFA Mini EFG2401A3S-10MH4L to External Antenna Integration with BL54L15µ RF trace pin variant (453-00224) Change Mag Layers EDA-8709-2G4C1-B27-CY antenna gain from 2dBi to 2.32dBi.	Raj Khatri	Jonathan Kaye
0.3	5 Nov 2024	Updated height of module to 1.75 mm.	Dave Drogowski	Jonathan Kaye
0.4	20 Nov 2024	Updated power supply voltage to 1.7 – 3.6 V.	Dave Drogowski	Jonathan Kaye
0.5	19 Feb. 25	Updated 6. Mechanical Details, 7.On -Board PCB Chip Antenna Characteristics, 8.Application Note for Surface Mount Modules, 9.Reliability Test	Louis Chang	Jonathan Kaye
0.6	18 Mar. 25	Update Power consumption in 2.1	Louis Chang	Jonathan Kaye
0.7	11 Apr. 25	Change (VDD_nRF) operating range from 1.7V-3.6V to 1.7V-3.5V. Add VDD_nRF supply voltage (1.7V-3.3V) under extended operating Temperature (85 to 105C) Update Absolute maximum ratings of VDD_nRF (-0.3V-3.6V)	Louis Chang	
1.0	26 June 2025	Initial Release.	Louis Chang Dave Drogowski	Jonathan Kaye
1.1	1 Aug 2025	Updated max output power to +8 dBm	Dave Drogowski	Jonathan Kaye

Contents

1 Overview and Key Features

Experience a new pinnacle of performance, efficiency, and security with our new BL54L15µ series, built on Nordic Semiconductor's powerful **nRF54** silicon. Elevating what you know and love from the nRF52 series, this next generation redefines Bluetooth LE and 802.15.4 solutions. Unleashing enhanced processing power, expanded memory, and innovative peripherals, the BL54L15µ is the ultimate choice for low power connectivity, in the smallest footprint.

Powered by **Nordic's nRF54L15** (WLCSP 300um) SoC, our ultra compact BL54L15µ modules deliver secure and robust Bluetooth LE and 802.15.4 with flexible programming via the Nordic SDK, Zephyr RTOS and Canvas Software Suite.

Featuring a **128MHz ARM Cortex M33** and **128MHz RISC-V coprocessor**, supported by 1.5 MB non-volatile memory and 256 KB RAM, the BL54L15µ modules offer double the processing power (vs prior BL654 – nRF52840). The BL54L15µ series brings out all nRF54L15 hardware features and capabilities including up to **+8 dBm** transmit power, **1.7V – 3.5V** supply considerations, and **NFC A-Tag** implementation.

It's further enhanced with state-of-the-art security and is designed for PSA Certified level 3. It supports services such as Secure Boot, Secure Firmware Update, Secure Storage plus protection from physical attacks.

Note: BL54L15µ hardware provides all functionality of the nRF54L15 chipset used in the module design. This is a hardware datasheet only – it does not cover the software aspects of the BL54L15µ. This is to acknowledge that information in this datasheet is referenced from the nRF54L15 datasheet.

1.1 Features and Benefits

- **Nordic nRF54L15** – 2.4 x 2.25mm WSCLP with 32 GPIOs utilized.
- **Multi-protocol support:** Bluetooth LE Core 6.0, 802.15.4 (Thread/Matter)
- **Cortex M33** processor core: 128 MHz ARM Cortex M33
- **RISC-V** co-processor core: 128 MHz VPR
- **Memory:** 1.5MB non-volatile memory, 256 KB RAM
- **High Speed Peripherals**: - HS-SPI/UART, software defined peripherals on 128 MHz VPR, GPIO - 1x 64 MHz Port, 1.7 – 3.5V, 11 GPIOs
- **Low Leakage Peripherals:** 2x QDEC, 7x Timer, Global RTC, 2x WDT, NFC A-Tag, TEMP, I2S, COMP, 3x PWM, LPCOMP, 14-bit 8CH ADC, 5x TWI/SPI/UART, GPIO (2x 16 MHz Port (P0, P1), 20 GPIO's, 1.7-3.6V, 32 GPIO)
- **Antenna choice** – integrated pre-certified **Chip antenna** or external antenna support via **Trace Pad**
- **Ultra-small footprint** (6.3 mm x 7.9 mm x 1.75 mm)
- **Extended** Industrial **Temperature Rating** (-40° to +105 °C)
- **Development choice:** Zephyr RTOS, Nordic nRF Connect SDK & Canvas
- **Bluetooth LE**: Peripheral/Central, 2 Mbps (high throughput), LE Coded (long range), AoA/AoD, Mesh
- Firmware Over the Air **(FOTA)** via MCUboot and Zephyr
- **Hostless operation** – Multi Core MCU reduces BOM
- **Fully featured development kits** to jump start Bluetooth LE development

1.2 Application Areas

- Building Automation
- Security
- Medical Peripherals
- Industrial Sensors

2 Specification

2.1 Specification Summary

Categories/Feature	Implementation
Wireless Specification	
Bluetooth®	Bluetooth 6.0 – Single mode • GATT client/server – Any adopted/custom services • Central/Peripheral roles • Bluetooth LE mesh • 2M PHY • LE Coded PHY • LE Advertising Extensions • LE secure connections • Data packet length extensions • LE privacy v1.2 • LE ping • DTM Firmware (Test Modes)
IEEE 802.15.4-2020 PHY	2405–2480 MHz IEEE 802.15.4-2006 radio transceiver, implementing IEEE 802.15.4-2006 compliant • 250kbps, 2450MHz, O-QPSK PHY • Channels 11-26. Channel 11 2405MHz and CH26 2480MHz. • Clear channel assessment (CCA) • Energy detection (ED) scan • CRC generation
Nordic proprietary 1Mbps, 2Mbps, 4Mbps modes radio	2402–2480 MHz Nordic proprietary 1Mbps and 2Mbps modes radio transceiver • 1Mbps nRF proprietary mode (ideal transmitter) • 2Mbps nRF proprietary mode (ideal transmitter) • 4Mbps nRF proprietary mode (ideal transmitter)
Frequency	2.402 - 2.480 GHz for BLE (CH0 to CH39) 2.405 - 2.480 GHz for IEEE 802.15.4-2006 PHY (CH11 to CH26)
Raw Data Rates	1 Mbps BLE (over-the-air) 2 Mbps BLE (over-the-air) 125 kbps BLE (over-the-air) 500 kbps BLE (over-the-air) 250 kbps IEEE 802.15.4 802.15.4-2006 (over-the-air) Nordic proprietary 1Mbps, 2Mbps and 4Mbps modes (over-the-air)
Maximum Transmit Power Setting	+8 dBm Conducted 453-00001 (Integrated antenna) (Exclude antenna gain) +8 dBm Conducted 453-00044 (External antenna) (Test at MHF4 connector)
Minimum Transmit Power Setting	-40dBm
Receive Sensitivity[1] (≤37byte packet for BLE)	BLE 1 Mbps (BER=1E-3) -95dBm typical BLE 2 Mbps -92dBm typical BLE 125 kbps -103dBm typical BLE 500 kbps -98.5dBm typical IEEE 802.15.4-2006 250kbps TBD dBm typical
Link Budget (conducted)	102 dB @ BLE 1 Mbps (TX power used is 7dBm) 110 dB @ BLE 125 kbps (TX power used is 7dBm)

Note1 Known Noise on channels 2432MHz and 2464MHz degrades receiver sensitivity, in which sensitivity are not within the typical value

NFC	
NFC-Type A Listen mode compliant	**Based on NFC forum specification:** 13.56 MHz, Date rate 106 kbps, NFC Type2 and Type 4 emulation **Modes of Operation:** Disable, Sense, Activated **Use Cases:** Touch-to-Pair with NFC, NFC enabled Out-of-Band Pairing
Security	Designed for PSA Certified Level 3 with Secure Boot, Secure Firmware Update, and Secure Storage. Integrated tamper sensors detect attacks and take action, and cryptographic accelerators are hardened against side-channel attacks.

Host Interfaces and Peripherals	**Applications Core (High Performance)**	**Software defined peripheral Core (ultra-low power)**
Total	32 x multifunction I/O lines	
Two co-processors	Arm Cortex-M33 with DSP, FPU, TrustZone support. 1524KB non-voltaile RRAM 256KB RAM L1 cache 128MHz clock Uses voltage and clock frequency scaling	RISC-V CPU (VPR) fast lightweight peripheral processor (FLPR) dedicated for software defined peripherals 16MHz clock
GPIO	Up to 32 multifunction GPIO's	
	64MHz 1.7-3.5V GPIO port P2.00-P2.10	16MHz 1.7-3.5V GPIO port P1.00-P1.15; P0.00-P0.04
ADC (14-bit)	14-bit 20KS/s with oversampling 12-bit 250KS/s 10-bit 2MS/s AIN0-AIN7 pins up to 8 programmable gain channels	
Global RTC (GRTC)		Implements full real time clock and calendar as shared system time. Can run in System OFF mode. Ultra low power, 1us resolution, 52bits wide, uses 16MHz clock, 32.76kHz when other power modes.
RTC		2x low power runs off LFCLK
High Speed SPI/UART	1 x	
SPI/UART/TWI		4x
PWM		3x 4channel PWM
I2S		1x I2S (Inter-IC sound interface)
PDM		1x PDM (Pulse code modulation interface) for digital microphones
TIMER		7x Timer (32bit)
QDEC		2x QDEC (Quadrature decoder)
COMP		1x COMP (comparator)
LPCOMP		1x LPCOMP (low power comparator)
TEMP		1x Temperature sensor Temperature range equal to operating temperature range
WDT		2x WDT (Watchdog timer)

Host Interfaces and Peripherals	Applications Core (High Performance)	Software defined peripheral Core (ultra-low power)
NFC A-Tag		1x
Wakeup pins		21
External optional 32.768 kHz crystal		Not needed for normal radio operation. Optionally, connect +/-20ppm accuracy crystal for more accurate protocol timing. Fit associated load capacitor for crystal or use nRF54L15 internal load capacitor, which is configurable as 4 pF to 18 pF in 0.5pF steps on pins XL1, XL2.
Security	Designed for PSA Certified Level 3 with Secure Boot, Secure Firmware Update, and Secure Storage. Integrated tamper sensors detect attacks and take action, and cryptographic accelerators are hardened against side-channel attacks.	

Zephyr RTOS	**Via SWD (JTAG) 2 wire interface**	
Programmability Options	**Nordic nRFConnect SDK:** Software/Support available from Nordic directly https://devzone.nordicsemi.com/ **Zephyr RTOS:** Software/Support available from https://www.zephyrproject.org/ **Canvas SW Suite**: Software/ Support available from https://www.ezurio.com/canvas/software-suite	
FW upgrade	Via SWD (JTAG) 2 wire interface or UART	
Supply Voltage	1.7V-3.5V	
Power Consumption		
Active Modes Peak Current (for maximum Tx power +8dBm) – Radio only	29 mA peak Tx@ 1.8V, LE1M 23 mA peak Tx@ 1.8V, CW 16 mA peak Tx@ 3.3V, LE1M 13 mA peak Tx@ 3.3V, CW	
Active Modes Peak Current (for Tx power -40dBm) – Radio only	9 mA peak Tx @ 1.8V, LE1M 6.5 mA peak Tx @ 1.8V, CW 6 mA peak Tx @ 3.3V, LE1M 5 mA peak Tx @ 3.3V, CW	
Ultra-low Power Modes	System ON Idle	3 uA (System ON IDLE with GRTC (XOSC) and 256 KB RAM)
	System OFF	0.6 uA
Antenna Options		
Internal	Chip antenna – on-board (**453-00223 variant)**	
External	Connection via *off module* IPEX MHF4 (**453-00224 RF trace pin variant)**	
Physical		
Dimensions	7.9mm x 6.3mm x 1.75mm Pad Pitch – 0.65 mm Pad Type – Two rows of pads (LGA - Land Grid Array).	
Weight	<1 gram	
Environmental		
Operating	-40 ˚C to +105 ˚C	
Storage	-40 ˚C to +105 ˚C	
Miscellaneous		
Lead Free	Lead-free and RoHS compliant	
Warranty	One-Year Warranty	
Development Tools		
Development Kit	Development kit per module SKU (453-00223-K1 and 453-00224-K1 respectively)	
Development Tools	Nordic nRFConnect - Android and iOS applications UART firmware upgrade Tools and utilities	Xbit
Bluetooth®	Full Bluetooth SIG Declaration ID	
FCC/ISED/CE/MIC/RCM/UKCA	All BL54L15µ Series	

3 Hardware Specifications

3.1 Block Diagram and Pin-out

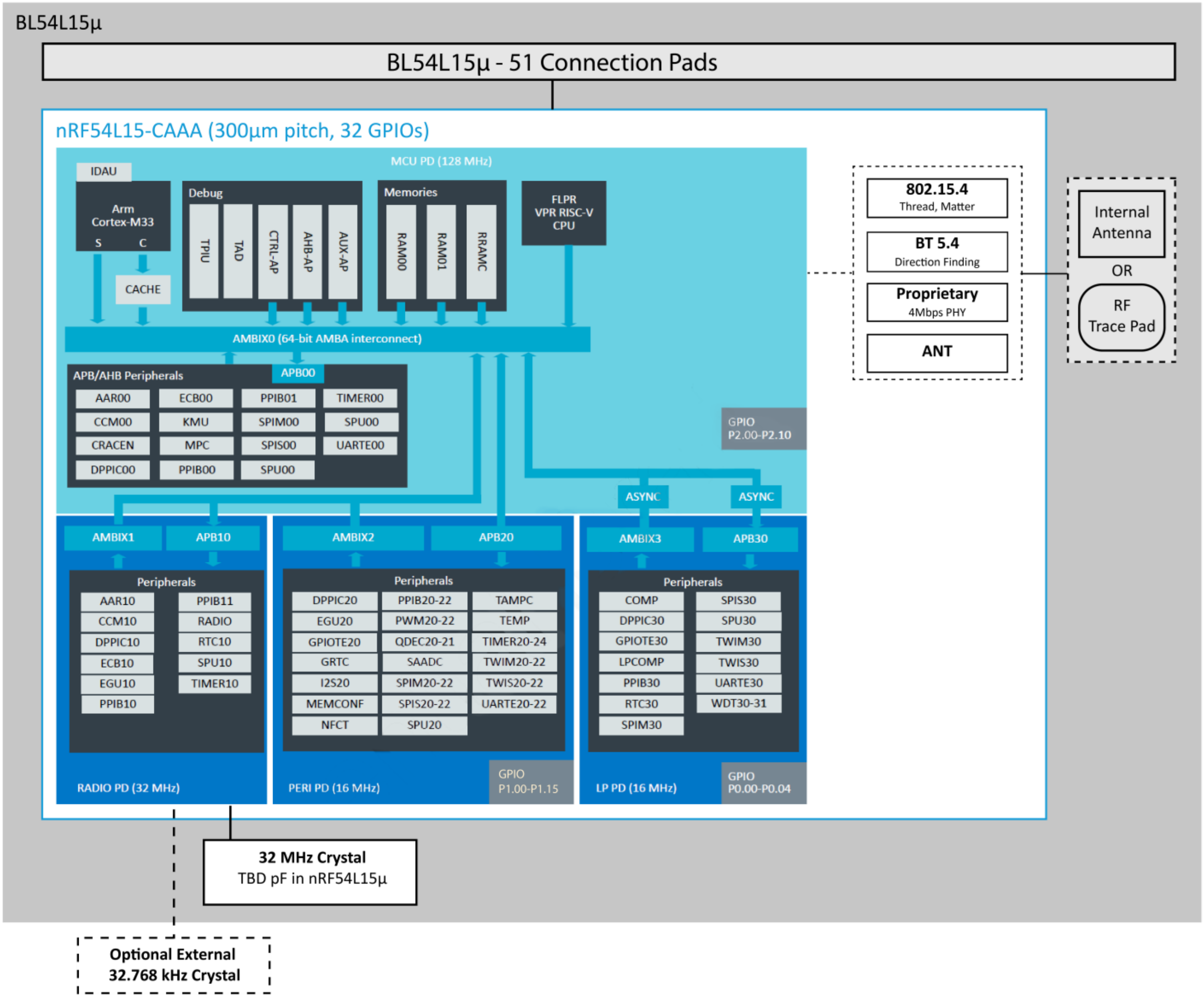


Figure 1: BL54L15µ HW block diagram

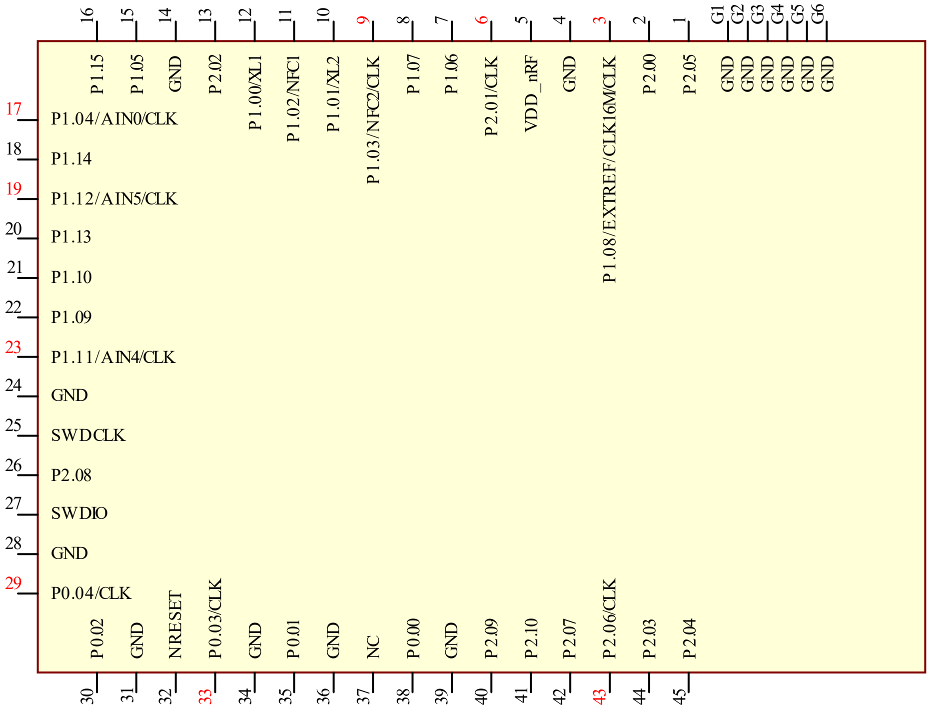


Figure 2: Top view - Schematic symbol for 453-00223 BL54L15µ Module (Nordic nRF54L15-CAAA) – Chip Antenna variant

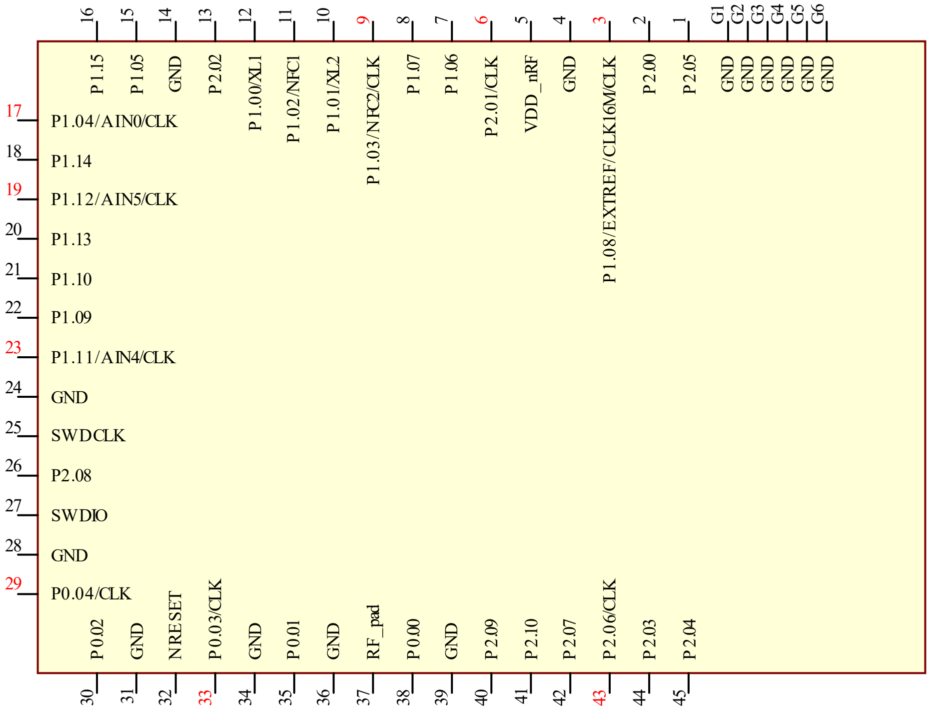


Figure 3: Top view - Schematic symbol for 453-00224 BL54L15µ Module (Nordic nRF54L15-CAAA) – RF Trace pin variant

3.2 Pin Definitions

Table 1: Pin definitions

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15-CAAA 300um WLCSP, 32 GPIOs	nRF54L15-CAAA 300u pitch WLCSP, 32GPIOs Name	Description	Example usage
1	P2.05	G5	P2.05	General purpose I/O SPIM CS SPIS CS UARTE RTS FLPR.5 QSPI CS	SPIM00/20 SPIS00/20 UARTE00/20 FLPR FLPR (QSPI)
2	P2.00	G6	P2.00	General purpose I/O SPIM DCX UARTE RXD FLPR.4 QSPI D3	SPIM00/20 UARTE00/20 FLPR FLPR (QSPI)
3	P1.08/GRTCHFOUT/EXTREF	F7	P1.08 EXTREF	General purpose I/O GRTC CLKOUTFAST External reference for SAADC	Clock pin
4	GND		VSS		
5	VDD_nRF	G3	VDD	1.7V-3.5V, connect external supply of 1.7V-3.5V to pin5(VDD_nRF)	
6	P2.01	G7	P2.01	General purpose I/O SPIM SCK SPIS SCK FLPR.0 QSPI SCK	Clock pin SPIM00/20 SPIS00/20 FLPR FLPR (QSPI)
7	P1.06/ASO[1]/AIN2	D7	P1.06 ASO[1] AIN2	General purpose I/O TAMPC active shield 1 output Analog input	TAMPC
8	P1.07/ASI[1]/AIN3	E7	P1.07 ASI[1] AIN3	General purpose I/O TAMPC active shield 1 input Analog input	TAMPC
9	P1.03/NFC2	D5	P1.03 NFC2	General purpose I/O NFC antenna connection	Clock pin
10	P1.01/XL2	C6	P1.01 XL2	General purpose I/O Connection for 32.768 kHz crystal	Ezurio Devkit: Optional 32.768kHz crystal pad XL2, XL1 and associated built-in configurable internal capacitors inside nRF54L15-CAAA chipset.
11	P1.02/NFC1	C7	P1.02 NFC1	General purpose I/O NFC antenna connection	

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15-CAAA 300um WLCSP, 32 GPIOs	nRF54L15-CAAA 300u pitch WLCSP, 32GPIOs Name	Description	Example usage
12	P1.00/XL1	C5	P1.00 XL1	General purpose I/O Connection for 32.768 kHz crystal	Ezurio Devkit: Optional 32.768kHz crystal pad XL2, XL1 and associated built-in configurable internal capacitors inside nRF54L15-CAAA chipset.
13	P2.02/SWO	F6	P2.02	General purpose I/O SPIM SDO SPIS SDO UARTE TXD FLPR.1 QSPI D0 Serial wire output (SWO)	 SPIM00/20 SPIS00/20 UARTE00/20 FLPR FLPR (QSPI) Trace
14	GND		VSS		
15	P1.05/ASI[0]/AIN1	E6	P1.05 ASI[0] RADIO[6] AIN1	General purpose I/O TAMPC active shield 0 input RADIO DFEGPIO Analog input	TAMPC RADIO
16	P1.15	B6	P1.15	General purpose I/O	
17	P1.04/ASO[0]/AIN0	D6	P1.04 ASO[0] AIN0	General purpose I/O TAMPC active shield 0 output Analog input	Clock pin TAMPC
18	P1.14/RADIO[5]/AIN7	B5	P1.14 RADIO[5] AIN7	General purpose I/O RADIO DFEGPIO Analog input	RADIO
19	P1.12/ASI[3]/RADIO[3]/AIN5 Please see note 7	A3	P1.12 ASI[3] RADIO[3] AIN5	General purpose I/O TAMPC active shield 3 input RADIO DFEGPIO Analog input	Clock pin TAMPC RADIO
20	P1.13/RADIO[4]/AIN6	B4	P1.13 RADIO[4] AIN6	General purpose I/O RADIO DFEGPIO Analog input	RADIO
21	P1.10/ASI[2]/RADIO[1] Please see note 7	C3	P1.10 ASI[2] RADIO[1]	General purpose I/O TAMPC active shield 2 input RADIO DFEGPIO	TAMPC RADIO
22	P1.09/ASO[2]/RADIO[0] Please see note 7	B3	P1.09 ASO[2] RADIO[0]	General purpose I/O TAMPC active shield 2 output RADIO DFEGPIO	TAMPC RADIO

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15-CAAA 300um WLCSP, 32 GPIOs	nRF54L15-CAAA 300u pitch WLCSP, 32GPIOs Name	Description	Example usage
23	P1.11/ASO[3]/RADIO[2]/AIN4 Please see note 7	C4	P1.11 ASO[3] RADIO[2] AIN4	General purpose I/O TAMPC active shield 3 output RADIO DFEGPIO Analog input	Clock pin TAMPC RADIO
24	GND	-	VSS		
25	SWDCLK	E3	SWDCLK	Serial Wire Debug clock input with on-chip pull-up for debug and programming	
26	P2.08/TRACEDATA[1]	D4	P2.08 TRACEDATA[1]	General purpose I/O FLPR.8 Trace data SPIM SDO SPIS SDO UARTE TXD	FLPR Trace SPIM00/21 SPIS00/21 UARTE00/21
27	SWDIO	F2	SWDIO	Serial Wire Debug IO withstandard-drive and on-chip pull-down for debug and programming	
28	GND	-	VSS		
29	P0.04/GRTCLFCLKOUT	D3	P0.04	General purpose I/O GRTC CLKOUT32K	Clock pin GRTC
30	P0.02	E2	P0.02	General purpose I/O	
31	GND	-	VSS		
32	nRESET	D2	nRESET	Pin RESET with internal pull-up resistor (13k Ohms). System Reset (Active Low).	
33	P0.03/GRTCPWM	E1	P0.03	General purpose I/O GRTC PWM	Clock pin GRTC
34	GND	-	VSS		
35	P0.01	F1	P0.01	General purpose I/O	
36	GND	-	VSS		
37	RF_pad or NC	D1	ANT	Single ended radio antenna connection	RF pad active on BL54L15µ RF pin variant 453-00224. NC on BL54L15µ Integrated antenna variant 453- 00223.
38	P0.00	G1	P0.00	General purpose I/O	
39	GND	-	VSS		
40	P2.09/TRACEDATA[2]	F3	P2.09 TRACEDATA[2]	General purpose I/O FLPR.9 Trace data SPIM SDI SPIS SDI UARTE CTS	FLPR Trace SPIM00/21 SPIS00/21 UARTE00/21

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15-CAAA 300um WLCSP, 32 GPIOs	nRF54L15-CAAA 300u pitch WLCSP, 32GPIOs Name	Description	Example usage
41	P2.10/TRACEDATA[3]	G2	P2.10 TRACEDATA[3]	General purpose I/O FLPR.10 Trace data SPIM CS SPIS CS UARTE RTS	FLPR Trace SPIM00/21 SPIS00/21 UARTE00/21
42	P2.07/TRACEDATA[0]/SWO	E4	P2.07 TRACEDATA[0] SWO	General purpose I/O FLPR.7 Trace data Serial wire output (SWO) SPIM DCX UARTE RXD	FLPR Trace Trace SPIM00/21 UARTE00/21
43	P2.06/TRACECLK	F4	P2.06 TRACECLK	General purpose I/O FLPR.6 SPIM SCK SPIS SCK Trace clock	Clock pin FLPR SPIM00/21 SPIS00/21 Trace
44	P2.03	E5	P2.03	General purpose I/O FLPR.3 QSPI D2	FLPR FLPR (QSPI)
45	P2.04	F5	P2.04	General purpose I/O SPIM SDI SPIS SDI UARTE CTS FLPR.2 QSPI D1	SPIM00/20 SPIS00/20 UARTE00/20 FLPR FLPR (QSPI)
G1	GND	-	VSS		
G2	GND	-	VSS		
G3	GND	-	VSS		
G4	GND	-	VSS		
G5	GND	-	VSS		
G6	GND	-	VSS		

Pin Definition Notes:

Note 1 GPIO	**GPIO = General Input or Output (GPIO level voltage tracks VDD pin). AIN =Analog input.** If GPIO is selected as an input, ensure the input is not floating (which can cause current consumption to drive with time in low power modes (such as System ON Idle), by selecting the internal pull up or pull down. **Must connect all GND pads to host board PCB GND plane.**
Note2 Clock for serial interfaces or trace	Some peripherals (SPI, TWI, PDM, I2S, TRACE, GRTC) have clock signals. Dedicated clock pins have been optimized to ensure correct timing relationship between clock and data signal for these peripherals. Pins that can be used as clock signals are shown with pin name in red colour. The peripheral data signal must be configured to use pins close to the clock pin. This ensures that the internal paths from the peripheral to the pin have the same delay, so that the data and clock signals reach the pins at the same time. For high-speed signals, the printed circuit board (PCB) layout must use short PCB traces of identical length. This makes sure any delays are kept to a minimum and it assures close to identical delay and clock path.

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15-CAAA 300um WLCSP, 32 GPIOs	nRF54L15-CAAA 300u pitch WLCSP, 32GPIOs Name	Description	Example usage
Note 3 **Dedicated pins**	UARTE20/21: Can use any pin on GPIO port P1. Can be connected across power domains to dedicated pin on P2. SPIM00: Has dedicated pins on GPIO port P2. For 32MHz operation, the pins must be configured using extra high drive E0/E1 configuration. SPIM20/21: Can use any pin on GPIO port P1. Can be connected across power domains to dedicated pin on P2. SPIS20/21: Can use any pin on GPIO port P1. Can be connected across power domains to dedicated pin on P2. TRACE: Has dedicated pins on GPIO port P2. For 32MHz operation, the pins must be configured using extra high drive E0/E1 configuration. GRTC: Has dedicated pins for clock and PWM output. TAMPC: Has dedicated pins for active shield inputs and outputs. FLPR: Uses dedicated pins on GPIO port P2 for emulated peripherals such as QSPI. RADIO: Uses dedicated pins on GPIO port P1 for antenna switch control (DFEGPIO for direction finding). NFC: Uses dedicated pin listed in pin definitions table1.				
Note 4 **SWDIO / SWCLK / nRESET / VDD / GND**	Customer MUST bring out SWDIO, SWCLK, nRESET, VDD, GND for programming purposes.				
Note 5 **GPIO P2.15**	P1.15 GPIO is only available on the BL54L15µ which uses nRF54-CAAA(300um pitch) which as 32 GPIO's.				
Note 6 **RF_PAD**	RF_pad (pin37) is for the BL54L15µ RF pad variant (453-00224) module only. If using the BL54L15µ module RF pad variant (453-00224), customer MUST copy the 50-Ohms GCPW RF track design, detailed in 50-Ohms RF Trace on Host PCB for BL54L15µ RF pad variant (453-00224)				
Note 7	If GPIOs P1.09, P1.10, P1.11, and P1.12 are used, please apply the following operations. • Add a 330 Ω or larger series resistance directly after the tracks enter the outer layer of the PCB. • Keep PCB tracks as short as possible and in between ground layers if possible. • Use toggling speed lower than 1 MHz If unused, leave these pins unconnected.				

3.3 Electrical Specifications

3.3.1 Absolute Maximum Ratings

Absolute maximum ratings are the extreme limits for supply voltage and voltages on digital and analogue pins of the module are listed below; exceeding these values causes permanent damage.

Table 2: Absolute maximum ratings

Parameter	Min	Max	Unit
Supply Voltages			
VDD_nRF	-0.3	3.6	V
I/O pin voltage			
Voltage at GPIO pin (at VDD≤3.5V)	-0.3	VDD_nRF + 0.3	V
Voltage at GPIO pin (at VDD>3.5V)		3.6	V
NFC antenna pin current (NFC1/2)	-	130	mA
Environmental			
Storage temperature	-40	+105	°C
MSL (Moisture Sensitivity Level)	-	4	-
ESD (as per EN301-489)			
Conductive		4	kV
Air Coupling		8	kV
Flash Memory (Endurance) (Note 2)	10,000		Write/erase cycles
Flash Memory (Retention)	10 years at 85°C 2 years at 105°C		years at TBD °C

Absolute maximum Ratings Notes:	
Note 1	The absolute maximum rating for VDD pin (max) is 3.6 V for the BL54L15µ.
Note 2	Wear levelling can be implemented by customer.

3.3.2 Recommended Operating Parameters

Table 3: Power supply operating parameters

Parameter	Min	Typ	Max	Unit
VDD_nRF (independent of DCDC) supply range	1.7		3.5	V
VDD_nRF$_{ext}$ (**VDD_nRF** supply voltage under extended operating temperature)	1.7		3.3	V
VDD_nRF Maximum ripple or noise (See Note 1)	-	-	10	mV
Operating Temperature Range	-40	+25	+85	°C
Extended operating temperature	85		105	°C

Recommended Operating Parameters Notes:	
Note 1	This is the maximum VDD_nRF ripple or noise (at any frequency) that does not disturb the radio.
Note 2	The on-board power-on reset circuitry may not function properly for rise times longer than the specified maximum.
Note 3	BL54L15µ power supply: Connect external supply voltage (within range 1.7V-3.5V) to VDD_nRF pin. Please note an additional parameter for the extended operating temperature condition is provided.

3.4 Clocks

3.4.1 HFXO - 32MHz crystal oscillator and nRF54L15 internal load capacitor setting

The BL54L15µ module contains the 32 MHz crystal, but the load capacitors to create 32MHz crystal oscillator circuit are inside the nRF54L15 chipset. Customer MUST set the internal nRF54L15 capacitors from 4 pF to 17 pF in 0.25pF if needed or use default value without changing.

The 32 MHz crystal inside the BL54L15µ module is a high accuracy crystal (±15 ppm at room temperature) that helps with radio operation and reducing power consumption in the active modes.

3.4.2 LFCLK – Low Frequency clock source

There are four possibilities (see figure 5) for the low frequency clock (LFCLK) and options are:

LFRC (32.768kHz RC oscillator): The Internal 32.768 kHz RC oscillator (LFRC) is fully embedded in nRF54L15 (and does not require additional external components) with an accuracy ±250 ppm (after calibration of LFRC at least every eight seconds using the HFXO as a reference oscillator).

LFXO (32.768kHz crystal oscillator): For higher LFCLK accuracy (greater than ±250ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used. To use LFXO, a 32.768kHz crystal must be connected between the XL1 and XL2 pins and the load capacitance between each crustal terminal and ground. Optionally internal (to nRF54L15) capacitor of maximum 18pF in 0.5pF steps are provided on pins XL1 and XL2.

Low frequency (32.768 kHz) external source: The 32.768 kHz oscillator (LFXO) is designed to work with external sources

LFSYNTH (32.768kHz Synthesised clock) from HFCLK (LFSYNTH): The LFCLK can be synthesised from the HFCLK source. LFSYNTH depends on the HFCLK to run. The accuracy of the LFCLK clock with LFSYNTH as a source assumes the accuracy of the HFCLK. If high accuracy is required, the HFCLK must generated from the HFXO. Using the LFSYNT clock removes the requirement for an external 32.768kHz crystal but the increases the average power consumption as the HFCLK will turned on in the system.

3.4.3 Other Internal Clocks

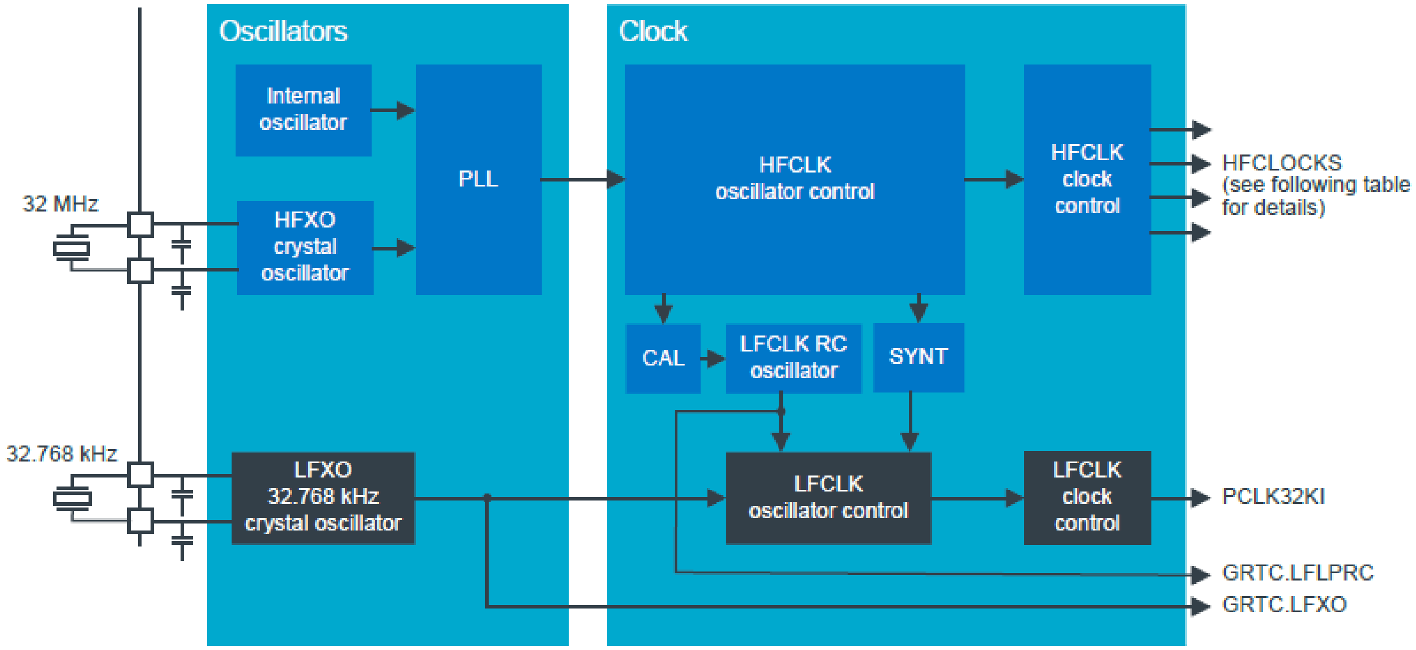


Figure 4: nRF54L15 Clock System Overview (adapted from Nordic)

3.5 BL54L15µ Power Supply

The BL54L15µ module power supply internally contains the following main supply regulator stage (Figure 5):

- VREGMAIN – Connected to the VDD_nRF pin

power supply mode is entered when the external supply voltage (1.7V-3.5V) is connected to VDD_nRF pin. See Figure 5.

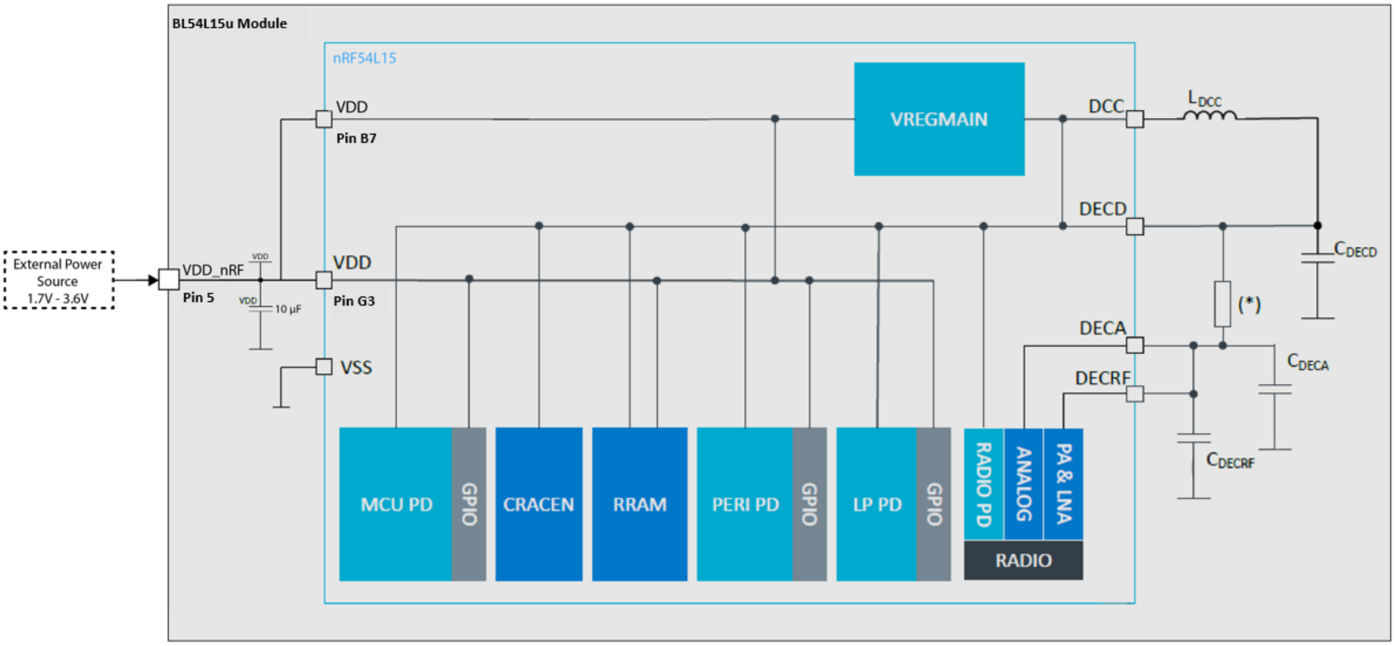


Figure 5: BL54L15µ power supply block diagram (adapted from Nordic)

4 Mandatory SW requirements related to hardware

4.1 32MHz crystal internal load capacitor setting

MANDATORY. BL54L15µ module contains the 32 MHz crystal but the load capacitors to create 32 MHz crystal oscillator circuit are inside the nRF54L15-CAAA chipset. Customer MUST set the internal nRF54L15 capacitors to from 4 pF to 17 pF in 0.25pF if needed, or use default value without changing.

5 Hardware Integration Suggestions

5.1 Circuit

The BL54L15µ is easy to integrate, requiring one mandatory external 10uF capacitor on customers board and apart from that those components which customer require for development and in your end application.

The following are suggestions for your design for the best performance and functionality.

Checklist (for Schematic):

- **BL54L15µ power supply:**
  External supply voltage (1.7V-3.5V) is connected to VDD_nRF pin(pin5).

  External power source should be within the operating range, rise time and noise/ripple specification of the BL54L15µ. Add decoupling capacitors for filtering the external source. Power-on reset circuitry within BL54L15µ series module incorporates brown-out detector, thus simplifying your power supply design. Upon application of power, the internal power-on reset ensures that the module starts correctly.
- **AIN (ADC) and GPIO pin IO voltage levels**
  BL54L15µ GPIO voltage levels are at VDD. Ensure input voltage levels into GPIO pins are at VDD also (if VDD source is a battery whose voltage drops). Ensure ADC pin maximum input voltage for damage is not violated.
- **AIN (ADC) impedance and external voltage divider setup**
  If you need to measure with ADC a voltage higher than 3.5V, you can connect a high impedance voltage divider to lower the voltage to the ADC input pin.
- **SWD**
  This is REQUIRED for loading firmware. MUST wire out the SWD two wire interface on host design. Five lines should be wired out, namely SWDIO, SWDCLK, nRESET, GND and VDD.
- **UART and flow control (CTS, RTS)**
  Required if customer requires UART.
- **TWI (I2C)**
  It is essential to remember that pull-up resistors on both SCL and SDA lines are required, the value as per I2C standard. BL54L15µ (nRF54L15-CAAA) can provide 13K Ohms typical pull up values internally. For other values, fit external pull-up resistor on both SCL and SDA as per I2C specification to set speed. The I2C specification allows a line capacitance of 400pF.
- **QSPI, High Speed SPI, High speed TWI (I2C, 1Mbps) and Trace**
  High-Speed SPI, TWI and Trace come on dedicated GPIO pins only. Other lower speed SPI and TWI can come out on any GPIO pins.

  For all high-speed signal, the printed circuit board (PCB) layout must ensure that connections are made using short PCB traces.
- **GPIO pins**
  If GPIO is selected as an input, ensure the input is not floating (which can cause current consumption to drive with time in low power modes (such as System ON Idle), by selecting the internal pull up or pull down.
- **NFC antenna connector** To make use of the Ezurio flexi-PCB NFC antenna (part # 0600-00061), fit connector:
  - Description – FFC/FPC Connector, Right Angle, SMD/90d, Dual Contact,1.2 mm Mated Height
  - Manufacturer – Molex
  - Manufacturers Part number – 512810594

  Add tuning capacitors of 300 pF on NFC1 pin to GND and 300 pF on NFC2 pins to GND if the PCB track length is similar as development board.
- **nRESET pin (active low)**
  Hardware reset. Wire out to push button or drive by host.
  By default module is out of reset when power applied to VDD pins (13K pull-up inside BL54L15µ (nRF54L15-CAAA)).
- **Optional External 32.768kHz crystal**
  If the optional external 32.768kHz crystal is needed, then use a crystal that meets specification and add load capacitors (either inside nRF541L15-CAAA or discrete capacitors outside BL54L15µ (nRF54L15-CAAA) whose values should be tuned to meet all specification for frequency and oscillation margin.
- **BL54L15µ module RF pad variant (453-00224)**
  RF_pad (pin37) is for the BL54L15µ RF pad variant (453-00224) module only. If using the BL54L15µ module RF pad variant (453-00224), customer MUST use 50-Ohms RF track design, detailed in the following section: 50-Ohms RF Trace on Host PCB for BL54L15µ RF pad variant (453-00224)

5.2 PCB Layout on Host PCB - General

Checklist (for PCB):

- MUST locate BL54L15µ module close to the edge of PCB (mandatory for the 453-00223 for on-board chip antenna to radiate properly).
- Use solid GND plane on inner layer (for best EMC and RF performance).
- All module GND pins MUST be connected to host PCB GND.
- Place GND vias close to module GND pads as possible.
- Unused PCB area on surface layer can flooded with copper but place GND vias regularly to connect the copper flood to the inner GND plane. If GND flood copper is on the bottom of the module, then connect it with GND vias to the inner GND plane.
- Route traces to avoid noise being picked up on VDD supply and AIN (analogue), GPIO (digital) traces and high-speed traces.
- Ensure no exposed copper is on the underside of the module (refer to land pattern of BL54L15µ development board).

5.3 PCB Layout on Host PCB for the 453-00223

5.3.1 Antenna Keep-out on Host PCB

The 453-00223 has an integrated chip antenna and its performance is sensitive to host PCB. It is critical to locate the 453-00223 on the edge of the host PCB (or corner) to allow the antenna to radiate properly. Refer to guidelines in section 6.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00223. Some of those guidelines repeated below.

- Ensure there is no copper in the antenna keep-out area on any layers of the host PCB. Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.
- For best antenna performance, place the 453-00223 module on the edge of the host PCB, preferably in the edge center.
- The BL54L15µ development board (453-00223-K1) has the 453-00223 module on the edge of the board (not in the corner). The antenna keep-out area is defined by the BL54L15µ development board which was used for module development and antenna performance evaluation shown in Figure 6, where the antenna keep-out area is 3mm wide, 5mm long; with PCB dielectric (no copper) height ~1.6mm sitting under the 453-00223 chip antenna module.
- The 453-00223 chip antenna is tuned when the 453-00223 is sitting on development board (host PCB) with size of 113mm x 63.5mm x1.6mm.
- A different host PCB thickness dielectric will have small effect on antenna.
- The antenna-keep-out defined in the 6.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00223 section.
- Host PCB land pattern and antenna keep-out for the BL54L15µ applies when the 453-00223 is placed in the edge of the host PCB preferably in the edge center. Figure 6 shows an example.

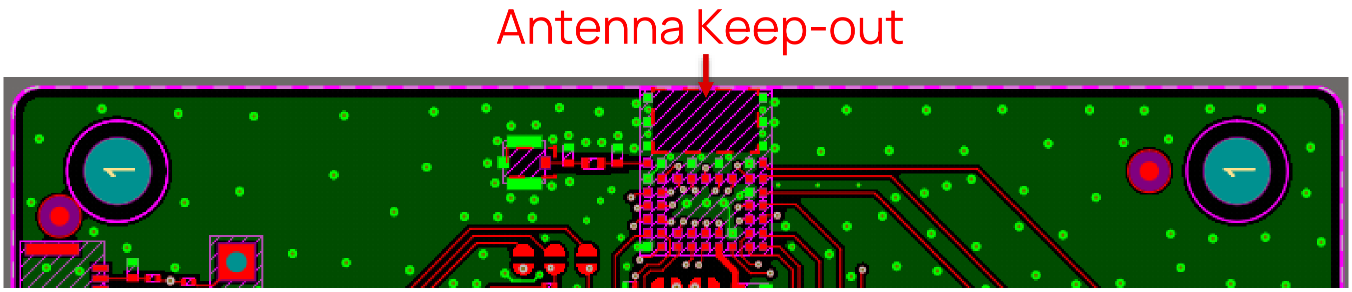


Figure 6: Chip Antenna keep-out area (shown in red) of the BL54L15µ development board for the 453-00223 module.

Antenna Keep-out Notes:	
Note 1	The BL54L15µ module is placed on the edge, preferably edge centre of the host PCB.
Note 2	Copper cut-away on all layers in the *Antenna Keep-out* area under the 453-00223 on host PCB.

5.3.2 Antenna Keep-out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40 mm top/bottom and 30 mm left or right.
- Metal close to the 453-00223 Chip antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. The amount of that degradation is entirely system dependent, meaning you will need to perform some testing with your host application.
- Any metal closer than 20 mm will begin to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that you test the range with a mock-up (or actual prototype) of the product to assess effects of enclosure height (and materials, whether metal or plastic) and host PCB ground (GND plane size).

5.4 50-Ohms RF Trace on Host PCB for BL54L15µ RF pad variant (453-00224)

To use an external antenna requires BL54L15µ module variant with RF trace pad (453-00224) and 50-Ohm RF trace from RF_pad (pin37) of the module (BL54L15µ 453-00054) to RF antenna connector (IPEX MHF4) on host PCB. On this RF path, BL54L15µ module GND pin36, pin39 and pin G1 used to support 50-Ohm RF trace.

Checklist for SCH

- Suggest fit RF connector IPEX MHF4 Receptacle (MPN: 20449-001E), https://www.i-pex.com/product/mhf-4-smt#!
- Suggest preserve pi network for tuning as shown below

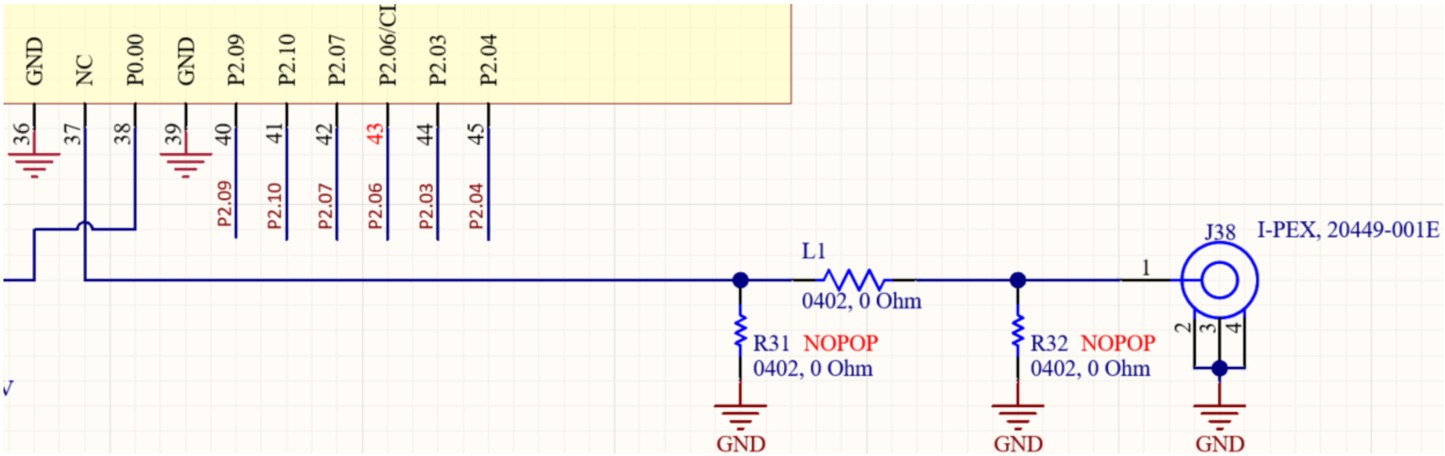
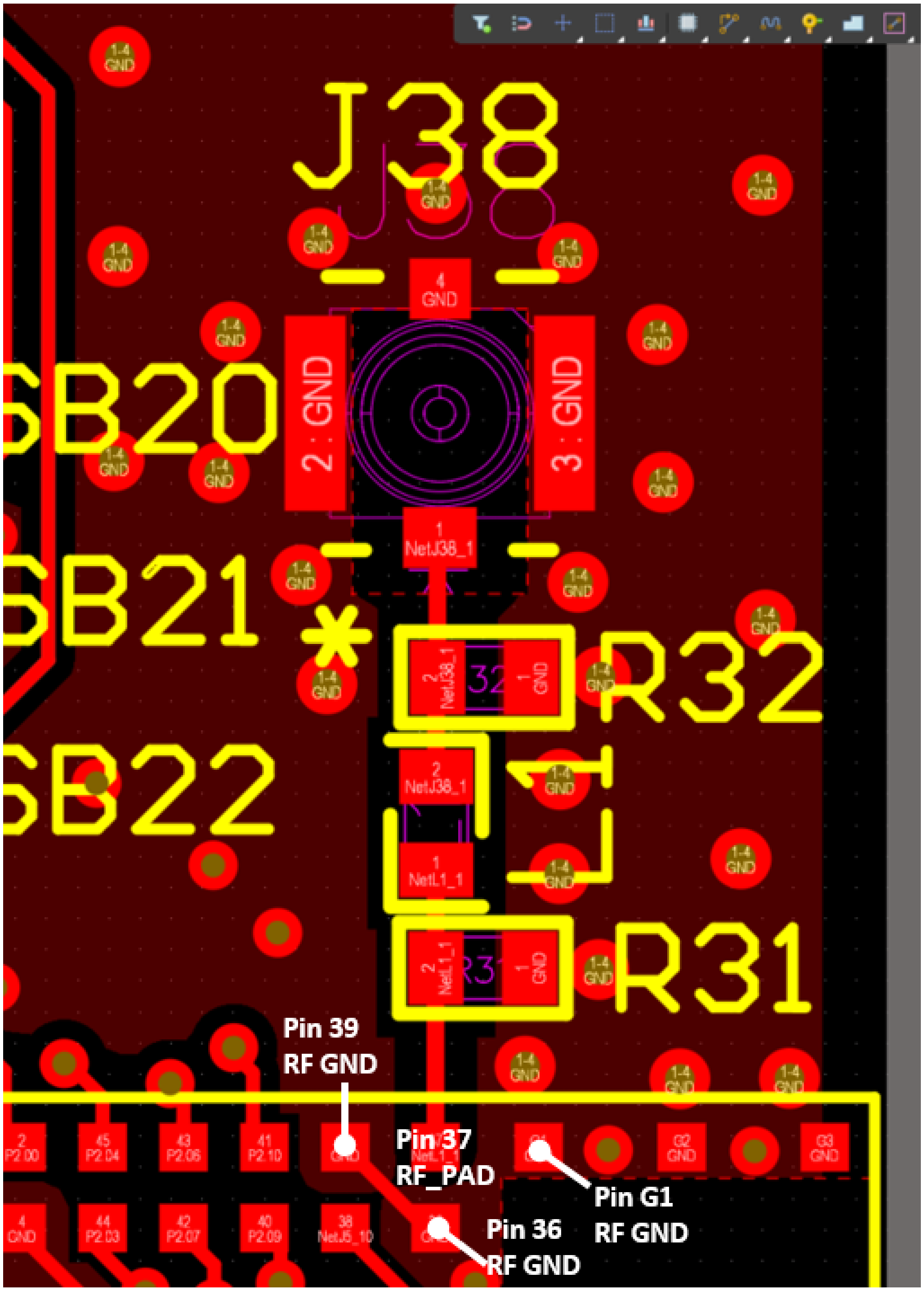


Figure 7: BL54L15µ RF trace pad variant (453-00224) Host PCB 50-Ohm RF trace schematic with pi network, RF connector

Layer1 (RF Track and RF GND)



Layer2 (RF GND) and Layer2 copper cut-out under RF connector

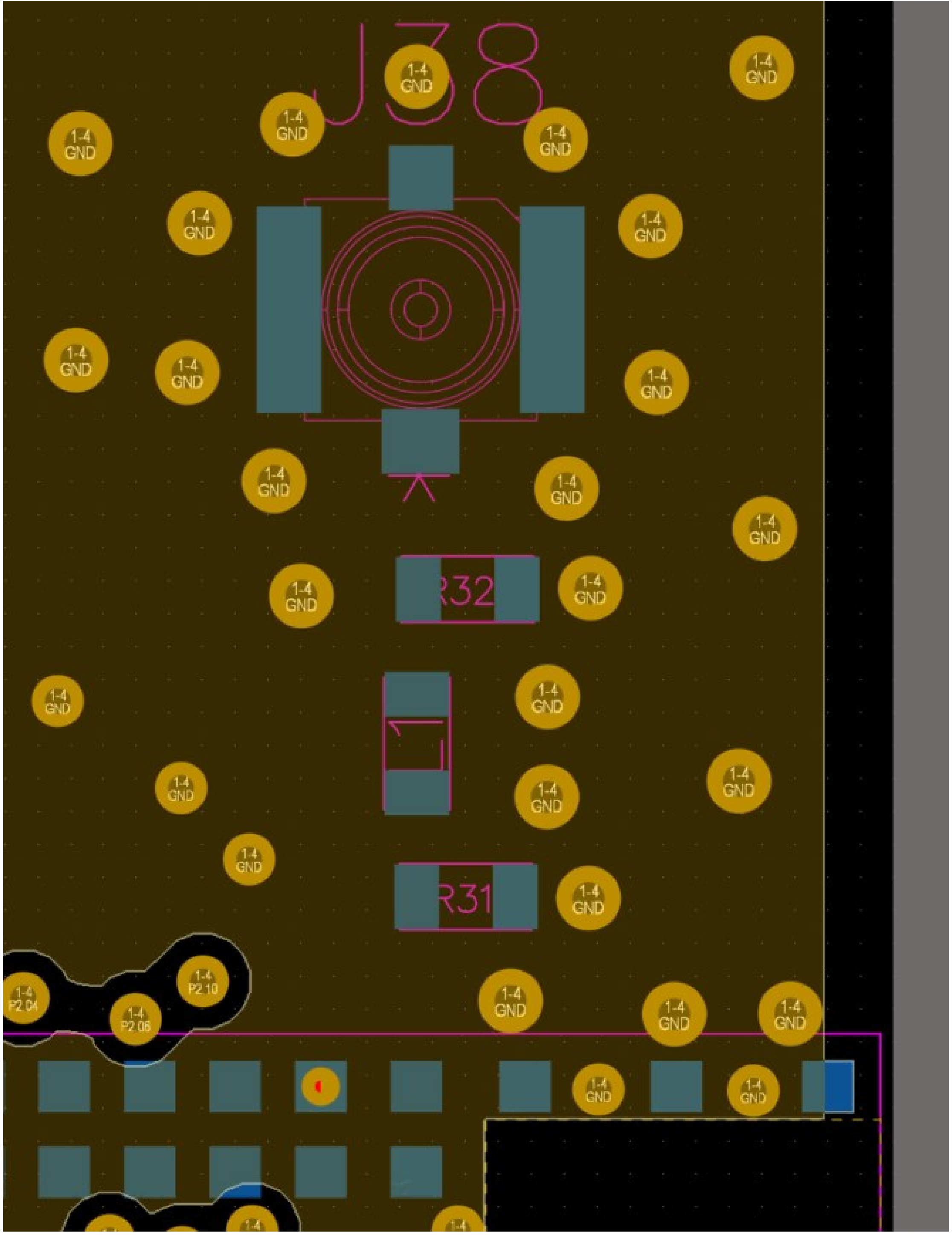
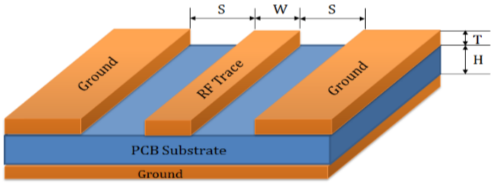


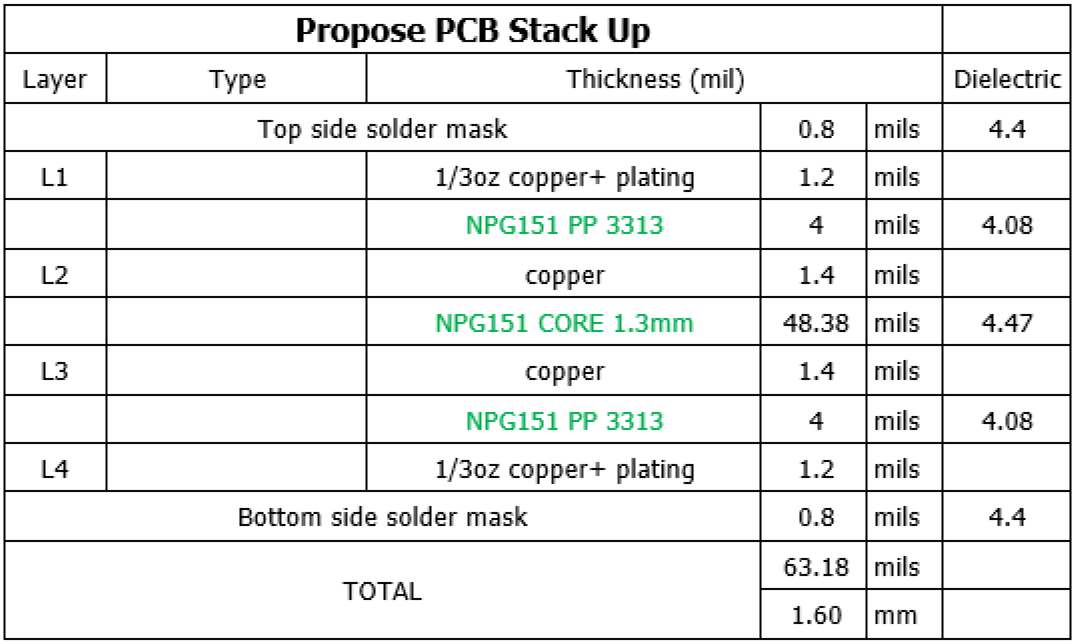
Figure 8: 50-Ohm RF trace design (Layer1 and Layer2) on BL54L15µ development board (or host PCB) for use with BL54L15µ RF trace pin variant (453-00224) module

Checklist for PCB:

▪ MUST use a 50-Ohm RF trace (GCPW, that is Grounded Coplanar Waveguide) from RF_pad (pin37) of the module (BL54L15µ 453-00224) to RF antenna connector (IPEX MHF4) on host PCB.

▪ To ensure regulatory compliance, MUST follow exactly the following considerations for 50-Ohms RF trace design and test verification:





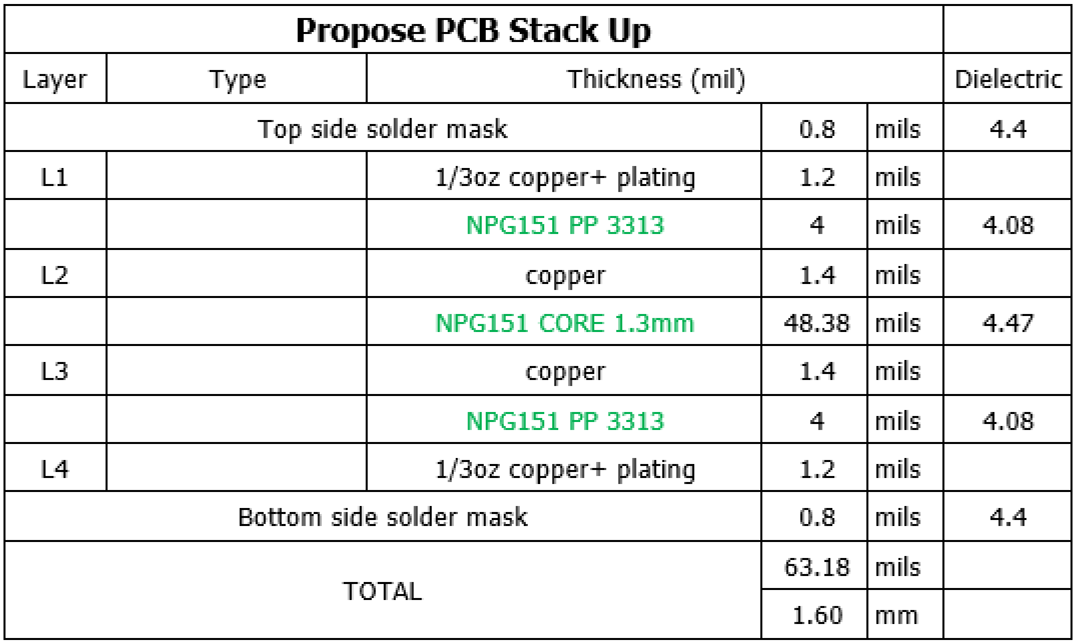
Propose PCB Stack Up					
Layer	Type	Thickness (mil)			Dielectric
Top side solder mask			0.8	mils	4.4
L1		1/3oz copper+ plating	1.2	mils	
		NPG151 PP 3313	4	mils	4.08
L2		copper	1.4	mils	
		NPG151 CORE 1.3mm	48.38	mils	4.47
L3		copper	1.4	mils	
		NPG151 PP 3313	4	mils	4.08
L4		1/3oz copper+ plating	1.2	mils	
Bottom side solder mask			0.8	mils	4.4
TOTAL			63.18	mils	
			1.60	mm	

Figure 9: BL54L15u development board PCB stack-up and L1 to L2 50-Ohms Grounded CPW RF trace design

Note 1: The plating (ENIG) above base 0.5 oz copper is not listed, but plating expected to be ENIG.

- The 50-Ohms RF trace design MUST be Grounded Coplanar Waveguide (GCPW) with
  - Layer1 RF track width (W) of 6.0 mil and
  - Layer1 gap (G) to GND of 10 mil and where the
  - Layer1 to Layer 2 dielectric thickness (H) MUST be 4 mil (dielectric constant Er 4.08).
  - Further the Layer1 base copper must be 0.33-ounce base copper (that is 0.46 mil) plus the plating
  - Layer1 MUST be covered by solder mask of 0.8 mil thickness (dielectric constant Er 4.4).

- The 50-Ohms RF trace design MUST follow the PCB stack-up shown in



Propose PCB Stack Up

Layer	Type	Thickness (mil)			Dielectric
Top side solder mask			0.8	mils	4.4
L1		1/3oz copper+ plating	1.2	mils	
		NPG151 PP 3313	4	mils	4.08
L2		copper	1.4	mils	
		NPG151 CORE 1.3mm	48.38	mils	4.47
L3		copper	1.4	mils	
		NPG151 PP 3313	4	mils	4.08
L4		1/3oz copper+ plating	1.2	mils	
Bottom side solder mask			0.8	mils	4.4
TOTAL			63.18	mils	
			1.60	mm	

- Figure 9. (Layer1 to Layer2 thickness MUST be identical to the BL5415u development board).
- The 50-Ohms RF track should be a controlled-impedance trace e.g., ±10%.
- Place GND vias regularly spaced either side of 50-Ohms RF trace to form GCPW (Grounded coplanar waveguide) transmission line as shown in Figure 8 and use BL54L15u module GND pin 36, pin 39 and pin G1.
- Use spectrum analyzer to confirm the radiated (and conducted) signal is within the certification limit.

5.5 External Antenna Integration with BL54L15µ RF trace pin variant (453-00224)

Please refer to the regulatory sections for FCC, ISED, CE, MIC, UKCA and RCM details of use of BL54L15µ with external antennas in each regulatory region.

The BL54L15µ family has been designed to operate with the below external antennas (with a maximum gain of 2.32 dBi). The required antenna impedance is 50 ohms. See Table 4. External antennas improve radiation efficiency.

Table 4: External antennas for the BL54L15µ RF trace pin variant (453-00224)

Manufacturer	Model	Ezurio Part Number	Type	Connector	Peak Gain 2400-2500 MHz	Peak Gain 2400-2480 MHz
Ezurio (Laird Connectivity)	NanoBlue	EBL2400A1-10MH4L	PCB Dipole	IPEX MHF4	2 dBi	-
Ezurio (Laird Connectivity)	FlexPIFA	001-0022	PIFA	IPEX MHF4	-	2 dBi
Mag.Layers	EDA-8709-2G4C1-B27-CY	0600-00057	Dipole	IPEX MHF4	2.32 dBi	-
Ezurio (Laird Connectivity)	mFlexPIFA	EFA2400A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	iFlexPIFA Mini	EFG2401A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	Ezurio NFC	0600-00061	NFC	N/A	-	-

6 Mechanical Details

6.1 BL54L15u Mechanical Details

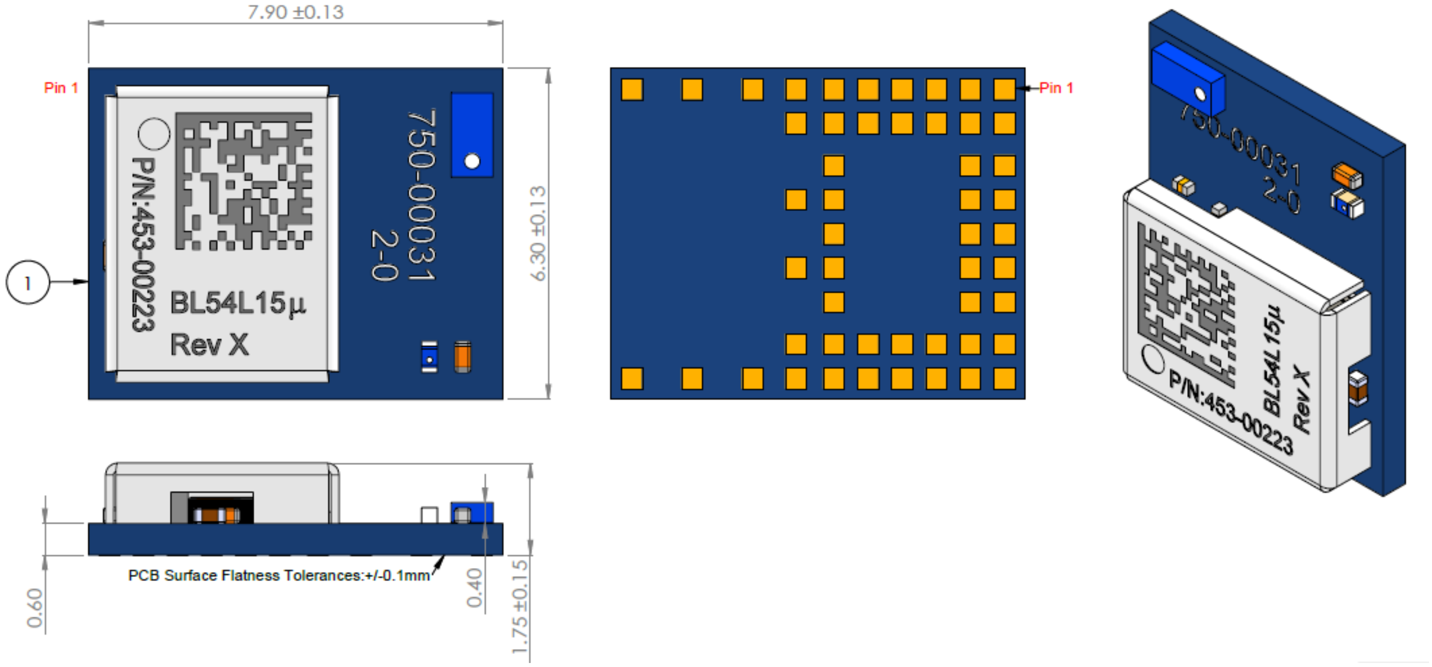


Figure 10: Mechanical Details – Chip Antenna variant (453-00223)

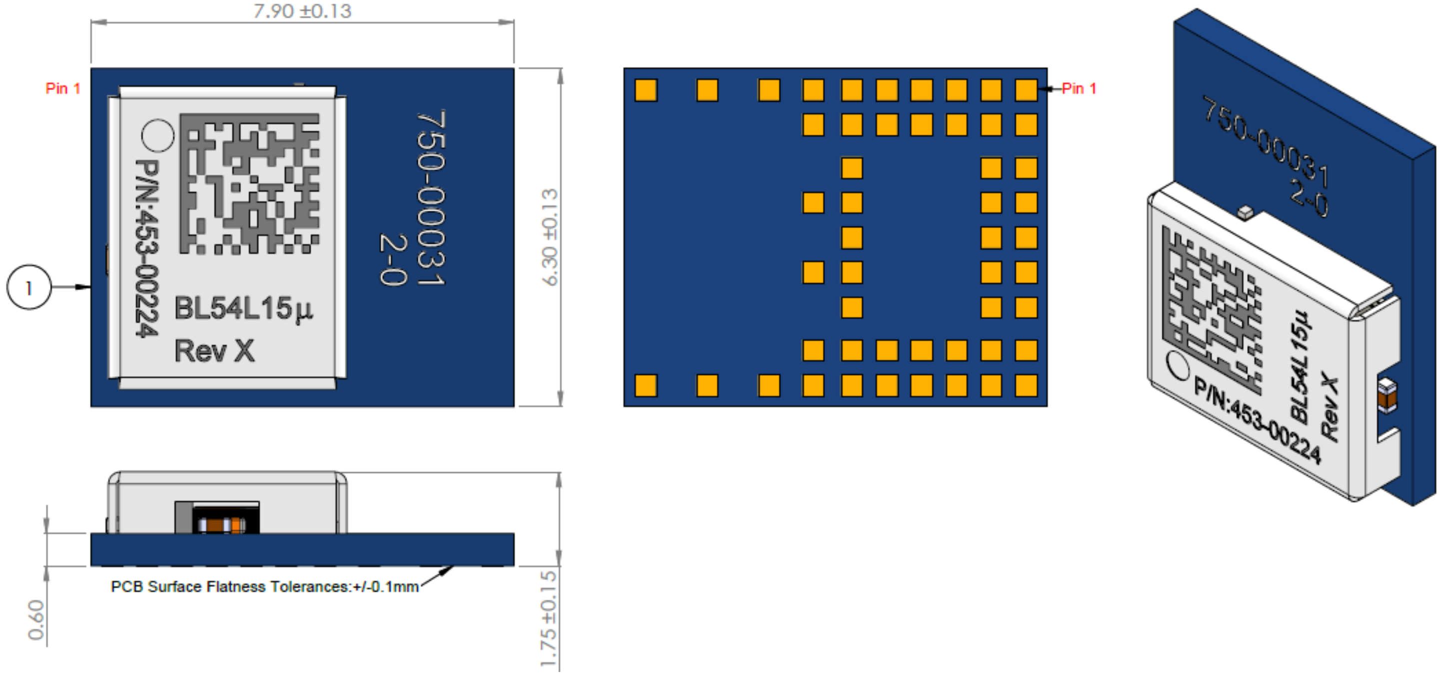
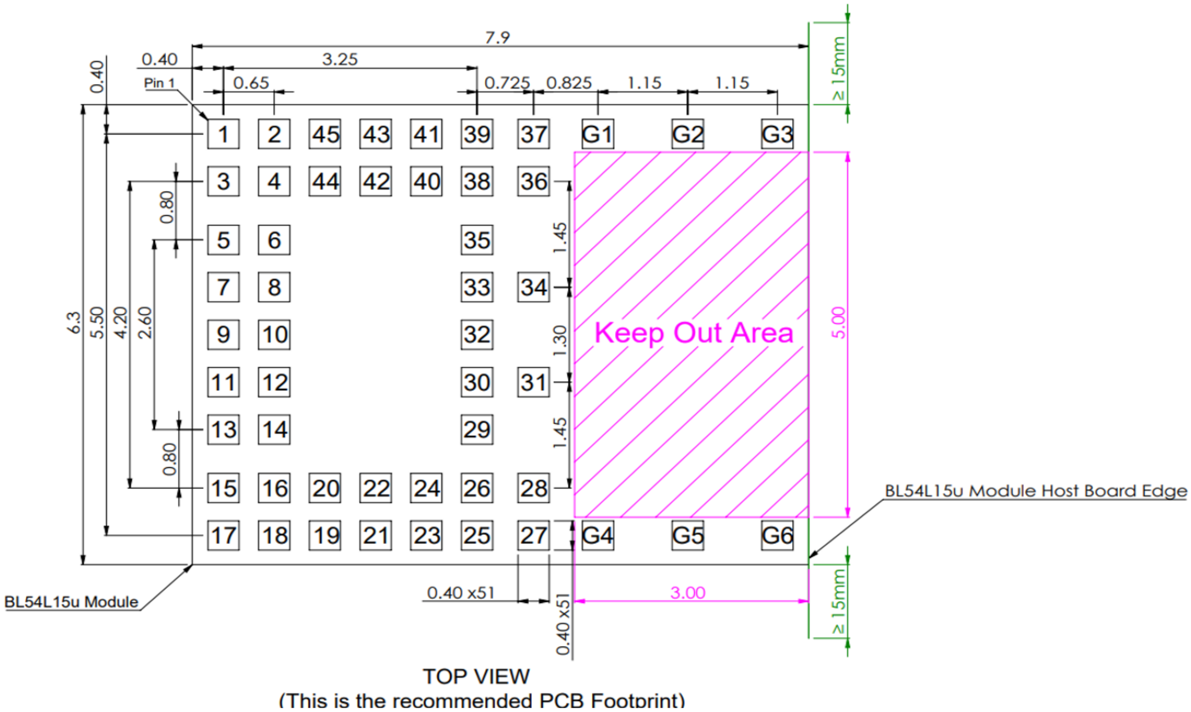


Figure 11: Mechanical Details – RF Trace pin variant (453-00224)

3D models for BL54L15µ Module, RF Trace Pin (453-00224) and BL54L15µ Module, Chip Antenna (453-00223) on the BL54L15µ product page – https://www.ezurio.com/product/BL54L15µ-series-bluetooth-le-80215-4-nfc

6.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00223

PCB footprint - BL54L15µ (DXF and Altium format) and SCH Symbol - BL54L15µ (Altium format) can be found on the BL54L15µ product page – https://www.ezurio.com/product/BL54L15µ-series-bluetooth-le-80215-4-nfc



All dimensions are in mm.

Figure 12: Land pattern and Keep-out for the 453-00223

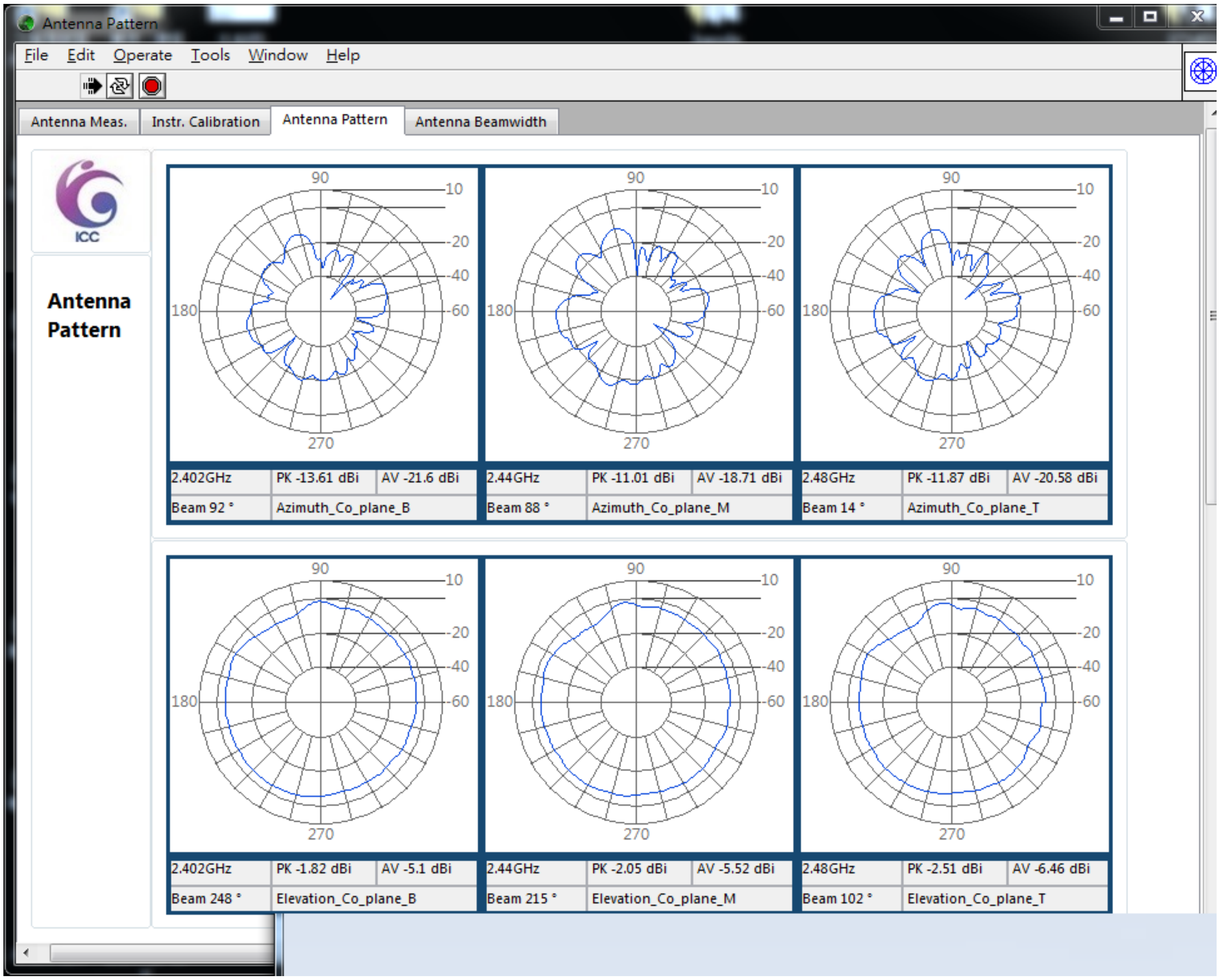
Host PCB Land Pattern and Antenna Keep-out for the 453-00xxx Notes:	
Note 1	Ensure there is no copper in the antenna 'keep out area' on any layers of the host PCB. Also keep all mounting hardware or any metal clear of the area (Refer to 5.3.2) to reduce effects of proximity detuning the antenna and to help antenna radiate properly.
Note 2	For the best on-board chip antenna performance, the module 453-00223 MUST be placed on the edge of the host PCB and preferably in the edge centre and host PCB.
Note 3	BL54L15µ development board has the 453-00223 placed on the edge of the PCB board (and not in corner), see section 6.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00223.
Note 4	Ensure that there is no exposed copper under the module on the host PCB.
Note 5	You may modify the PCB land pattern dimensions based on their experience and/or process capability.

7 On -Board PCB Chip Antenna Characteristics

7.1 Summary of Antenna Performance

	2402MHz		2440MHz		2480MHz	
	Peak	Avg	Peak	Avg	Peak	Avg
453-00223 Chip antenna	-1.82dBi	-5.1dBi	-2.05dBi	-5.52dBi	-2.51dBi	-6.46dBi

7.2 2.4GHz Radiated Performance



2.402GHz	PK -13.61 dBi	AV -21.6 dBi
Beam 92 °	Azimuth_Co_plane_B	

2.44GHz	PK -11.01 dBi	AV -18.71 dBi
Beam 88 °	Azimuth_Co_plane_M	

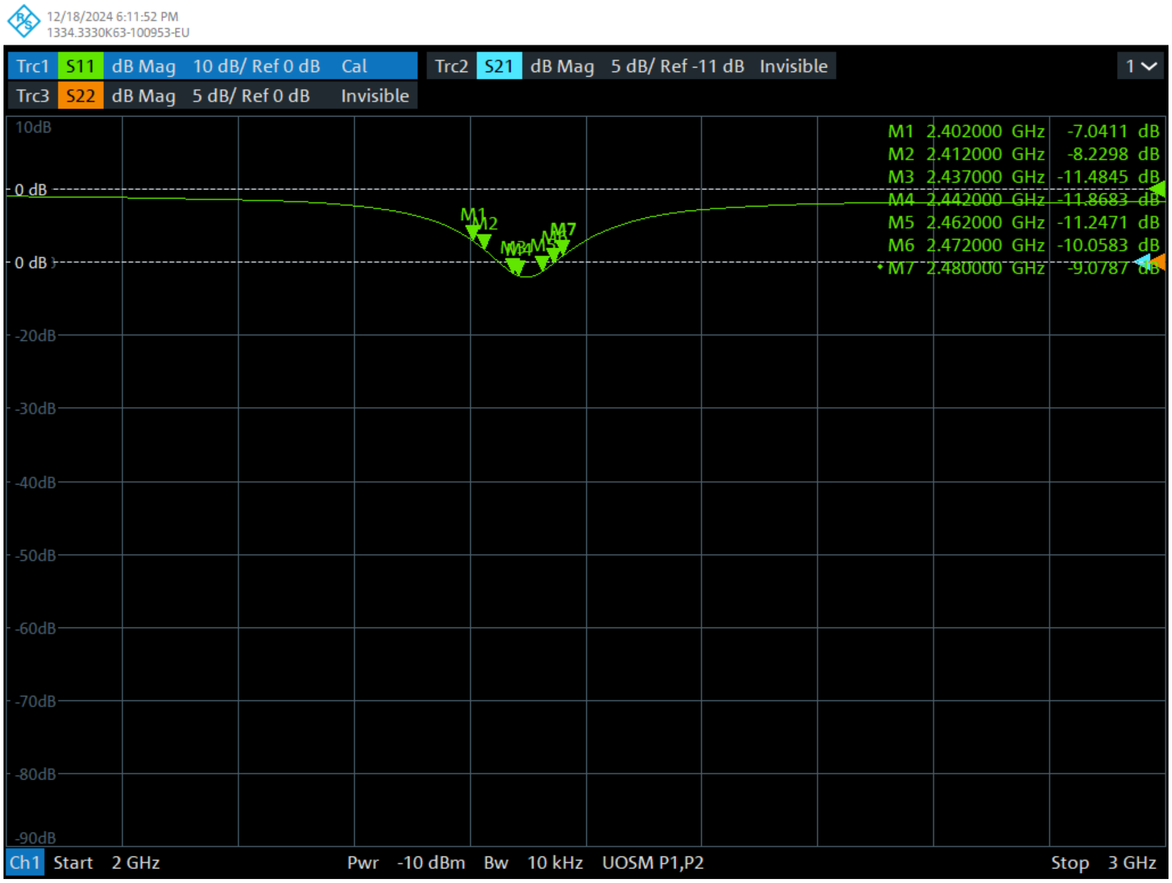
2.48GHz	PK -11.87 dBi	AV -20.58 dBi
Beam 14 °	Azimuth_Co_plane_T	

2.402GHz	PK -1.82 dBi	AV -5.1 dBi
Beam 248 °	Elevation_Co_plane_B	

2.44GHz	PK -2.05 dBi	AV -5.52 dBi
Beam 215 °	Elevation_Co_plane_M	

2.48GHz	PK -2.51 dBi	AV -6.46 dBi
Beam 102 °	Elevation_Co_plane_T	

7.3 Antenna S11 measuring data



12/18/2024 6:11:52 PM
1334.3330K63-100953-EU

```
Trc1  S11  dB Mag  10 dB/ Ref 0 dB  Cal
Trc2  S21  dB Mag  5 dB/ Ref -11 dB  Invisible
Trc3  S22  dB Mag  5 dB/ Ref 0 dB  Invisible
```

```
M1  2.402000  GHz   -7.0411  dB
M2  2.412000  GHz   -8.2298  dB
M3  2.437000  GHz  -11.4845  dB
M4  2.442000  GHz  -11.8683  dB
M5  2.462000  GHz  -11.2471  dB
M6  2.472000  GHz  -10.0583  dB
M7  2.480000  GHz   -9.0787  dB
```

```
Ch1  Start  2 GHz        Pwr  -10 dBm   Bw  10 kHz   UOSM P1,P2        Stop  3 GHz
```

8 Application Note for Surface Mount Modules

8.1 Introduction

Ezurio's surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the user manual. This application note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of several commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

Part numbers – 453-00223R and 453-00224R are shipped as Tape / Reel, with a reel containing 1,000 pcs.

8.2 Module Packaging Configuration

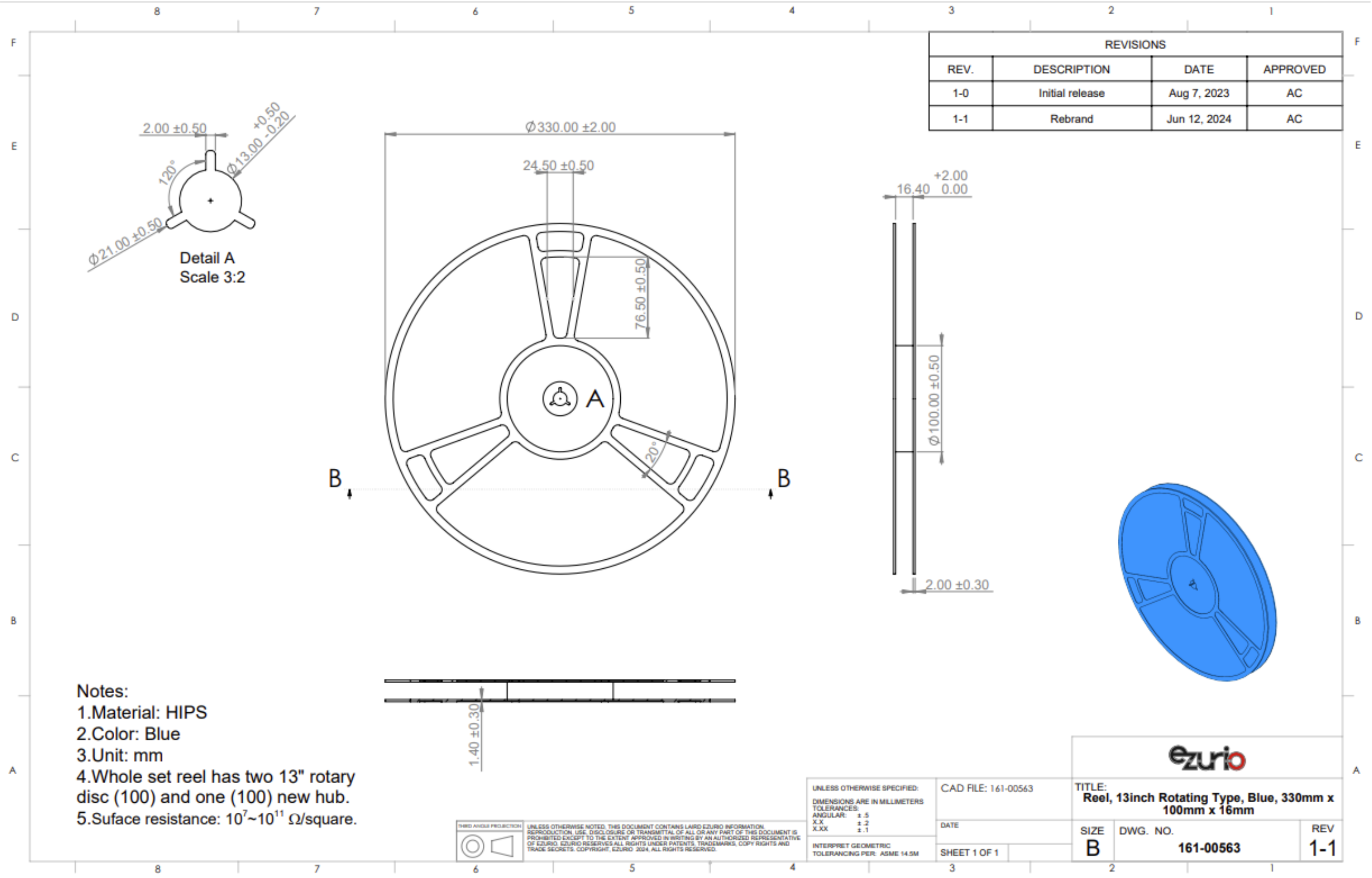
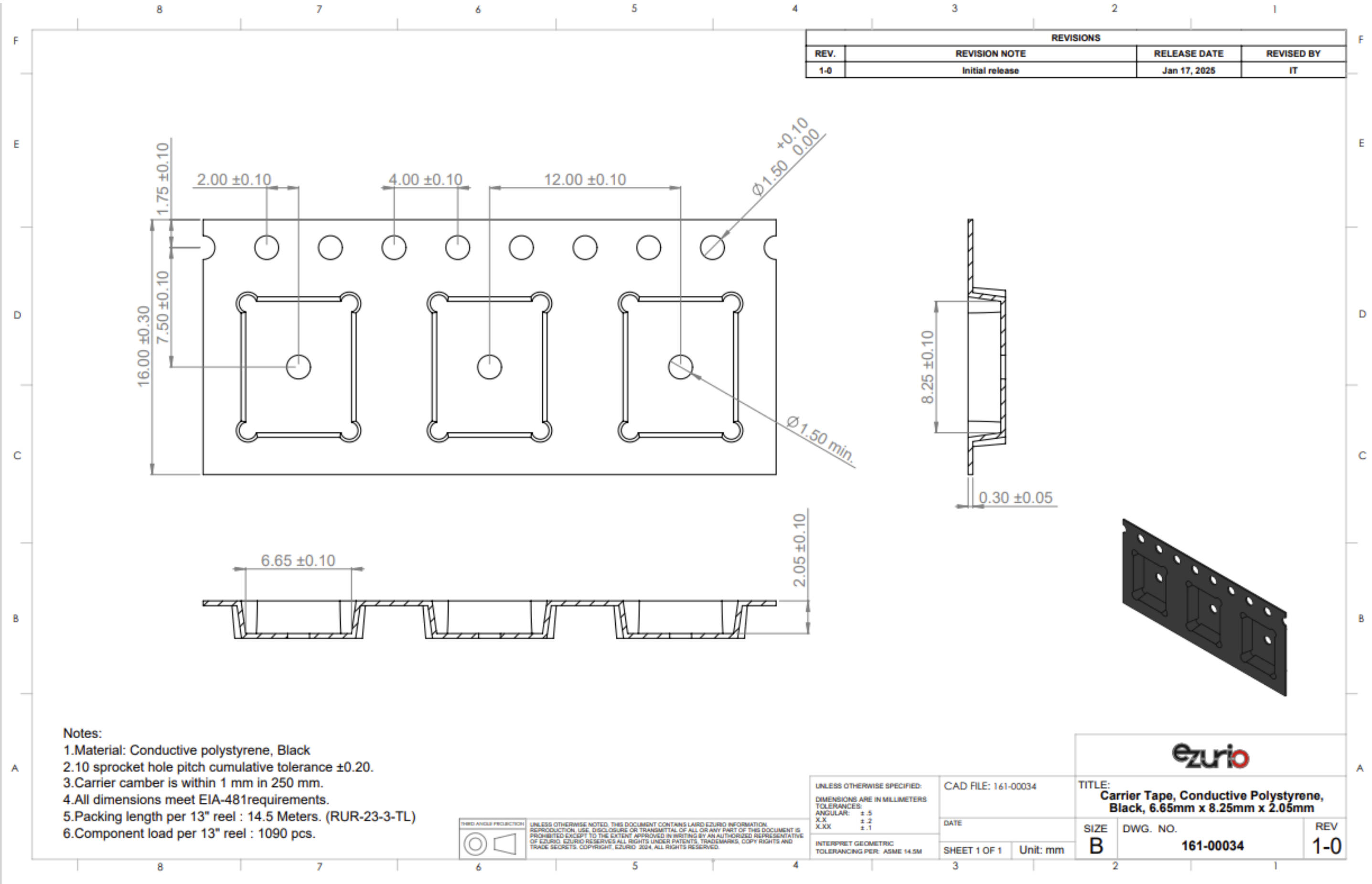


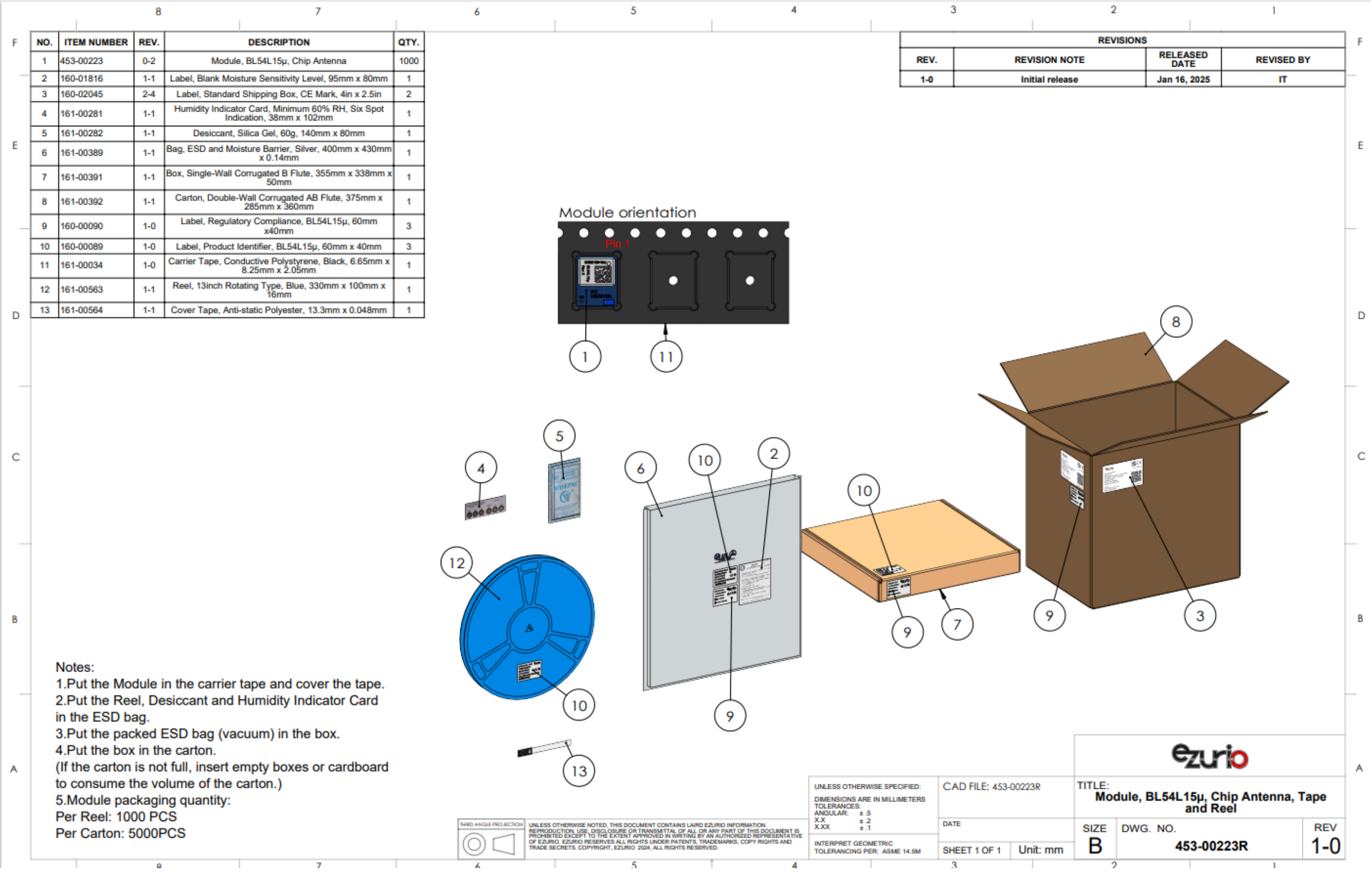
Figure 13: Reel specifications – 1,000 pieces per reel



REVISIONS			
REV.	REVISION NOTE	RELEASE DATE	REVISED BY
1-0	Initial release	Jan 17, 2025	IT

Notes:
1.Material: Conductive polystyrene, Black
2.10 sprocket hole pitch cumulative tolerance ±0.20.
3.Carrier camber is within 1 mm in 250 mm.
4.All dimensions meet EIA-481requirements.
5.Packing length per 13" reel : 14.5 Meters. (RUR-23-3-TL)
6.Component load per 13" reel : 1090 pcs.

Figure 14: Carrier Tape specifications



NO.	ITEM NUMBER	REV.	DESCRIPTION	QTY.
1	453-00223	0-2	Module, BL54L15µ, Chip Antenna	1000
2	160-01816	1-1	Label, Blank Moisture Sensitivity Level, 95mm x 80mm	1
3	160-02045	2-4	Label, Standard Shipping Box, CE Mark, 4in x 2.5in	2
4	161-00281	1-1	Humidity Indicator Card, Minimum 60% RH, Six Spot Indication, 38mm x 102mm	1
5	161-00282	1-1	Desiccant, Silica Gel, 60g, 140mm x 80mm	1
6	161-00389	1-1	Bag, ESD and Moisture Barrier, Silver, 400mm x 430mm x 0.14mm	1
7	161-00391	1-1	Box, Single-Wall Corrugated B Flute, 355mm x 338mm x 50mm	1
8	161-00392	1-1	Carton, Double-Wall Corrugated AB Flute, 375mm x 285mm x 360mm	1
9	160-00090	1-0	Label, Regulatory Compliance, BL54L15µ, 60mm x40mm	3
10	160-00089	1-0	Label, Product Identifier, BL54L15µ, 60mm x 40mm	3
11	161-00034	1-0	Carrier Tape, Conductive Polystyrene, Black, 6.65mm x 8.25mm x 2.05mm	1
12	161-00563	1-1	Reel, 13inch Rotating Type, Blue, 330mm x 100mm x 16mm	1
13	161-00564	1-1	Cover Tape, Anti-static Polyester, 13.3mm x 0.048mm	1

REVISIONS

REV.	REVISION NOTE	RELEASED DATE	REVISED BY
1-0	Initial release	Jan 16, 2025	IT

Notes:
1.Put the Module in the carrier tape and cover the tape.
2.Put the Reel, Desiccant and Humidity Indicator Card in the ESD bag.
3.Put the packed ESD bag (vacuum) in the box.
4.Put the box in the carton.
(If the carton is not full, insert empty boxes or cardboard to consume the volume of the carton.)
5.Module packaging quantity:
Per Reel: 1000 PCS
Per Carton: 5000PCS

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UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILLIMETERS
TOLERANCES:
ANGULAR: ± .5
X.X ± .2
X.XX ± .1
INTERPRET GEOMETRIC TOLERANCING PER: ASME 14.5M

CAD FILE: 453-00223R
DATE
SHEET 1 OF 1
Unit: mm

TITLE: Module, BL54L15µ, Chip Antenna, Tape and Reel
SIZE: B
DWG. NO.: 453-00223R
REV: 1-0

Figure 15: BL54L15u Packaging Process for Chip Antenna Variant

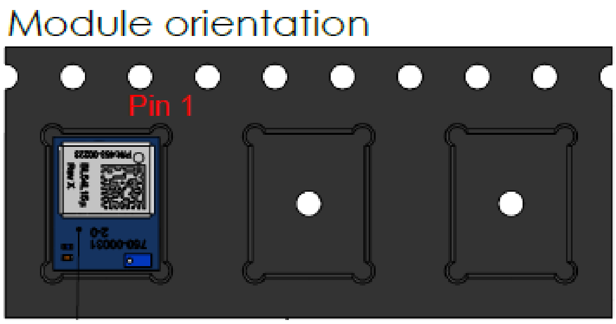
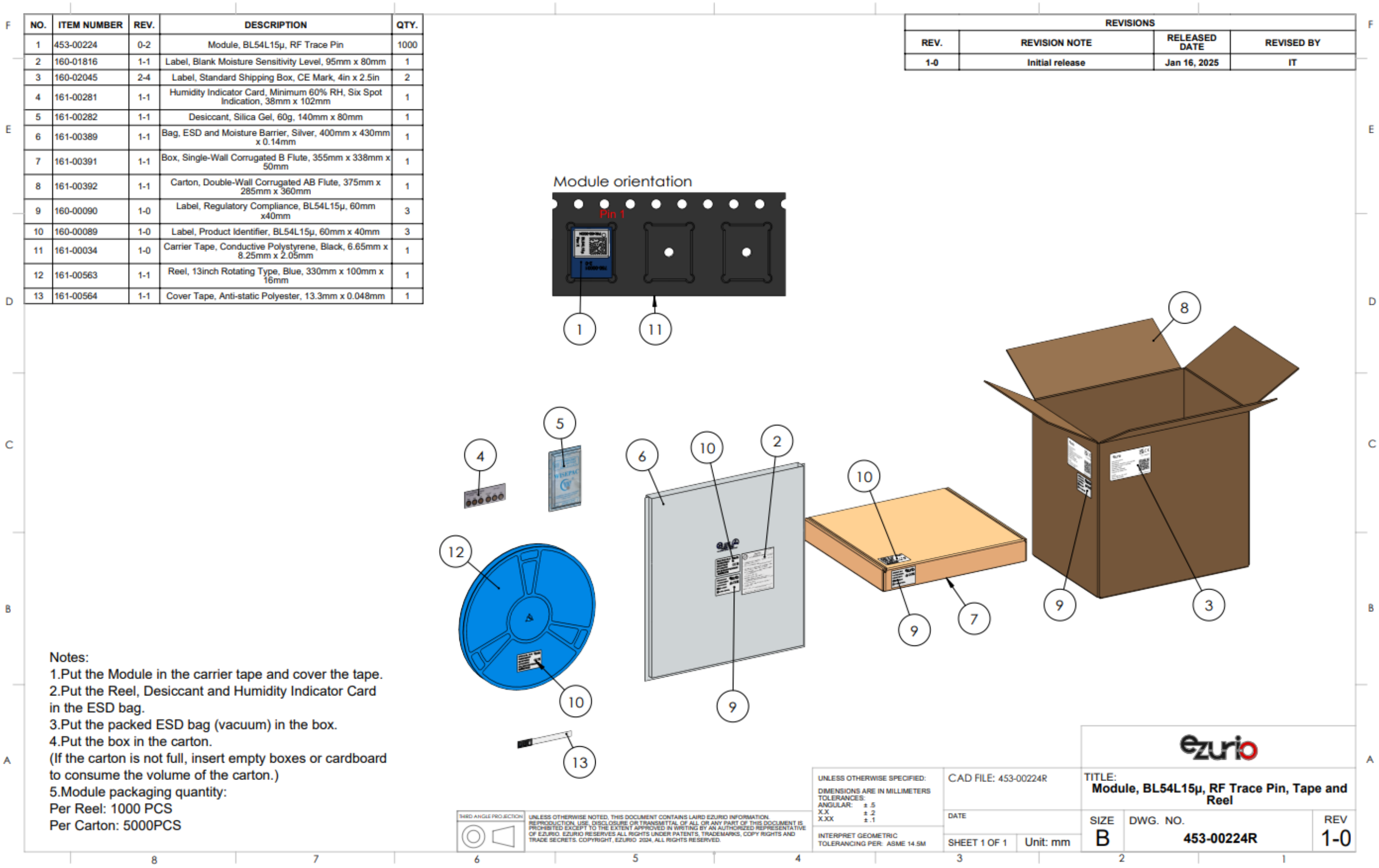


Figure 16: Module Orientation in Carrier Tape Pocket, Chip Antenna Variant



NO.	ITEM NUMBER	REV.	DESCRIPTION	QTY.
1	453-00224	0-2	Module, BL54L15µ, RF Trace Pin	1000
2	160-01816	1-1	Label, Blank Moisture Sensitivity Level, 95mm x 80mm	1
3	160-02045	2-4	Label, Standard Shipping Box, CE Mark, 4in x 2.5in	2
4	161-00281	1-1	Humidity Indicator Card, Minimum 60% RH, Six Spot Indication, 38mm x 102mm	1
5	161-00282	1-1	Desiccant, Silica Gel, 60g, 140mm x 80mm	1
6	161-00389	1-1	Bag, ESD and Moisture Barrier, Silver, 400mm x 430mm x 0.14mm	1
7	161-00391	1-1	Box, Single-Wall Corrugated B Flute, 355mm x 338mm x 50mm	1
8	161-00392	1-1	Carton, Double-Wall Corrugated AB Flute, 375mm x 285mm x 360mm	1
9	160-00090	1-0	Label, Regulatory Compliance, BL54L15µ, 60mm x40mm	3
10	160-00089	1-0	Label, Product Identifier, BL54L15µ, 60mm x 40mm	3
11	161-00034	1-0	Carrier Tape, Conductive Polystyrene, Black, 6.65mm x 8.25mm x 2.05mm	1
12	161-00563	1-1	Reel, 13inch Rotating Type, Blue, 330mm x 100mm x 16mm	1
13	161-00564	1-1	Cover Tape, Anti-static Polyester, 13.3mm x 0.048mm	1

REVISIONS			
REV.	REVISION NOTE	RELEASED DATE	REVISED BY
1-0	Initial release	Jan 16, 2025	IT

Notes:
1.Put the Module in the carrier tape and cover the tape.
2.Put the Reel, Desiccant and Humidity Indicator Card in the ESD bag.
3.Put the packed ESD bag (vacuum) in the box.
4.Put the box in the carton.
(If the carton is not full, insert empty boxes or cardboard to consume the volume of the carton.)
5.Module packaging quantity:
Per Reel: 1000 PCS
Per Carton: 5000PCS

THIRD ANGLE PROJECTION

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UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILLIMETERS
TOLERANCES:
ANGULAR: ± .5
X.X ± .2
X.XX ± .1
INTERPRET GEOMETRIC TOLERANCING PER: ASME 14.5M

CAD FILE: 453-00224R
DATE
SHEET 1 OF 1
Unit: mm

TITLE: Module, BL54L15µ, RF Trace Pin, Tape and Reel
SIZE: B
DWG. NO.: 453-00224R
REV: 1-0

Figure 17: BL54L15u Packaging Process for trace pin Variant

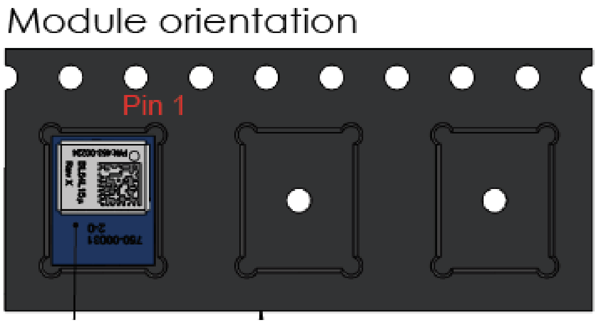


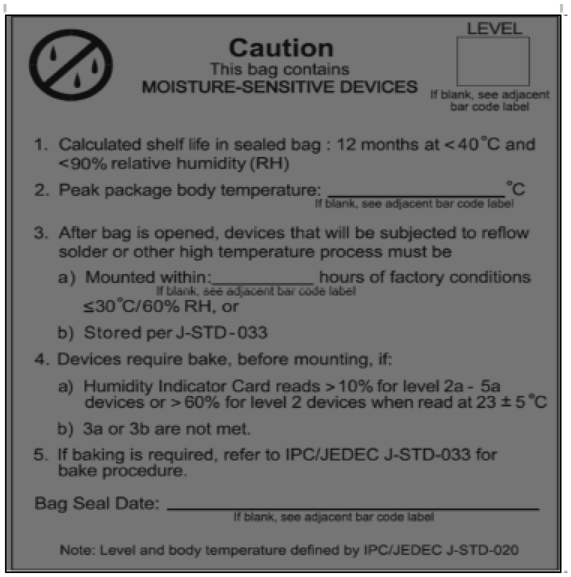
Figure 18: Module Orientation in Carrier Tape Pocket, trace pin Variant

8.3 Module Shipping

All modules are shipped in tape and reel package and sealed in ESD Bags.

8.4 Labeling

The following labels are placed on the anti-static bag. The BL54L15u solder-down modules are classified as MSL4 devices.



Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

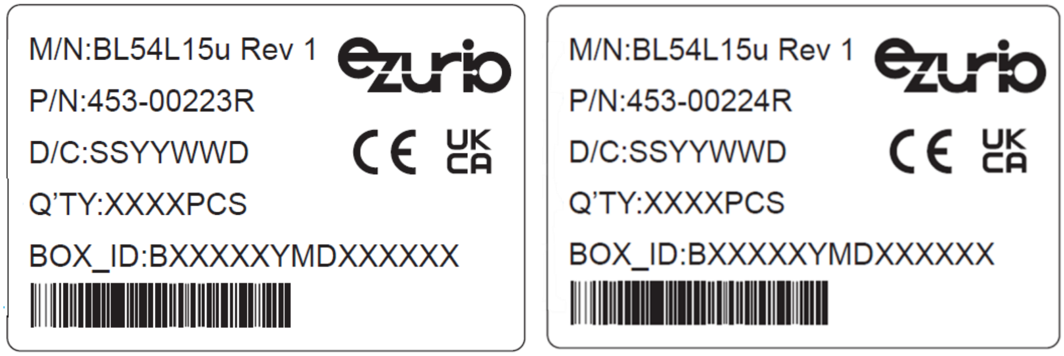
LEVEL
If blank, see adjacent bar code label

1. Calculated shelf life in sealed bag : 12 months at < 40°C and <90% relative humidity (RH)
2. Peak package body temperature: ____________ °C
   If blank, see adjacent bar code label
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within: ________ hours of factory conditions
      If blank, see adjacent bar code label
      ≤30°C/60% RH, or
   b) Stored per J-STD-033
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card reads > 10% for level 2a - 5a devices or > 60% for level 2 devices when read at 23 ± 5°C
   b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

Bag Seal Date: ____________________
If blank, see adjacent bar code label

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

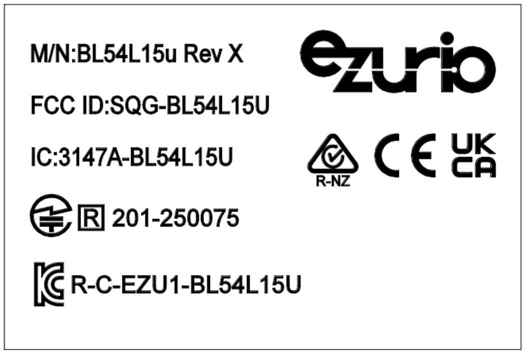
Figure 19: Moisture Sensitivity Level Label



M/N:BL54L15u Rev 1
P/N:453-00223R
D/C:SSYYWWD
Q'TY:XXXXPCS
BOX_ID:BXXXXXYMDXXXXXX

M/N:BL54L15u Rev 1
P/N:453-00224R
D/C:SSYYWWD
Q'TY:XXXXPCS
BOX_ID:BXXXXXYMDXXXXXX

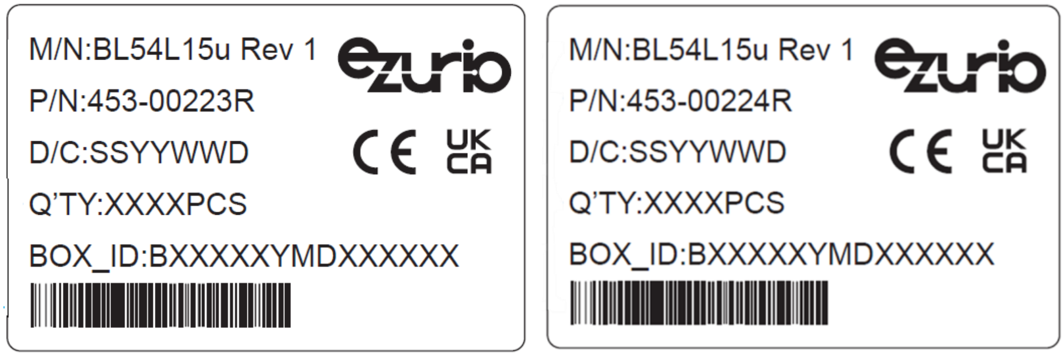
Figure 20: Product Identifier Label



M/N:BL54L15u Rev X
FCC ID:SQG-BL54L15U
IC:3147A-BL54L15U
R 201-250075
R-C-EZU1-BL54L15U
R-NZ

Figure 21: Regulatory Compliance Label

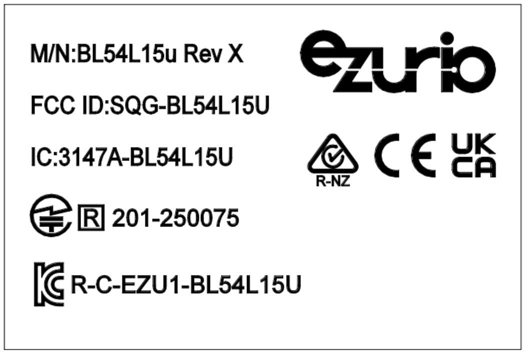
The following labels are placed on the pizza box.



M/N:BL54L15u Rev 1
P/N:453-00223R
D/C:SSYYWWD
Q'TY:XXXXPCS
BOX_ID:BXXXXXYMDXXXXXX

M/N:BL54L15u Rev 1
P/N:453-00224R
D/C:SSYYWWD
Q'TY:XXXXPCS
BOX_ID:BXXXXXYMDXXXXXX

Figure 22: Product Identifier Label



M/N:BL54L15u Rev X
FCC ID:SQG-BL54L15U
IC:3147A-BL54L15U
R-NZ
R 201-250075
R-C-EZU1-BL54L15U

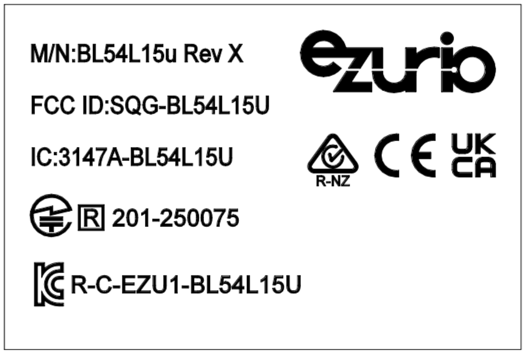
Figure 23: Regulatory Compliance Label

The following labels are placed on the master shipping carton.

P/N:453-00223R
Revision:1
Description:*Module,*BL54L15u,
*Chip Antenna,*T/R
Quantity:XXXX
Date*Code:SSYYWWD
Country*of*Origin:XX
Ezurio
50*S.*Main*St.*Ste.*1100
Akron,*OH*44308
PO:XXXXXXX
www.ezurio.com

P/N:453-00224R
Revision:1
Description:*Module,*BL54L15u,
*Chip Antenna,*T/R
Quantity:XXXX
Date*Code:SSYYWWD
Country*of*Origin:XX
Ezurio
50*S.*Main*St.*Ste.*1100
Akron,*OH*44308
PO:XXXXXXX
www.ezurio.com

Figure 24: Standard Shipping Carton Label



M/N:BL54L15u Rev X
FCC ID:SQG-BL54L15U
IC:3147A-BL54L15U
R-NZ
R 201-250075
R-C-EZU1-BL54L15U

Figure 25:Regulatory Compliance Label

8.5 Required Storage Conditions

8.5.1 Prior to Opening the Dry Packing

The following are required storage conditions ***prior* to opening the dry packing**:

- Normal temperature: 5~40˚C
- Normal humidity: 80% (Relative humidity) or less
- Storage period: One year or less

Note: Humidity means relative humidity.

8.5.2 After Opening the Dry Packing

The following are required storage conditions ***after* opening the dry packing** (to prevent moisture absorption):

- Storage conditions for one-time soldering:
  - Temperature: 5-25°C
  - Humidity: 60% or less
  - Period: 72 hours or less after opening
- Storage conditions for two-time soldering
  - Storage conditions following opening and prior to performing the 1st reflow:
    - Temperature: 5-25°C
    - Humidity: 60% or less
    - Period: A hours or less after opening
  - Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow
    - Temperature: 5-25°C
    - Humidity: 60% or less
    - Period: B hours or less after completion of the 1st reflow

---

Note: Should keep A+B within 72 hours.

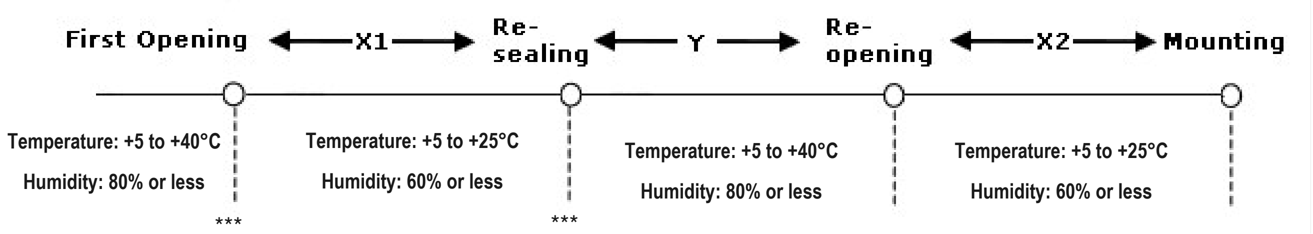
8.5.3 Temporary Storage Requirements after Opening

The following are temporary storage requirements after opening:

- Only re-store the devices *once* prior to soldering.
- Use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using vacuumed heat-sealing.

The following indicate the required storage period, temperature, and humidity for this temporary storage:

- Storage temperature and humidity:



*** - External atmosphere temperature and humidity of the dry packing

- Storage period:
  - X1+X2 – Refer to After Opening the Dry Packing storage requirements. Keep is X1+X2 within 72 hours.
  - Y – Keep within two weeks or less.

8.6 Baking Conditions

Baking conditions and processes for the module follow the J-STD-033 standard which includes the following:

- The calculated shelf life in a sealed bag is 12 months at ‹ 40℃ and ‹ 80% relative humidity.
- Once the packaging is opened, the SiP must be mounted (per MSL4/Moisture Sensitivity Level 4) within 72 hours at ‹ 30 ˚C and ‹ 60% relative humidity.
- If the SiP is not mounted within 72 hours or if, when the dry pack is opened, the humidity indicator card displays ›10% humidity, then the product must be baked for 48 hours at 125 ˚C (±5 ˚C).

8.7 Surface Mount Conditions

The following soldering conditions are recommended to ensure device quality.

8.7.1 Soldering

Note: When soldering, the stencil thickness should be ≥ 0.1 mm.

Convection reflow or IR/Convection reflow (one-time soldering or two-time soldering in air or nitrogen environment)

- Measuring point – IC package surface
- Temperature profile:

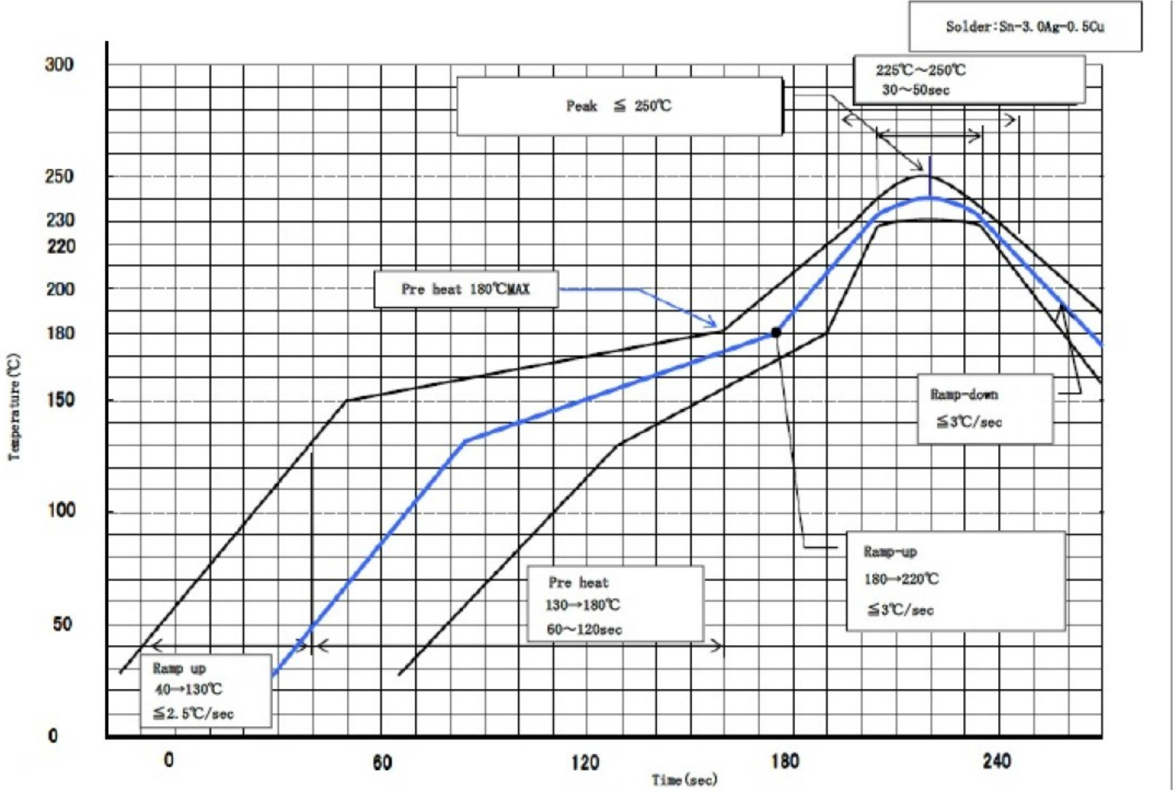


Figure 26: Temperature profile

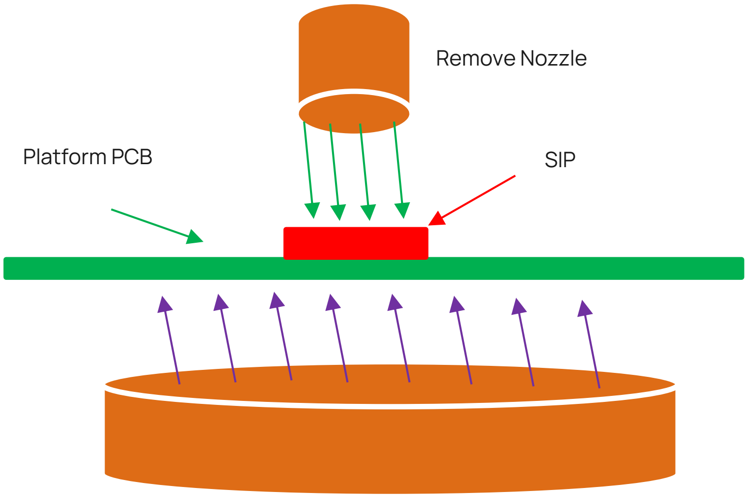
- Ramp-up: 40-130˚C. Less than 2.5˚C/sec
- Pre heat: 130-180˚C 60-120 sec, 180˚C MAX
- Ramp-up: 180-220˚C. Less than 3˚C/sec
- Peak Temperature: MAX 250˚C
  - 225˚C ~ 250˚C, 30 ~ 50 sec
- Ramp-down: Less than 3˚C/sec

8.7.2 Cautions When Removing the SIP from the Platform for RMA

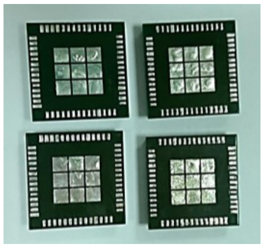
- Bake the platform before removing the SIP from the platform. Reference baking conditions.
- Remove the SIP by using a hot air gun. This process should be carried out by a skilled technician.

Suggestion conditions:

- One-side component platform:
  - Set the hot plate at 280 °C.
  - Put the platform on the hot plate for 8~10 seconds.
  - Remove the SIP from platform.
- Two-side components platform:
  - Use two hot air guns
  - On the bottom side, use a pre-heated nozzle (temperature setting of 200~250 °C) at a suitable distance from the platform PCB.
  - On the top side, apply a remove nozzle (temperature setting of 330 °C). Heat the SIP until it can be removed from platform PCB.

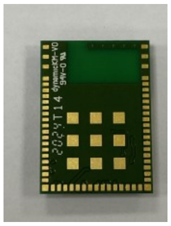


- Remove the residue solder under the bottom side of SIP. (Note: Alternate module pictured as an example)



(Not accepted for RMA)

Example SIP with residue solder on the bottom



(Accepted for RMA analysis)

Example Module, no residue solder

- Remove and clean the residue flux as needed.

8.7.3 Precautions for Use

- Opening/handing/removing must be done on an anti-ESD treated workbench. All workers must also have undergone anti-ESD treatment.
- The devices should be mounted within one year of the date of delivery.
- The BL54L15u modules are MSL 4 rated.

9 Reliability Test

9.1 Climatic And Dynamic Reliability Test

Table 5: Climatic and Dynamic Reliability Test Results for BL54L15u Modules

Test Item	Specification	Standard	Test Result
Thermal Shock	Temperature: -40 ~ 105℃ Ramp time: Less than 10 seconds. Dwell Time: 10 minutes Number of Cycles: 350 times	*JESD22-A106 *IEC 60068-2-14 for dwell time and number of cycles	PASS
Vibration Non-Operating Unpackaged device	Vibration Wave Form: Sine Waveform Vibration frequency / Displacement: 20-80 Hz/1.5mm Vibration frequency / Acceleration: 80-2000 Hz/20g Cycle Time: 4 min/cycle Number of Cycles: 4 cycle/axis Vibration Axes: X, Y and Z (Rotate each axis on vertical vibration table)	JEDEC 22-B103B (2016)	PASS
Mechanical Shock Non-Operating Unpackaged device	Pulse shape: Half-sine waveform Impact acceleration: 1500 g Pulse duration: 0.5 ms Number of shocks: 30 shocks (5 shocks for each face) Orientation: Bottom, top, left, right, front, and rear faces	JEDEC 22-B110B.01 (2019)	PASS

9.2 Reliability MTBF Prediction

Table 6: MTBF Predictions for BL54L15u Modules

Ezurio Part Number	Environment	Standard	Test Result 45 ℃ (Hours)
453-00223R 453-00223C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	6,126,139
453-00224R 453-00224C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	6,858,984
453-00223R 453-00223C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	2,297,302
453-00224R 453-00224C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	2,572,119
Ezurio Part Number	**Environment**	**Standard**	**Test Result 105 ℃ (Hours)**
453-00223R 453-00223C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	639,566
453-00224R 453-00224C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	724,666
453-00223R 453-00223C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	239,837
453-00224R 453-00224C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	271,750

10 Regulatory

Full regulatory information on the BL54L15u, including the Regulatory Information Guide, grants, and test reports are available on the BL54L15u product page (coming soon).

The BL54L15u holds current certifications in the following countries:

Table 7: BL54L15u Certifications

Country/Region	Regulatory ID
USA (FCC)	SQG-BL54L15U
EU (ETSI)	N/A (No ID Number Required)
UKCA	N/A (No ID Number Required)
Canada (ISED)	3147A-BL54L15U
Japan (MIC)	201-250075
Australia (RCM)	N/A
New Zealand (RCM)	N/A
Korea	R-C-EZU1-BL54L15U

10.1 Certified Antennas for the BL54L15u

Table 8: Certified Antennas for BL54L15u Modules

Manufacturer	Model	Ezurio Part Number	Type	Connector	Peak Gain 2400-2500 MHz	Peak Gain 2400-2480 MHz
Ezurio (Laird Connectivity)	NanoBlue	EBL2400A1-10MH4L	PCB Dipole	IPEX MHF4	2 dBi	-
Ezurio (Laird Connectivity)	FlexPIFA	001-0022	PIFA	IPEX MHF4	-	2 dBi
Mag.Layers	EDA-8709-2G4C1-B27-CY	0600-00057	Dipole	IPEX MHF4	2.32 dBi	-
Ezurio (Laird Connectivity)	mFlexPIFA	EFA2400A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	iFlexPIFA Mini	EFG2401A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	Ezurio NFC	0600-00061	NFC	N/A	-	-

11 Ordering Information

Part Number	Product Description
453-00223R	Module, BL54L15µ, (Nordic nRF54L15), Chip antenna, Tape/Reel
453-00224R	Module, BL54L15µ, (Nordic nRF54L15), RF Trace Pin, Tape/Reel
453-00223C	Module, BL54L15µ, (Nordic nRF54L15), Chip antenna, Cut Tape
453-00224C	Module, BL54L15µ, (Nordic nRF54L15), RF Trace Pin, Cut Tape
453-00223-K1	Development kit, Module, BL54L15µ (Nordic nRF54L15), Chip antenna
453-00224-K1	Development kit, Module, BL54L15µ (Nordic nRF54L15), RF Trace Pin

12 Bluetooth Qualification Process

12.1 Overview

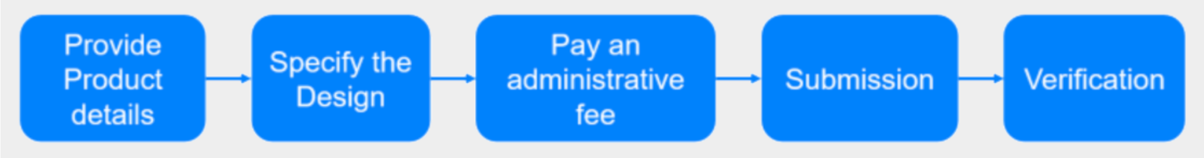
The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the Qualification Program Reference Document (QPRD) v3.

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

- Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
- Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:



To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: Apply for Adopter Membership

12.2 Scope

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference multiple existing designs, that have not been modified, (refer to Section 3.2.2.1 of the Qualification Program Reference Document v3).

For a Product that includes a new Design created by combining two or more unmodified designs that have DNs or QDIDs into one of the permitted combinations in Table 3.1 of the QPRDv3, a Member must also provide the following information:

- DNs or QDIDs for Designs included in the new Design
- The desired Core Configuration of the new Design (if applicable, see Table 3.1 below)
- The active TCRL Package version used for checking the applicable Core Configuration (including transport compatibility) and evaluating test requirements

Any included Design must not implement any Layers using withdrawn specification(s).

When creating a new Design using Option 2a, the Inter-Layer Dependency (ILD) between Layers included in the Design will be checked based on the latest TCRL Package version used among the included Designs.

For the purposes of this document, it is assumed that the member is combining unmodified Core-Controller Configuration and Core-Host Configuration designs, to complete a Core-Complete Configuration.

12.3 Qualification Steps When Referencing multiple existing designs, (unmodified) – Option 2a in the QPRDv3

For this qualification option, follow these steps:

1. To start a listing, go to: https://qualification.bluetooth.com/
2. Select **Start the Bluetooth Qualification Process**.
3. Product Details to be entered:
    - Project Name (this can be the product name or the Bluetooth Design name).
    - Product Description
    - Model Number
    - Product Publication Date (the product publication date may not be later than 90 days after submission)

   - Product Website (optional)
   - Internal Visibility (this will define if the product will be visible to other users prior to publication)
   - If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.
4. Specify the Design:
   - Do you include any existing Design(s) in your Product? Answer Yes, I do.
   - Enter the multiple DNs or QDIDs used in your, (for Option 2a two or more DNs or QDIDs must be referenced)
   - Select 'I'm finished entering DN's
   - Once the DNs or QDIDs are selected they will appear on the left-hand side, indicating the layers covered by the design (should show Core-Controller and Core Host Layers covered).
   - What do you want to do next? Answer, 'Combine unmodified Designs'.
   - The Qualification Workspace Tool will indicate that a new Design will be created and what type of Core-Complete configuration is selected.
   - An active TCRL will be selected for the design.
   - Perform the Consistency Check, which should result in no inconsistencies
   - If there are any inconsistencies these will need to be resolved before proceeding
   - Save and go to Test Plan and Documentation
5. Test Plan and Documentation
   a. As no modifications have been made to the combined designs the tool should report the following message:
   'No test plan has been generated for your new Design. Test declarations and test reports do not need to be submitted. You can continue to the next step.'
   b. Save and go to Product Qualification fee
6. Product Qualification Fee:
   - It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
   - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
   - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
   - Once you have selected the Prepaid Qualification Fee, select 'Save and go to Submission'
7. Submission:
   - Some automatic checks occur to ensure all submission requirements are complete.
   - To complete the listing any errors must be corrected
   - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.
   - Now select 'Complete the Submission'.
   - You will be asked a final time to confirm you want to proceed with the submission, select 'Complete the Submission'.
   - Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).
8. Download Product and Design Details (SDoC):
   a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:
https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

12.4 Example Design Combinations

The following gives an example of a design possible under option 1:

Ezurio End Product design using Nordic Component based design

Design Name	Owner	Design ID	Link to listing on the SIG website
BL54L15/BL54L15µ	Ezurio	Q345095	https://qualification.bluetooth.com/ListingDetails/274104

12.5 Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.

To add more products to your design, select 'Manage Submitted Products' in the Getting Started page, Actions, Qualify More Products. The tool will take you through the updating process.

13 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

Note: Information contained in this document is subject to change.

Ezurio's products are subject to standard Terms & Conditions.