XRT73LC04A

4 CHANNEL DS3/E3/STS-1 LINE INTERFACE UNIT

SEPTEMBER 2008 *REV. 1.0.2*

GENERAL DESCRIPTION

The XRT73LC04A, 4-Channel, DS3/E3/STS-1 Line Interface Unit is a low power CMOS version of the XRT73L04A and consists of four independent line transmitters and receivers integrated on a single chip designed for DS3, E3 or SONET STS-1 applications.

Each channel of the XRT73LC04A can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Each channel can be configured to operate in a mode/data rate that is independent of the other channels.

In the transmit direction, each channel encodes input data to either B3ZS (DS3/STS-1) or HDB3 (E3) format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction, the XRT73LC04A performs equalization on incoming signals, performs Clock Recovery, decodes data from either B3ZS or HDB3 format, converts the receive data into TTL/CMOS format, checks for LOS or LOL conditions and detects and declares the occurrence of Line Code Violations.

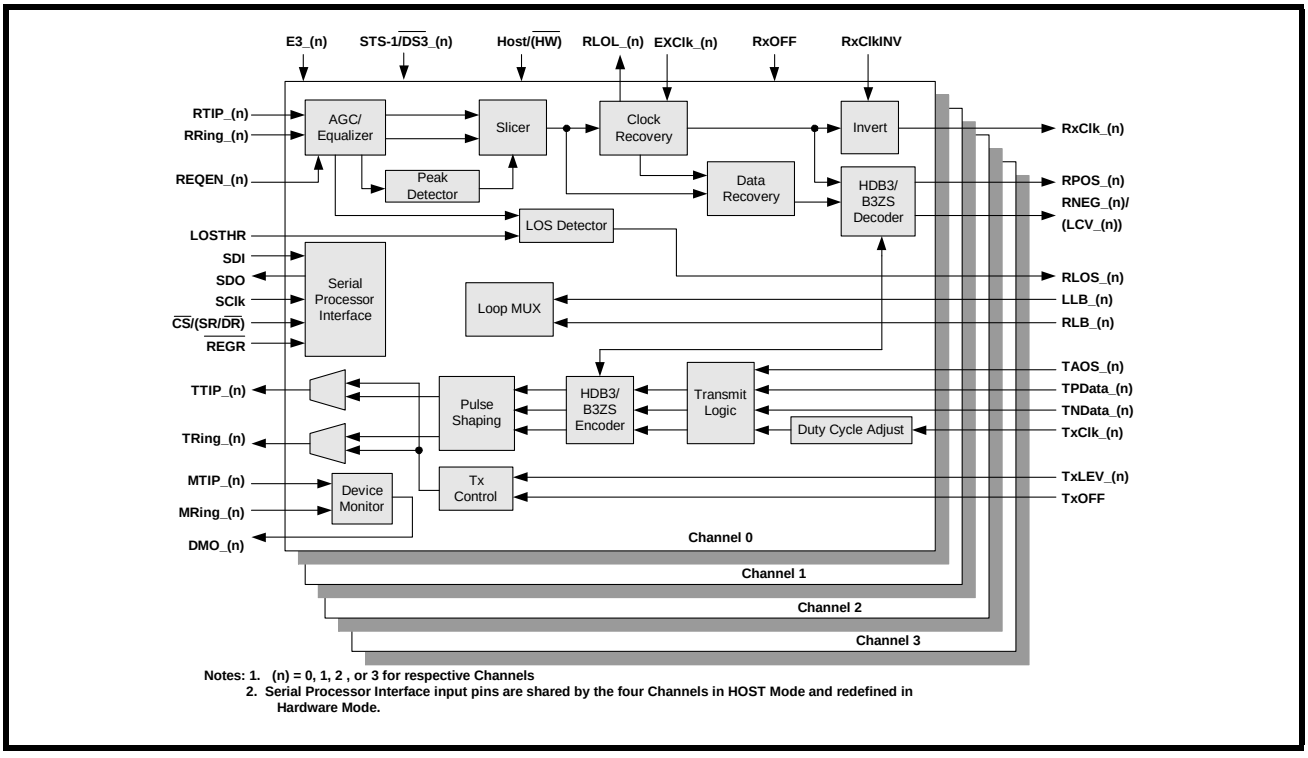
FEATURES

- Incorporates an improved Timing Recovery circuit and is pin and functional compatible to XRT73L04A
- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Contains a 4-Wire Microprocessor Serial Interface
- Full Loop-Back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Uses Minimum External components
- Single +3.3V Power Supply
- Low Power CMOS design
- 5V tolerant I/O
- -40℃ to +85℃ Operating Temperature Range
- Available in a Thermally Enhanced 144 pin LQFP package

APPLICATIONS

- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals
- Multiplexers
- ATM Switches

FIGURE 1. XRT73LC04A BLOCK DIAGRAM



Notes: 1. (n) = 0, 1, 2 , or 3 for respective Channels
2. Serial Processor Interface input pins are shared by the four Channels in HOST Mode and redefined in Hardware Mode.

TYPICAL APPLICATIONS

FIGURE 2. MULTICHANNEL ATM APPLICATION

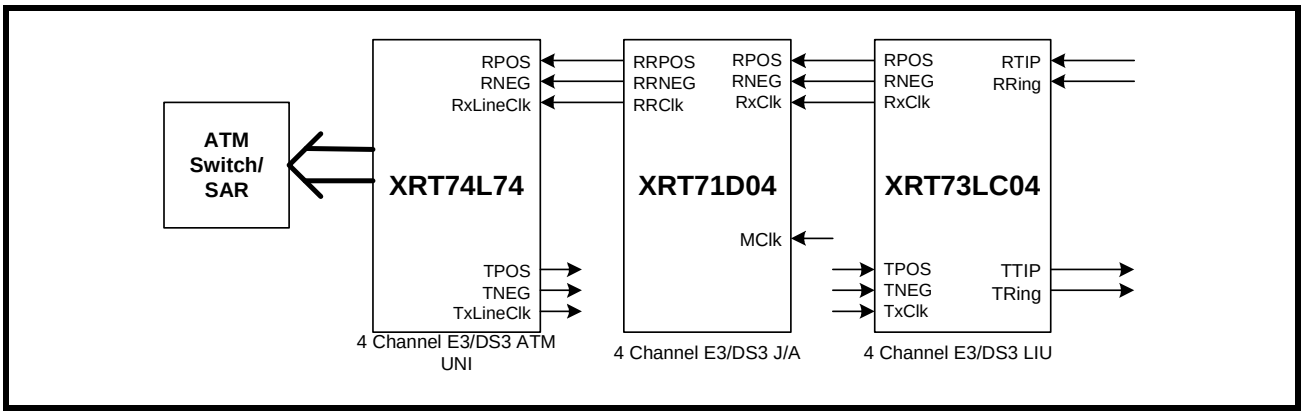
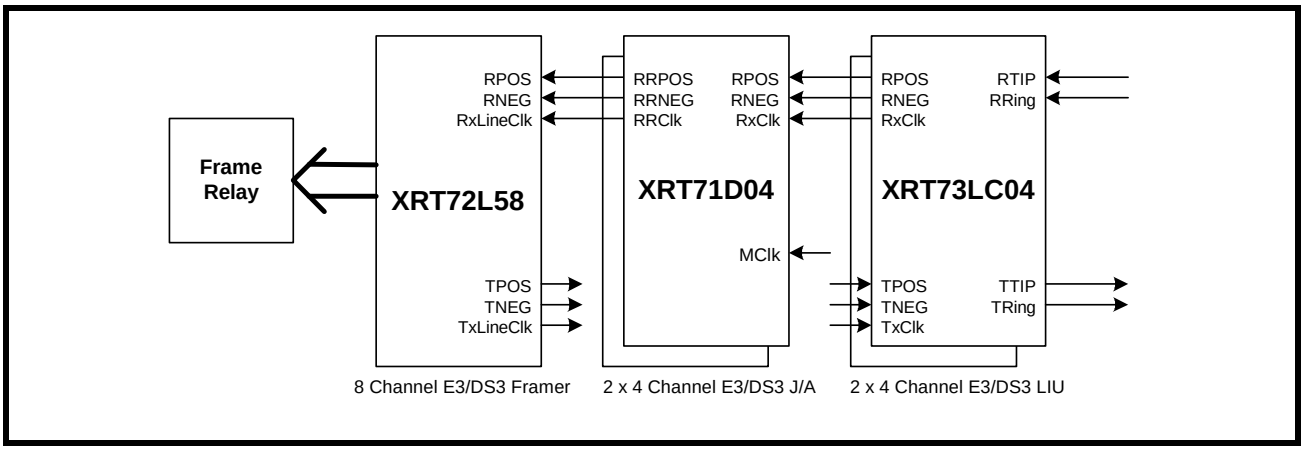


FIGURE 3. MULTISERVICE - FRAME RELAY APPLICATION



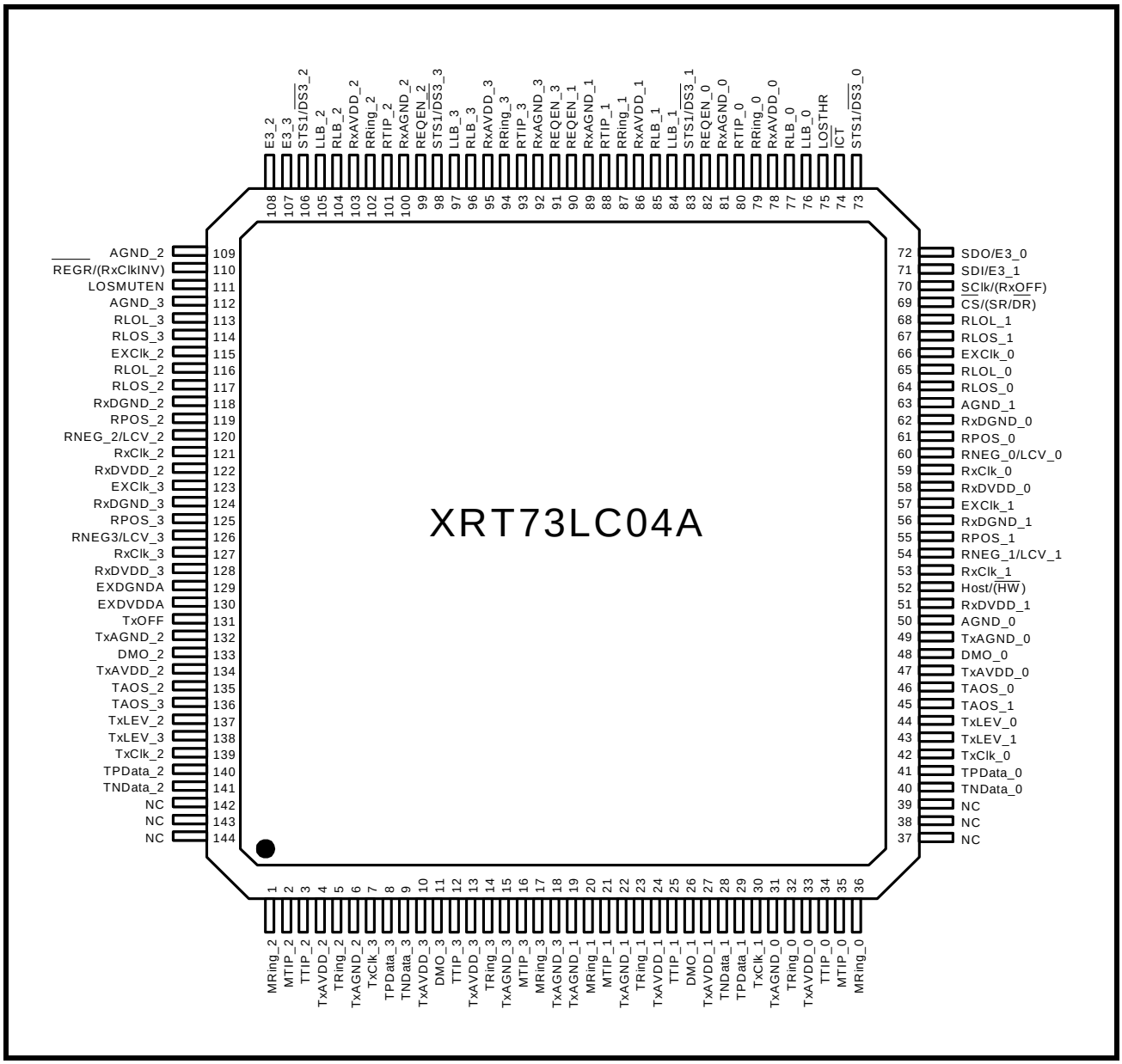
TRANSMIT INTERFACE CHARACTERISTICS:

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal from the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Contains Transmit Clock Duty Cycle Correction Circuit on-chip
- Generates pulses that comply with the ITU-T G.703 pulse template (E3 applications)
- Generates pulses that comply with the DSX-3 pulse template as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

RECEIVE INTERFACE CHARACTERISTICS:

- Integrated Adaptive Receive Equalization (optional) and Timing Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements (E3 and DS3 applications)
- Meets Jitter Tolerance Requirements as specified in ITU-T G.823_1993 (E3 Applications)
- Meets Jitter Tolerance Requirements as specified in Bellcore GR-499-CORE (DS3 Applications)
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment
- Receiver can be powered down in order to conserve power in redundancy designs

FIGURE 4. PIN OUT OF THE XRT73LC04A IN THE 144 PIN TQFP PACKAGE



ORDERING INFORMATION

PART #	PACKAGE	OPERATING TEMPERATURE RANGE
XRT73LC04AIV	144 Pin LQFP 20 X 20 X 1.4 mm	-40^{o}C to +85^{o}C

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PIN DESCRIPTIONS (BY FUNCTION)

TRANSMIT INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
34 25 3 12	TTIP_0 TTIP_1 TTIP_2 TTIP_3	O	**Transmit TTIP Output - Channel (n):** The XRT73LC04A uses this pin along with TRing_(n) to transmit a bipolar line signal via a 1:1 transformer.
32 23 5 14	TRing_0 TRing_1 TRing_2 TRing_3	O	**Transmit Ring Output - Channel (n):** The XRT73LC04A uses this pin along with TTIP_(n) to transmit a bipolar line signal via a 1:1 transformer.
42 30 139 7	TxClk_0 TxClk_1 TxClk_2 TxClk_3	I	**Transmit Clock Input for TPData and TNData - Channel (n):** This input pin must be driven at 34.368 MHz (for E3 applications), 44.736 MHz (for DS3 applications), or 51.84 MHz (for SONET STS-1 applications). The XRT73LC04A uses this signal to sample the TPData_(n) and TNData_(n) input pins. By default, the XRT73LC04A is configured to sample these two pins on the falling edge of this signal. ***NOTE:*** *If the XRT73LC04A is operating in the HOST Mode, then the device can be configured to sample the TPData_(n) and TNData_(n) input pins on either the rising or falling edge of TxClk_(n).*
41 29 140 8	TPData_0 TPData_1 TPData_2 TPData_3	I	**Transmit Positive Data Input - Channel (n)**: The XRT73LC04A samples this pin on the falling edge of TxClk_(n). If the device samples a "1", then it generates and transmits a positive polarity pulse to the line. The data should be applied to this input pin if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment. ***NOTE:*** *If the XRT73LC04A is operating in the HOST Mode, then the XRT73LC04A can be configured to sample the TPData_(n) pin on either the rising or falling edge of TxClk_(n).*
40 28 141 9	TNData_0 TNData_1 TNData_2 TNData_3	I	**Transmit Negative Data Input - Channel (n):** The XRT73LC04A samples this pin on the falling edge of TxClk_(n). If the device samples a "1", then it generates and transmits a negative polarity pulse to the line. In Single-Rail Mode, this pin must be tied to GND to enable the HDB3/B3ZS Encoder and Decoder, (internally pulled-down). In Dual-Rail Mode this input is the N-Rail Data input. ***NOTE:*** *If the XRT73LC04A is operating in the HOST Mode, then the XRT73LC04A can be configured to sample the TNData_(n) pin on either the rising or falling edge of TxClk_(n).*

TRANSMIT INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
44 43 137 138	TxLEV_0 TxLEV_1 TxLEV_2 TxLEV_3	I	**Transmit Line Build-Out Enable/Disable Select - Channel (n):** This input pin permits the Transmit Line Build-Out circuit, within Channel (n), to be enabled or disabled. In E3 mode, this pin has no effect on the transmit pulse shape. Setting this pin to "High" disables the Line Build-Out circuit. In this mode, Channel (n) outputs partially-shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins. Setting this pin to "Low" enables the Line Build-Out circuit within Channel (n). In this mode, Channel (n) outputs shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins. To comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-CORE or Bellcore GR-253-CORE: 1. Set this input pin to "1" if the cable length between the Cross-Connect and the transmit output of Channel (n) is greater than 225 feet. 2. Set this input pin to "0" if the cable length between the Cross-Connect and the transmit output of Channel (n) is less than 225 feet. This pin is active only if the following two conditions are true: a. The XRT73LC04A is configured to operate in either the DS3 or SONET STS-1 Modes. b. The XRT73LC04A is configured to operate in the Hardware Mode. ***NOTE:*** *This pin to should be tied to GND if the XRT73LC04A is going to be operating in the HOST Mode, (internally pulled-down).*
131	TxOFF	I	**Transmitter OFF Input:** Setting this input pin "High" turns off all of the Transmitter Sections. In this mode the TTIP and TRing outputs are tri-stated. ***NOTES:*** 1. *This input pin controls the TTIP and TRing outputs even when the XRT73LC04A is operating in the HOST Mode.* 2. *For HOST Mode Operation, this pin is tied to GND if the Transmitter is intended to be turned off via the Microprocessor Serial Interface.*

RECEIVE INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
59 53 121 127	RxClk_0 RxClk_1 RxClk_2 RxClk_3	O	**Receive Clock Output - Channel (n):** This output pin is the Recovered Clock signal from the incoming line signal for Channel (n). The Receive Section of Channel (n) outputs data via the RPOS_(n) and RNEG_(n) output pins on the rising edge of this clock signal. Configure the Receive Section of Channel (n) to update the data on the RPOS_(n) and RNEG_(n) output pins on the falling edge of RxClk_(n) by doing one of the following: **a. Operating in the Hardware Mode** Pull the RxClkINV pin to "High". **b. Operating in the HOST Mode** Write a "1" into the RxClkINV bit-field within the Command Register.
60 54 120 126	RNEG_0/LCV_0 RNEG_1/LCV_1 RNEG_2/LCV_2 RNEG_3/LCV_3	O	**Receive Negative Data Output - Channel (n):** The function of this pin is dependent on whether the 73L04A is in the Hardware or HOST Mode (HOST/$\overline{HW}$) and the condition of $\overline{CS}$/(SR/$\overline{DR}$). **a. Operating in the Hardware Mode** **Receive Negative Data:** Setting the $\overline{CS}$/(SR/$\overline{DR}$) pin "Low", (Dual-Rail operation) this output pin pulses "High" whenever Channel (n) has received a Negative Polarity pulse in the incoming line signal at the RTIP_(n) and RRing_(n) inputs. **Line Code Violation:** When $\overline{CS}$/(SR/$\overline{DR}$) is set "High", (Single-Rail operation), the B3ZS/HDB3 Encoder/Decoder is activated and the Line Code Violation signal is output on this pin. **b. Operating in the HOST Mode** **Receive Negative Data:** Writing a "0" to the (SR/$\overline{DR}$)_(n) bit in the command register configures channel(n) in the Dual-Rail Mode and activates RNEG_(n). Writing a "1" to (SR/$\overline{DR}$)_(n) bit of the Command Register configures the Single-Rail Mode and activates LCV_(n). *If the B3ZS/HDB3 Decoder is enabled then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.*
61 55 119 125	RPOS_0 RPOS_1 RPOS_2 RPOS_3	O	**Receive Positive Data Output - Channel (n):** The function of this pin is dependent on the setting of the $\overline{CS}$/(SR/$\overline{DR}$) pin. **Receive Positive Data** If $\overline{CS}$/(SR/$\overline{DR}$) is set "Low" (Dual-Rail Mode), this output pin pulses "High" whenever Channel (n) has received a Positive Polarity pulse in the incoming line signal at the RTIP_(n)/RRing_(n) inputs. **Data Output** If $\overline{CS}$/(SR/$\overline{DR}$) is set "High" (Single-Rail Mode), data is output on this pin. *If the B3ZS/HDB3 Decoder is enabled then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.*
79 87 102 94	RRing_0 RRing_1 RRing_2 RRing_3	I	**Receive Ring Input - Channel (n):** This input pin along with RTIP_(n) is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.

RECEIVE INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
80 88 101 93	RTIP_0 RTIP_1 RTIP_2 RTIP_3	I	**Receive TIP Input - Channel (n):** This input pin along with RRing_(n) is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
82 90 99 91	REQEN_0 REQEN_1 REQEN_2 REQEN_3	I	**Receive Equalization Enable Input - Channel (n):** Setting this input pin "High" enables the Internal Receive Equalizer within Channel (n). Setting this pin "Low" disables the Internal Receive Equalizer. The guidelines for enabling and disabling the Receive Equalizer are described in Section 3.2. ***NOTE:*** *This pin is ignored and should be tied to GND if the XRT73LC04A is going to be operating in the HOST Mode, (internally pulled-down).*
110	RxClkINV	I	**Invert RxClk_(n) Output - Select:** The function of this pin depends upon the mode of operation. **Hardware Mode - Invert RxClk Output Select:** Setting this input pin "High" configures the Receive Section of all Channels to invert their RxClk_(n) clock output signals. Setting this pin "Low" configures Channel(n) to output the recovered data via the RPOS_(n) and RNEG_(n) output pins on the rising edge of RxClk_(n). Setting this input pin "High" configures Channel (n) to output the recovered data via the RPOS_(n) and RNEG_(n) output pins on the falling edge of RxClk_(n). ***NOTE:*** *This pin is internally pulled "High".*

CLOCK INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
66 57 115 123	EXClk_0 EXClk_1 EXClk_2 EXClk_3	I	**External Reference Clock Input - Channel (n):** Apply a 34.368 MHz clock signal for E3 applications, a 44.736 MHz clock signal for DS3 applications or a 51.84 MHz clock signal for SONET STS-1 applications. The Channel (n) Clock Recovery PLL uses this signal as a Reference Signal for Declaring and Clearing the Receive Loss of Lock Alarm. The Clock recovery PLL also generates the exact clock for the LIU. It is permissible to use the same clock that drives the TxClk_(n) input pin. It is permissible to operate the four Channels at different data rates.

OPERATING MODE SELECT

PIN #	NAME	TYPE	DESCRIPTION
69	SR/$\overline{DR}$/$\overline{CS}$	I	**Microprocessor Serial Interface - Chip Select Input/Encoder-Decoder Disable Input:** The function of this pin depends upon whether the XRT73LC04A is operating in the HOST Mode or in the Hardware Mode. ***NOTE:*** *This pin is internally pulled "High".* **Hardware Mode - Receive Output Single-Rail/Dual-Rail Select:** In Hardware Mode, setting this pin “High” configures each of the four channels to operate in the Single-Rail Mode. When each of the four channels are configured to operate in the Single-Rail Mode, then the Receive Section of each channel will output data via the RPOS_(n) output pin. ***NOTE:*** *Tie the TNData_(n) input to GND to enable HDB3/B3ZS Encoding and Decoding.* Setting this pin “Low” configures each of the four channels to operate in the Dual-Rail Mode. When each of the four channels are configured to operate in the Dual-Rail Mode, then the Receive Section of each channel will output data via both the RPOS_(n) and RNEG_(n) output pins. ***NOTE:*** *This input pin functions as the $\overline{CS}$ input pin, if the XRT73LC04A device has been configured to operate in the HOST Mode.*
72 71 108 107	E3_0/SDO E3_1/SDI E3_2 E3_3	I/O I I I	**E3_Mode Select - Channel 0:** This pin has a dual function. In HOST mode, this pin functions as SDO. **E3_Mode Select - Channel 1** This pin has a dual function. In HOST mode,this pin functions as SDI. **E3_Mode Select - Channel 2** **E3_Mode Select - Channel 3** **Hardware Mode Operation - E3 Mode Select - Channel (n):** This input pin is used to configure Channel (n) of the XRT73LC04A to operate in the E3 or STS-1/DS3 Modes. Setting this input pin to "High" configures Channel (n) to operate in the E3 Mode. Setting it "Low" configures Channel (n) to operate in either the DS3 or STS-1 Modes, depending upon the state of the STS-1/$\overline{DS3}$_(n) input pin. ***NOTE:*** *This pin is internally pulled “Low” when XRT73LC04A is in the Hardware Mode.*
73 83 106 98	STS1/$\overline{DS3}$_0 STS1/$\overline{DS3}$_1 STS1/$\overline{DS3}$_2 STS1/$\overline{DS3}$_3	I	**STS-1/DS3 Select Input - Channel (n):** “High” for STS-1 and “Low” for DS3 Operation. The XRT73LC04A ignores this pin if the E3_(n) pin is set to "1". This input pin is ignored if the XRT73LC04A is operating in the HOST Mode. ***NOTE:*** *This pin should be tied to GND if the XRT73LC04A is going to be operating in the HOST Mode, (internally pulled-down).*

OPERATING MODE SELECT

PIN #	NAME	TYPE	DESCRIPTION
52	HOST/($\overline{HW}$)	I	**HOST-Hardware Mode Select:** This input pin is used to enable or disable the Microprocessor Serial Interface (e.g., consisting of the SDI, SDO, SClk, and $\overline{CS}$ pins). Setting this input pin "High" enables the Microprocessor Serial Interface (e.g. configures the XRT73LC04A to operate in the HOST Mode). In this mode, configure the XRT73LC04A via the Microprocessor Serial Interface. When the XRT73LC04A is operating in the HOST Mode, then it ignores the states of many of the discrete input pins. Setting this input pin "Low" disables the Microprocessor Serial Interface (e.g., configures the XRT73LC04A to operate in the Hardware Mode). In this mode, many of the external input control pins are functional. (Internally Pulled-up)

CONTROL AND ALARM INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
36 20 1 17	MRing_0 MRing_1 MRing_2 MRing_3	I	**Monitor Ring Input - Channel (n):** The bipolar line output signal from TRing_(n) can be connected to this pin via a 270-ohm resistor in order to check for line driver failure. This pin is internally pulled "High".
35 21 2 16	MTIP_0 MTIP_1 MTIP_2 MTIP_3	I	**Monitor Tip Input - Channel (n):** The bipolar line output signal from TTIP_(n) can be connected to this pin via a 270-ohm resistor in order to check for line driver failure. This pin is internally pulled "High".
48 26 133 11	DMO_0 DMO_1 DMO_2 DMO_3	O	**Drive Monitor Output - Channel (n):** If no transmitted AMI signal is present on MTIP_(n) and MRing_(n) input pins for 128±32 TxClk periods, then DMO_(n) toggles and remains "High" until the next AMI signal is detected.
46 45 135 136	TAOS_0 TAOS_1 TAOS_2 TAOS_3	I	**Transmit All Ones Select - Channel (n):** A "High" on this pin causes the Transmit Section, within Channel (n), to generate and transmit a continuous AMI all “1’s" pattern onto the line. The frequency of this "1’s" pattern is determined by TxClk_(n). This input pin is ignored if the XRT73LC04A is operating in the HOST Mode. ***NOTE:*** *This pin should be tied to GND if the XRT73LC04A is going to be operating in the HOST Mode, (internally pulled-down).*
64 67 117 114	RLOS_0 RLOS_1 RLOS_2 RLOS_3	O	**Receive Loss of Signal Output Indicator - Channel (n):** This output pin toggles "High" if Channel (n) has detected a Loss of Signal Condition in the incoming line signal. The criteria that the XRT73LC04A uses to declare an LOS Condition depends upon whether the device is operating in the E3 or STS-1/DS3 Mode.
65 68 116 113	RLOL_0 RLOL_1 RLOL_2 RLOL_3	O	**Receive Loss of Lock Output Indicator - Channel (n):** This output pin toggles "High" if Channel (n) has detected a Loss of Lock Condition. Channel (n) declares an LOL (Loss of Lock) condition if the recovered clock frequency deviates from the Reference Clock frequency (available at the EXClk_(n) input pin) by more than 0.5%.

CONTROL AND ALARM INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
60 54 120 126	RNEG_0/(LCV_0) RNEG_1/(LCV_1) RNEG_2/(LCV_2) RNEG_3/(LCV_3)	O	**Line Code Violation - Channel (n):** The function of this pin is dependent on whether the XRT73LC04A is in the Hardware or HOST Mode (HOST/$\overline{HW}$) and if $\overline{CS}$/(SR/$\overline{DR}$) is set "High". **Hardware Mode** **Line Code Violation:** When $\overline{CS}$/(SR/$\overline{DR}$) is set "High", (Single-Rail operation), the B3ZS/HDB3 Encoder/Decoder is activated and the Line Code Violation signal is output on this pin. **HOST Mode** **Receive Negative Data:** Writing a "1" to (SR/$\overline{DR}$)_(n) bit of the Command Register configures the Single-Rail Mode and activates LCV_(n). *If the B3ZS/HDB3 Decoder is enabled then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.*
74	$\overline{ICT}$	I	**In-Circuit Test Input**: Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. This pin should be set to "High" for normal operation. This pin is internally pulled "High".
75	LOSTHR	I	**Loss of Signal Threshold Control**: Forcing the LOSTHR pin to GND or VDD provides two settings. This pin must be set to a "High" or "Low" level upon power up and should not be changed during operation. This pin is only applicable during DS3 or STS-1 operations.
76 84 105 97	LLB_0 LLB_1 LLB_2 LLB_3	I	**Local Loop-back - Channel (n)**: This input pin along with RLB_(n) dictates which Loop-Back mode Channel (n) is operating in. A "High" on this pin with RLB_(n) set to "Low" configures Channel (n) to operate in the Analog Local Loop-Back Mode. A "High" on this pin with RLB_(n) also being set to "High" configures Channel (n) to operate in the Digital Local Loop-Back Mode. ***NOTE:*** *This pin is ignored and should be tied to GND if the XRT73LC04A is going to be operating in the HOST Mode.*
77 85 104 96	RLB_0 RLB_1 RLB_2 RLB_3	I	**Remote Loop-Back - Channel (n):** This input pin in conjunction with LLB_(n) dictates which Loop-Back mode Channel (n) is operating in. A "High" on this pin with LLB_(n) being set to "Low" configures Channel (n) to operate in the Remote Loop-Back Mode. A "High" on this pin with LLB_(n) also being set to "High" configures Channel (n) to operate in the Digital Local Loop-Back Mode. ***NOTE:*** *This pin is ignored and should be tied to GND if the XRT73LC04A is going to be operating in the HOST Mode.*

CONTROL AND ALARM INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
111	LOSMUTEN	I	**MUTE-upon-LOS Enable Input (Hardware Mode):** This input pin is use to configure the XRT73LC04A, while it is operating in the Hardware Mode, to MUTE the recovered data via the RPOS_(n), RNEG_(n) output pins whenever one of the Channels declares an LOS conditions. Setting this input pin “High" configures all Channels to automatically pull the RPOS_(n) and RNEG_(n) output pins “Low” whenever it is declaring an LOS condition, thereby MUTing the data being output to the Terminal Equipment. Setting this input pin "Low" configures all Channels to NOT automatically MUTE the recovered data whenever an LOS condition is declared. ***NOTES:*** 1. *This pin is ignored and should be tied to GND if the XRT73LC04A is going to be operating in the HOST Mode.* 2. *This pin is internally pulled "Low".*

MICROPROCESSOR INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
69	$\overline{CS}$/ SR/$\overline{DR}$	I	**Microprocessor Serial Interface - Chip Select Input/Encoder-Decoder Disable Input:** The function of this pin depends upon whether the XRT73LC04A is operating in the HOST Mode or in the Hardware Mode. **HOST Mode Operation - Chip Select Input:** The Local Microprocessor must assert this pin to "0" in order to enable communication with the XRT73LC04A via the Microprocessor Serial Interface. ***NOTE:*** *This pin is internally pulled "High".*
70	SClk/(RxOFF)	I	**Microprocessor Serial Interface Clock Signal/Receiver Shut OFF Input:** The function of this pin depends upon: **HOST Mode - Microprocessor Serial Interface Clock Signal:** This signal is used to sample the data on the SDI pin on the rising edge of this signal. During Read operations the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. **Hardware Mode - Receiver Shut OFF input:** Setting this input pin "High" shuts off all of the Receiver Sections. Setting this input pin "Low" enables all of the Receive Sections for full operation.
71	SDI/E3_1	I	**Serial Data Input for the Microprocessor Serial Interface** This pin has a dual function. **HOST Mode:** To read or write data into the Command Registers over the Microprocessor Serial Interface, apply the Read/Write bit, the Address Values of the Command Registers and Data Value to be written during Write Operations to this pin. This input is sampled on the rising edge of the SClk pin.

MICROPROCESSOR INTERFACE

PIN #	NAME	TYPE	DESCRIPTION
72	SDO/E3_0	O	**Serial Data Output from the Microprocessor Serial Interface** The function of this pin depends upon the mode of operation. **HOST Mode Operation:** This pin serially outputs the contents of the specified Command Register during Read Operations. The data on this pin is updated on the falling edge of the SClk input signal. This pin is tri-stated upon completion of data transfer.
110	$\overline{\text{REGR}}$/ RxClkINV	I	**Register Reset Input (Invert RxClk_(n) Output - Select):** The function of this pin depends upon the mode of operation.In Hardware mode, this pin functions as RxClkINV. **HOST Mode - Register Reset Input:** Setting this input pin "Low" causes the XRT73LC04A to reset the contents of the Command Registers to their default settings and to its default operating configuration. ***NOTE:*** *This pin is internally pulled "High".*

POWER AND GROUND PINS

PIN #	NAME	TYPE	DESCRIPTION
4	TxAVDD_2	****	**Transmitter Analog Supply, 3.3V ± 5% - Channel(n)**
6	TxAGND_2	****	**Transmitter Analog Ground - Channel(n)**
10	TxAVDD_3	****	**Transmitter Analog Supply, 3.3V ± 5% - Channel(n)**
13	TxAVDD_3	****	**Transmitter Analog Supply, 3.3V ± 5% - Channel(n)**
15	TxAGND_3	****	**Transmitter Analog Ground - Channel(n)**
18	TxAGND_3	****	**Transmitter Analog Ground - Channel(n)**
19	TxAGND_1	****	**Transmitter Analog Ground - Channel(n)**
22	TxAGND_1	****	**Transmitter Analog Ground - Channel(n)**
24	TxAVDD_1	****	**Transmitter Analog Supply, 3.3V ± 5% - Channel(n)**
27	TxAVDD_1	****	**Transmitter Analog Supply, 3.3V ± 5% - Channel(n)**
31	TxAGND_0	****	**Transmitter Analog Ground - Channel(n)**
33	TxAVDD_0	****	**Transmitter Analog Supply, 3.3V ± 5% - Channel(n)**
47	TxAVDD_0	****	**Transmitter Analog Supply, 3.3V ± 5% - Channel(n)**
49	TxAGND_0	****	**Transmitter Analog Ground - Channel (n)**
50	AGND_0	****	**Analog Ground Pin - Channel (n)**
51	RxDVDD_1	****	**Receiver Digital Supply 3.3V ± 5% Channel (n)**
56	RxDGND_1	****	**Receiver Digital Ground - Channel(n)**
58	RxDVDD_0	****	**Receiver Digital Supply 3.3V ± 5% Channel (n)**
62	RxDGND_0	****	**Receiver Digital Ground - Channel(n)**
63	AGND_1	****	**Analog Ground Pin - Channel(n)**
78	RxAVDD_0	****	**Receiver Analog Supply 3.3V ± 5% - Channel (n)**
81	RxAGND_0	****	**Receiver Analog Ground - Channel (n)**
86	RxAVDD_1	****	**Receiver Analog Supply 3.3V ± 5% - Channel (n)**
89	RxAGND_1	****	**Receiver Analog Ground - Channel (n)**
92	RxAGND_3	****	**Receiver Analog Ground - Channel (n)**
95	RxAVDD_3	****	**Receiver Analog Supply 3.3V ± 5% - Channel (n)**
100	RxAGND_2	****	**Receiver Analog Ground - Channel (n)**
103	RxAVDD_2	****	**Receiver Analog Supply 3.3V ± 5% - Channel (n)**
109	AGND_2	****	**Analog Ground Pin - Channel (n)**
112	AGND_3	****	**Analog Ground Pin - Channel (n)**
118	RxDGND_2	****	**Receiver Digital Ground - Channel(n)**
122	RxDVDD_2	****	**Receiver Digital Supply 3.3V ± 5% - Channel (n)**

POWER AND GROUND PINS

PIN #	NAME	TYPE	DESCRIPTION
124	RxDGND_3	****	**Receiver Digital Ground - Channel(n)**
128	RxDVDD_3	****	**Receiver Digital Supply 3.3V ± 5% - Channel (n)**
129	EXDGNDA	****	**External Clock Digital Ground**
130	EXDVDDA	****	**External Clock Digital Supply**
132	TxAGND_2	****	**Transmitter Analog Ground - Channel (n)**
134	TxAVDD_2	****	**Transmitter Analog Supply 3.3V ± 5% - Channel(n)**

NO CONNECTION PINS

PIN #	NAME	TYPE	DESCRIPTION
37	NC		No connection
38	NC		No connection
39	NC		No connection
142	NC		No connection
143	NC		No connection
144	NC		No connection

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	- 65℃ to + 150℃
Operating Temperature	- 40℃ to + 85℃
Supply Voltage Range	-0.5V to +3.465V
Theta-JA	24°C/W
Theta-JC	5.5°C/W

NOTE: *The XRT73LC04A is assembled in a thermally enhanced package with an integral Copper Heat Slug. The Heat Slug is solder plated and is exposed on the bottom of the package and is electrically connected to the internal Ground connections of the device. This Heat Slug can be soldered to the mounting board if desired, but must be electrically isolated from any V_{DD} connections.*

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DC Electrical Characteristics					
DV_{DD}	Digital DC Supply Voltage	3.135	3.3	3.465	V
AV_{DD}	Analog DC Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply Current (Measured while Transmitting and Receiving all "1's")			500	mA
V_{IL}	Input Low Voltage *			0.8	V
V_{IH}	Input High Voltage *	2.0		5.0	V
V_{OL}	Output Low Voltage, IOUT = -4.0mA *			0.4	V
V_{OH}	Output High Voltage, IOUT = 4.0mA *	2.8			V
I_L	Input Leakage Current *			±10	µA

NOTE: ** Not applicable to pins with pull-up or pull-down resistors.*

ELECTRICAL CHARACTERISTICS (CONTINUED) (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

AC ELECTRICAL CHARACTERISTICS (SEE FIGURE 5)					
TERMINAL SIDE TIMING PARAMETERS (SEE FIGURE 6 AND FIGURE 7) -- {(n) = 0, 1, 2 OR 3 }					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
	TxClk_(n) Clock Duty Cycle (STS-1/DS3)	30	50	70	%
	TxClk_(n) Clock Duty Cycle (E3)	30	50	70	%
	TxClk_(n) Frequency (SONET STS-1)		51.84		MHz
	TxClk_(n) Frequency (DS3)		44.736		MHz
	TxClk_(n) Frequency (E3)		34.368		MHz
t_{RTX}	TxClk_(n) Clock Rise Time (10% to 90%)		3	5	ns
t_{FTX}	TxClk_(n) Clock Fall Time (90% to 10%)		3	5	ns
t_{TSU}	TPData_(n)/TNData_(n) to TxClk_(n) Falling Set up time	3	1.5		ns
t_{THO}	TPData_(n)/TNData_(n) to TxClk_(n) Falling Hold time	3	1.5		ns
t_{LCVO}	RxClk_(n) to rising edge of LCV_(n) output delay		2.5		ns
t_{TDY}	TTIP_(n)/TRing_(n) to TxClk_(n) Rising Propagation Delay time		8		ns
	RxClk_(n) Clock Duty Cycle		50		%
	RxClk_(n) Frequency (SONET STS-1)		51.84		MHz
	RxClk_(n) Frequency (DS3)		44.736		MHz
	RxClk_(n) Frequency (E3)		34.368		MHz
t_{CO}	RxClk_(n) to RPOS_(n)/RNEG_(n) Delay Time	0	2.5		ns
t_{RRX}	RxClk_(n) Clock Rise Time (10% to 90%)		1.5		ns
t_{FRX}	RxClk_(n) Clock Fall Time (10% to 90%)		1.5		ns
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

NOTES:

1. *All XRT73LC04A digital inputs are designed to be TTL 5V compliant.*
2. *All XRT73LC04A digital outputs are also TTL 5V compliant. However, these outputs will not drive to 5V nor will they accept external 5V pull-ups.*

FIGURE 5. TRANSMIT PULSE AMPLITUDE TEST CIRCUIT FOR E3, DS3 AND STS-1 RATES (TYPICAL CHANNEL)

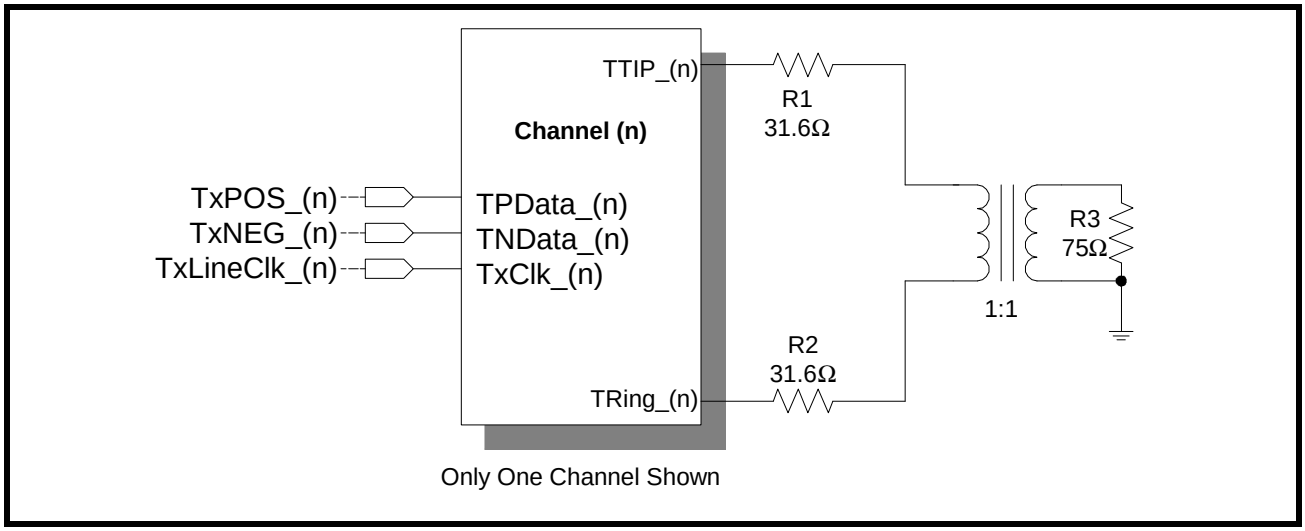


FIGURE 6. TIMING DIAGRAM OF THE TRANSMIT TERMINAL INPUT INTERFACE

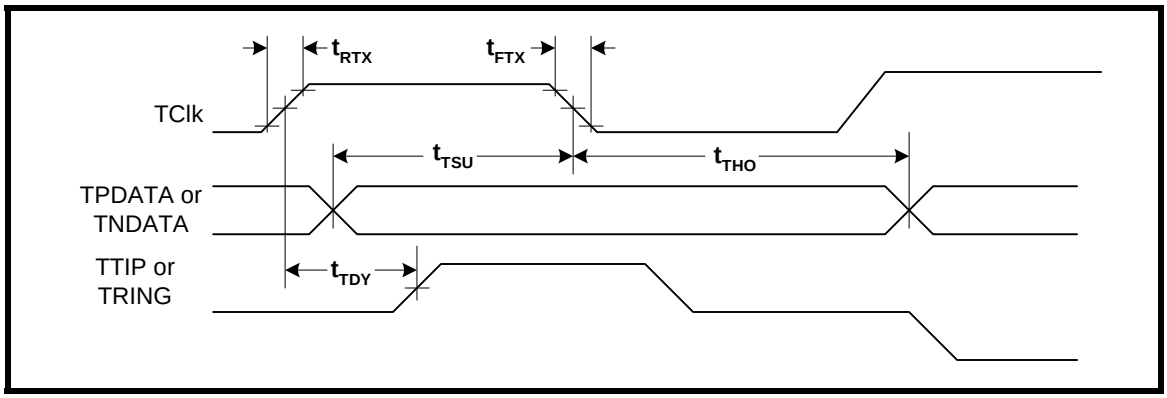
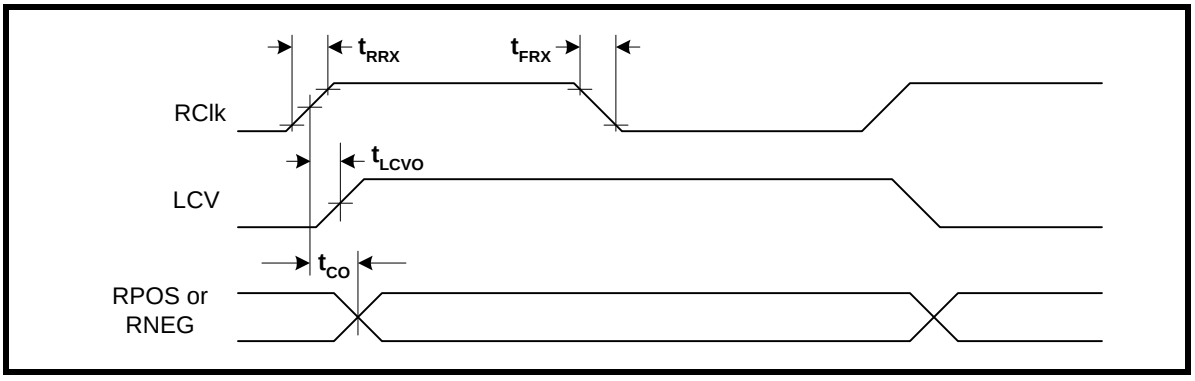


FIGURE 7. TIMING DIAGRAM OF THE RECEIVE TERMINAL OUTPUT INTERFACE



ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

LINE SIDE PARAMETERS E3 APPLICATION					
TRANSMIT CHARACTERISTICS (SEE FIGURE 5)					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
	Transmit Output Pulse Amplitude (Measured at Secondary Output of Transformer)	0.90	1.00	1.10	Vpk
	Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
	Transmit Output Pulse Width	12.5	14.55	16.5	ns
	Transmit Output Pulse Width Ratio	0.95	1.00	1.05	
	Transmit Output Jitter with jitter-free input @ TxClk_(n)		0.02	0.05	UIpp
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	1200	1400		feet
	Interference Margin	-20	-15		dB
	Signal Level to Declare Loss of Signal			-35	dB
	Signal Level to Clear Loss of Signal	-15			dB
	Occurrence of LOS to LOS Declaration Time	10		255	UI
	Termination of LOS to LOS Clearance Time	10		255	UI
	Intrinsic Jitter (all “1’s” pattern)		0.02		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1kHz	30			UI
	Jitter Tolerance @ Jitter Frequency = 10kHz	4			UI
	Jitter Tolerance @ Jitter Frequency = 800kHz	0.15	0.20		UI

ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

LINE SIDE PARAMETERS SONET STS-1 APPLICATION					
TRANSMIT CHARACTERISTICS (SEE FIGURE 5)					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
	Transmit Output Pulse Amplitude (Measured with TxLEV=0)	0.65	0.75	0.90	Vpk
	Transmit Output Pulse Amplitude (Measured with TxLEV=1)	0.90	1.00	1.10	Vpk
	Transmit Output Pulse Width	8.6	9.65	10.6	ns
	Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
	Transmit Output Jitter with jitter-free input @ TxClk_(n)		0.02	0.05	UI
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	900	1100		feet
	Signal Level to Declare or Clear Loss of Signal (See Table 5)				mV
	Intrinsic Jitter (all “1’s” pattern)		0.02		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1kHz	64			UI
	Jitter Tolerance @ Jitter Frequency = 10kHz	5			UI
	Jitter Tolerance @ Jitter Frequency = 400kHz	0.15	0.35		UI

ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

LINE SIDE PARAMETERS DS3 APPLICATION					
TRANSMIT CHARACTERISTICS (SEE FIGURE 5)					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
	Transmit Output Pulse Amplitude (Measured at 0 feet, TxLEV=0)	0.65	0.75	0.85	Vpk
	Transmit Output Pulse Amplitude (Measured at 0 feet, TxLEV=1)	0.90	1.00	1.10	Vpk
	Transmit Output Pulse Width	10.10	11.18	12.28	ns
	Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
	Transmit Output Jitter with jitter-free input @ TxClk_(n)		0.02	0.05	UI
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	900	1100		feet
	Signal Level to Declare or Clear Loss of Signal (See Table 5)				mV
	Intrinsic Jitter (all “1’s” pattern)		0.02		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1kHz	64			UI
	Jitter Tolerance @ Jitter Frequency = 10kHz	5			UI
	Jitter Tolerance @ Jitter Frequency = 300kHz (Cat II)	0.35	0.45		UI

Figure 8, Figure 9 and Figure 10 present the Pulse Template requirements for the E3, DS3 and STS-1 Rates.

FIGURE 8. ITU-T G.703 TRANSMIT OUTPUT PULSE TEMPLATE FOR E3 APPLICATIONS

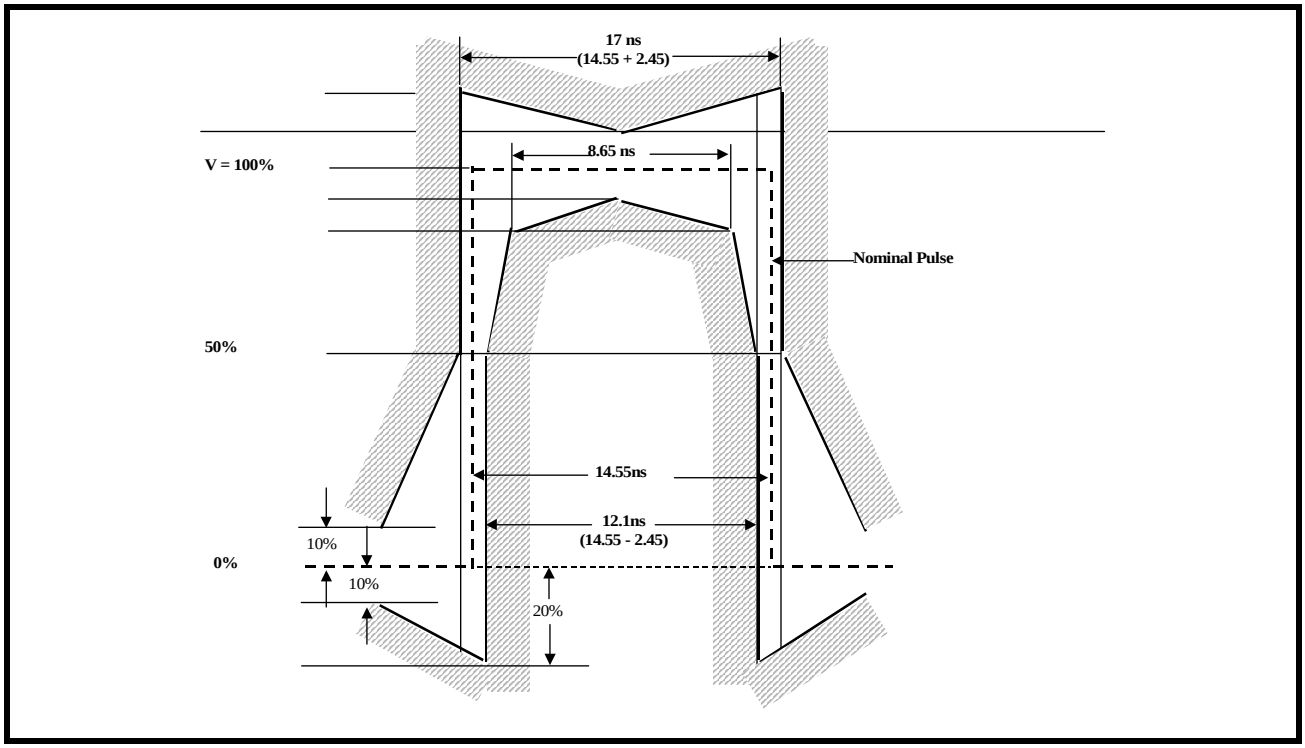


FIGURE 9. BELLCORE GR-499-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR DS3 APPLICATIONS

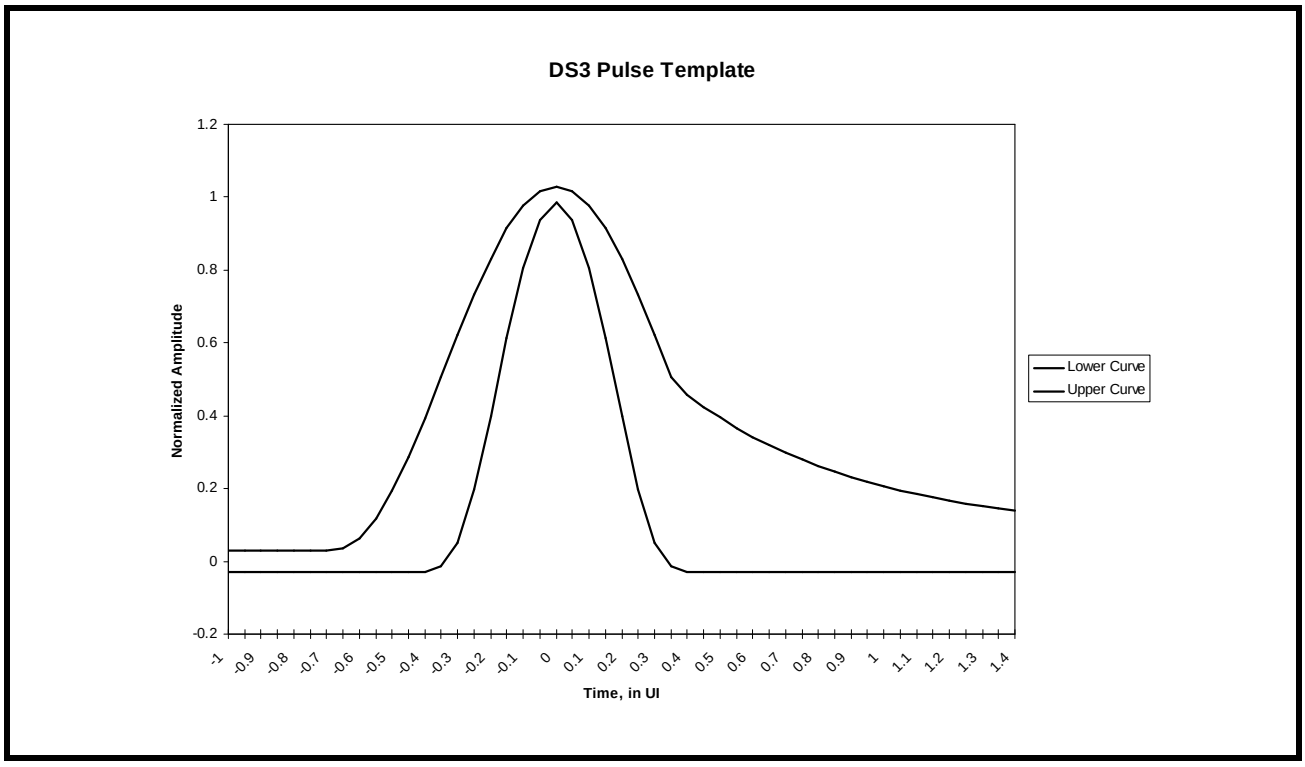


FIGURE 10. BELLCORE GR-253-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

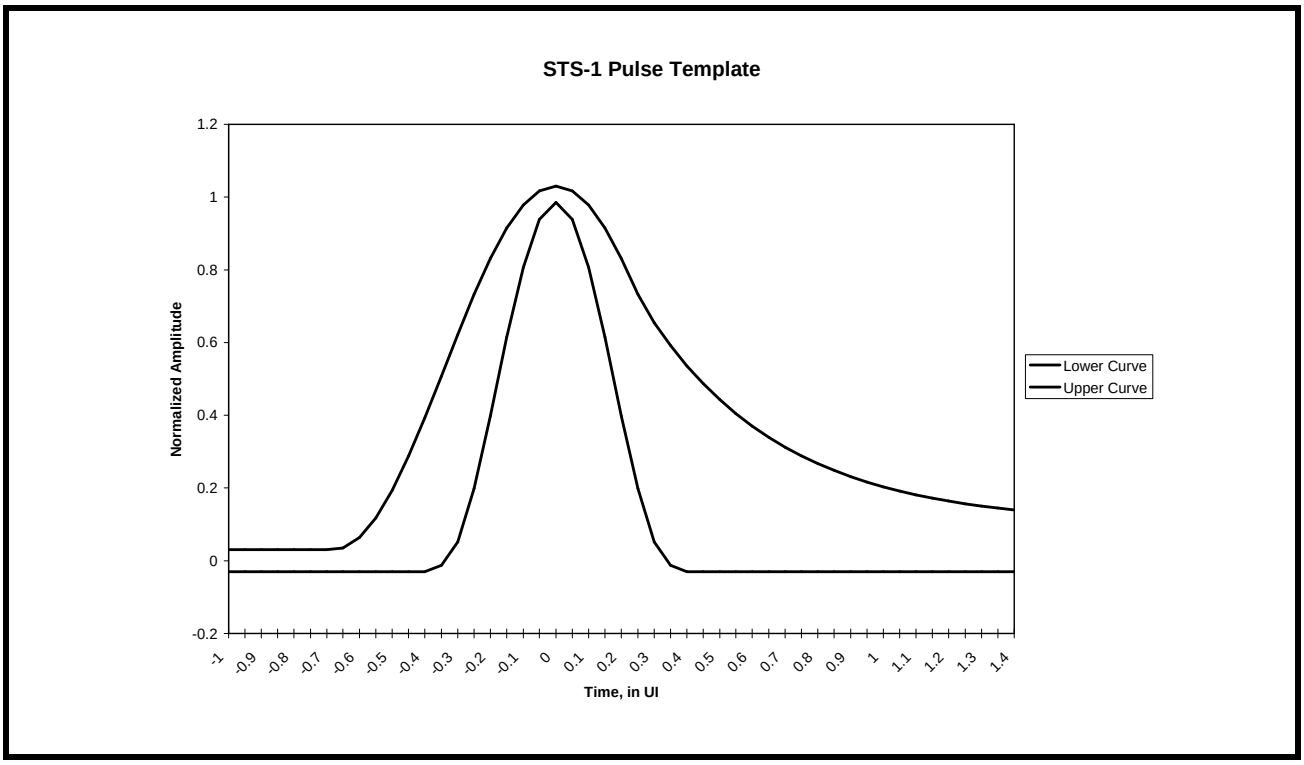
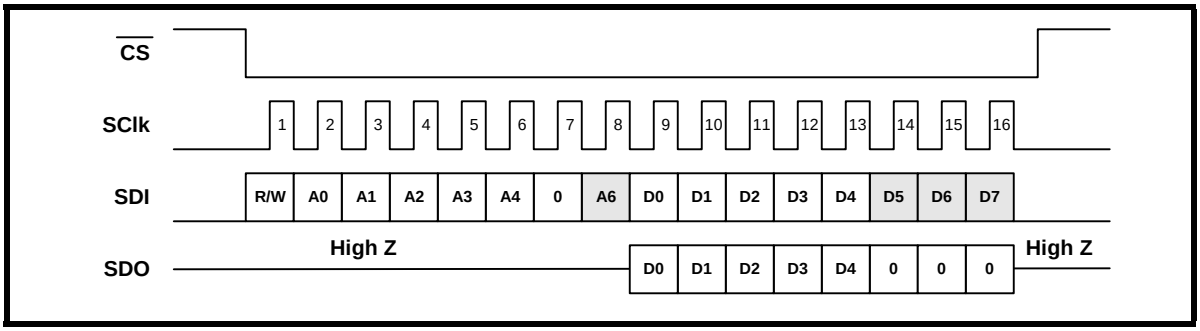


FIGURE 11. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



NOTES:

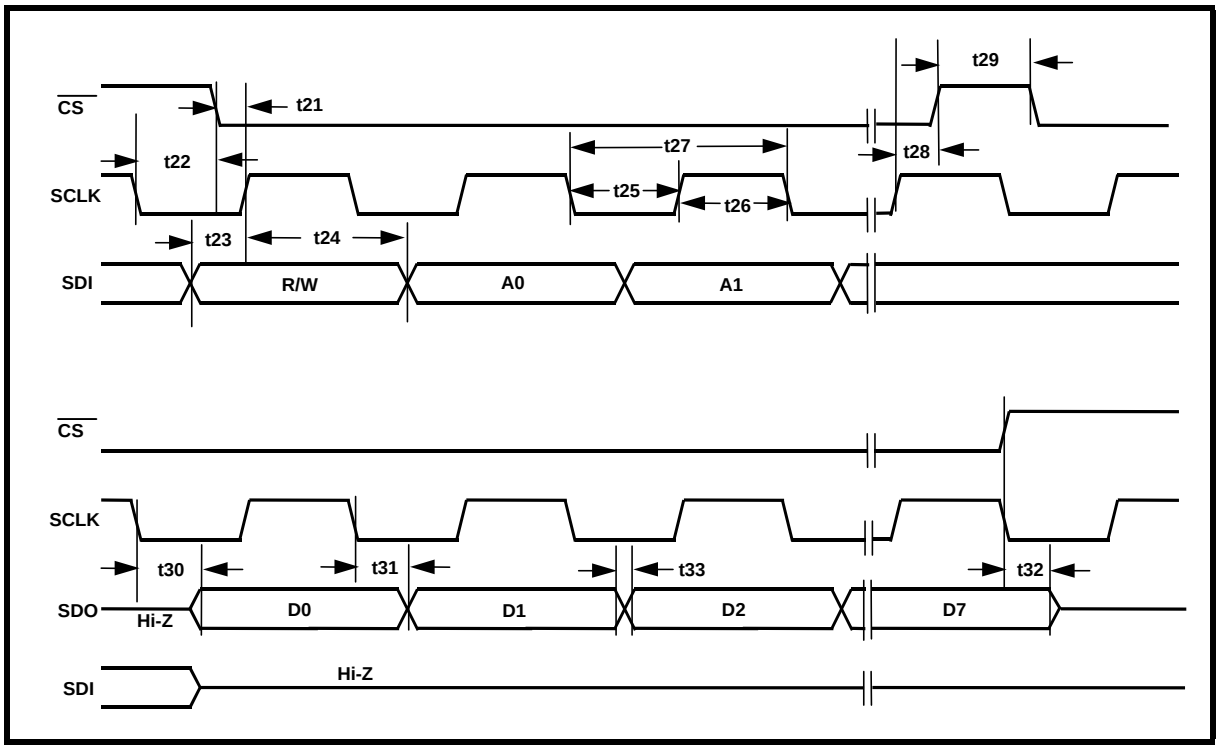
1. *A5 is always "0".*
2. *R/W = "1" for "Read" Operations*
3. *R/W = "0" for "Write" Operations*
4. *A shaded pulse, denotes a “don’t care” value.*

ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

MICROPROCESSOR SERIAL INTERFACE TIMING (SEE FIGURE 12)					
SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk Setup Time	5			ns
t_{22}	SCLK Falling Edge to $\overline{CS}$ Low Assertion Time	5			ns
t_{23}	SDI to Rising Edge of SClk Setup Time	5			ns
t_{24}	SDI to Rising Edge of SClk Hold Time	5			ns
t_{25}	SClk "Low" Time	65	80		ns
t_{26}	SClk "High" Time	65	80		ns
t_{27}	SClk Period	160			ns
t_{28}	$\overline{CS}$ Low to Rising Edge of SClk Hold Time	5			ns
t_{29}	$\overline{CS}$ "Inactive" Time	160			ns
t_{30}	Falling Edge of SClk to SDO Valid Time			80	ns
t_{31}	Falling Edge of SClk to SDO Invalid Time			65	ns
t_{32}	Rising edge of $\overline{CS}$ to High Z		100		ns
t_{33}	Rise/Fall time of SDO Output			20	ns

NOTE: *The load is 10pF*

FIGURE 12. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE



SYSTEM DESCRIPTION

A functional block diagram of the XRT73LC04A E3/DS3/STS-1 Transceiver IC is presented in Figure 13. The XRT73LC04A contains four separate channels with three distinct sections:

- The Transmit Section - Channels 0, 1, 2, and 3
- The Receive Section - Channels 0, 1, 2, and 3
- The Microprocessor Serial Interface Section

THE TRANSMIT SECTION - CHANNELS 0, 1, 2, AND 3

The Transmit Section, within each Channel, accepts TTL/CMOS level signals from the Terminal Equipment in either a Single-Rail or Dual-Rail format. The Transmit Section then takes this data and does the following:

- Encode this data into the B3ZS format if the DS3 or SONET STS-1 Modes has been selected or into the HDB3 format if the E3 Mode has been selected.
- Convert the CMOS level B3ZS or HDB3 encoded data into pulses with shapes that are compliant with the various industry standard pulse template requirements.
- Drive these pulses onto the line via the TTIP_(n) and TRing_(n) output pins across a 1:1 Transformer.

NOTE: *The Transmit Section drives a "1" (or a Mark) onto the line by driving either a positive or negative polarity pulse across the 1:1 Transformer within a given bit period. The Transmit Section drives a "0" (or a Space) onto the line by driving no pulse onto the line.*

THE RECEIVE SECTION - CHANNELS 0, 1, 2 AND 3

The Receive Section, within each Channel, receives a bipolar signal from the line via the RTIP and RRing signals through a 1:1 Transformer or 0.01µF Capacitor.

The recovered clock and data outputs to the Local Terminal Equipment in the form of CMOS level signals via the RPOS_(n), RNEG_(n) and RxClk_(n) output pins.

THE MICROPROCESSOR SERIAL INTERFACE

The XRT73LC04A can be configured to operate in either the Hardware Mode or the HOST Mode.

The XRT73LC04A contains four identical channels. The Microprocessor Interface Inputs are common to all channels. The descriptions that follow refer to Channel(n) where (n) represents channel 0, 1, 2 or 3.

a. Operating in the Hardware Mode

When the XRT73LC04A is operating in the Hardware Mode, then the following is true:

1. The Microprocessor Serial Interface block is disabled.
2. The XRT73LC04A is configured via input pin settings.

The XRT73LC04A can be configured to operate in the Hardware Mode by tying the HOST/($\overline{HW}$) input pin to GND.

Each of the pins associated with the Microprocessor Serial Interface takes on their alternative role as defined inTable 1.

TABLE 1: ROLE OF MICROPROCESSOR SERIAL INTERFACE PINS WHEN THE XRT73LC04A IS OPERATING IN THE HARDWARE MODE

PIN #	PIN NAME	FUNCTION, WHILE IN HARDWARE MODE
69	$\overline{CS}$/(SR/$\overline{DR}$)	(SR/$\overline{DR}$)
70	SClk/(RxOFF)	RxOFF
71	SDI/(E3_1)	E3_1
72	SDO/(E3_0)	E3_0
110	$\overline{REGR}$/(RxClkINV)	RxClkINV

When the XRT73LC04A is operating in the Hardware Mode, all of the remaining input pins become active.

b. Operating in the HOST Mode

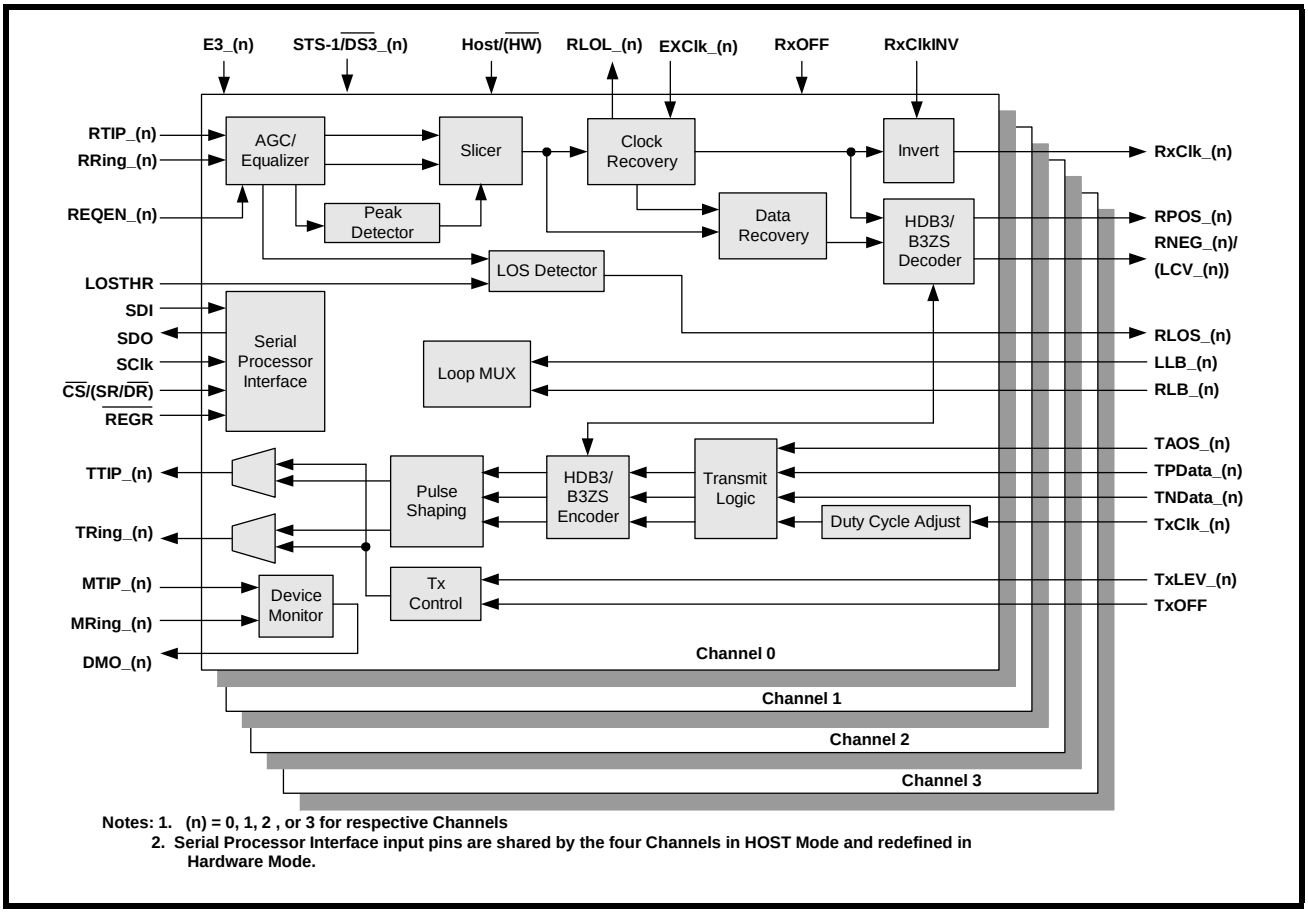
The XRT73LC04A can be configured to operate in the HOST Mode by tying the HOST/($\overline{HW}$) input pin to VDD.

When the XRT73LC04A is operating in the HOST Mode, then the following is true.

1. The Microprocessor Serial Interface block is enabled. Writing the appropriate data into the on-chip Command Registers makes many configuration selections.
2. All of the following input pins are disabled and should be connected to ground:
   - Pins 43, 44, 137 & 138 - TxLEV_(n)
   - Pins 45, 46, 135 & 136 TAOS_(n)
   - Pin 82, 90, 91 & 99 - REQEN_(n)
   - Pin 77, 85, 96 & 104 - RLB_(n)
   - Pin 76, 84, 97 & 105 - LLB_(n)
   - Pin 107 & 108 - E3_(n)
   - Pin 73, 83, 98 &106 - STS-1/$\overline{DS3}$_(n)

In HOST Mode Operation, the TxOFF input pins can be used to turn on or turn off the Transmit Output Drivers within all Channels concurrently. The intent behind this feature is to permit a system designed for redundancy to quickly switch out a defective line card and switch-in the back-up line card.

FIGURE 13. FUNCTIONAL BLOCK DIAGRAM OF THE XRT73LC04A



Notes: 1. (n) = 0, 1, 2 , or 3 for respective Channels
2. Serial Processor Interface input pins are shared by the four Channels in HOST Mode and redefined in Hardware Mode.

1.0 SELECTING THE DATA RATE

Each channel within the XRT73LC04A can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Further, each channel can be configured to operate in a mode/data rate that is independent of the other channels.

Two methods are available to select the data rate for each channel of the XRT73LC04A.

1.1 CONFIGURING CHANNEL(n)

For the following disscussion the reader should refer toTable 2 to determine the appropriate Address for each command register of each channel in the XRT73LC04A. The command register description refers to CR(x)-(n), where (x) = 0 to 7 and (n) refers to a particular channel of the XRT73LC04A.

TABLE 2: HEXADECIMAL ADDRESSES AND BIT FORMATS OF XRT73LC04A COMMAND REGISTERS

			REGISTER BIT-FORMAT				
ADDRESS	COMMAND REGISTER	TYPE	D4	D3	D2	D1	D0
CHANNEL 0							
0x00	CR0-0	RO	RLOL_0	RLOS_0	ALOS_0	DLOS_0	DMO_0
0x01	CR1-0	R/W	TxOFF_0	TAOS_0	TxClkINV_0	TxLEV_0	Reserved
0x02	CR2-0	R/W	Reserved	Reserved	ALOSDIS_0	DLOSDIS_0	REQEN_0
0x03	CR3-0	R/W	(SR/$\overline{DR}$)_0	LOSMUT_0	RxOFF	RxClk_0INV	Reserved
0x04	CR4-0	R/W	Reserved	STS-1/$\overline{DS3}$_0	E3_0	LLB_0	RLB_0
0x05	CR5-0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6-0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7-0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
CHANNEL 1							
0x08	CR0-1	RO	RLOL_1	RLOS_1	ALOS_1	DLOS_1	DMO_1
0x09	CR1-1	R/W	TxOFF_1	TAOS_1	TxClkINV_1	TxLEV_1	Reserved
0x0A	CR2-1	R/W	Reserved	Reserved	ALOSDIS_1	DLOSDIS_1	REQEN_1
0x0B	CR3-1	R/W	(SR/$\overline{DR}$)_1	LOSMUT_1	RxOFF	RxClk_1INV	Reserved
0x0C	CR4-1	R/W	Reserved	STS-1/$\overline{DS3}$_1	E3_1	LLB_1	RLB_1
0x0D	CR5-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0E	CR6-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0F	CR7-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
CHANNEL 2							
0x10	CR0-2	RO	RLOL_2	RLOS_2	ALOS_2	DLOS_2	DMO_2
0x11	CR1-2	R/W	TxOFF_2	TAOS_2	TxClkINV_2	TxLEV_2	Reserved
0x12	CR2-2	R/W	Reserved	Reserved	ALOSDIS_2	DLOSDIS_2	REQEN_2
0x13	CR3-2	R/W	(SR/$\overline{DR}$)_2	LOSMUT_2	RxOFF	RxClk_2INV	Reserved
0x14	CR4-2	R/W	Reserved	STS-1/$\overline{DS3}$_2	E3_2	LLB_2	RLB_2
0x15	CR5-2	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x16	CR6-2	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x17	CR7-2	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

TABLE 2: HEXADECIMAL ADDRESSES AND BIT FORMATS OF XRT73LC04A COMMAND REGISTERS

			REGISTER BIT-FORMAT				
ADDRESS	**COMMAND REGISTER**	**TYPE**	**D4**	**D3**	**D2**	**D1**	**D0**
CHANNEL3							
0x18	CR0-3	RO	RLOL_3	RLOS_3	ALOS_3	DLOS_3	DMO_3
0x19	CR1-3	R/W	TxOFF_3	TAOS_3	TxClkINV_3	TxLEV_3	Reserved
0x1A	CR2-3	R/W	Reserved	Reserved	ALOSDIS_3	DLOSDIS_3	REQEN_3
0x1B	CR3-3	R/W	(SR/$\overline{DR}$)_3	LOSMUT_3	RxOFF	RxClk_3INV	Reserved
0x1C	CR4-3	R/W	Reserved	STS-1/$\overline{DS3}$_3	E3_3	LLB_3	RLB_3
0x1D	CR5-3	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x1E	CR6-3	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x1F	CR7-3	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

Address:

The register addresses are presented in the **Hexadecimal** format.

Type:

The Command Registers are either Read-Only (RO) type of registers or Read/Write (R/W) type of registers.

The default value for each of the bit-fields within these registers is "0".

a. Operating in the Hardware Mode.

In order to configure individual Channels into the appropriate mode, set the E3_(n), and the STS-1/$\overline{DS3}$_(n) input pins (where n = 0, 1, 2, or 3) to the appropriate logic states, as presented below inTable 3.

TABLE 3: SELECTING THE DATA RATE FOR CHANNEL(n) VIA THE E3_(n) AND STS-1/$\overline{DS3}$_(n) INPUT PINS (HARDWARE MODE)

DATA RATE	STATE OF E3_(n) PIN	STATE OF STS-1/$\overline{DS3}$_(n) PIN	MODE OF B3ZS/HDB3 ENCODER/ DECODER BLOCKS
E3 (34.368 Mbps)	1	X (Don't Care)	HDB3
DS3 (44.736 Mbps)	0	0	B3ZS
STS-1 (51.84 Mbps)	0	1	B3ZS

b. Operating in the HOST Mode.

To configure a Channel into the appropriate mode, write the appropriate values into the STS-1/$\overline{DS3}$_(n) and E3_(n) bit-fields within the Command Register CR4-(n), as illustrated below (refer to Table 2 for the correct address for each channel).

COMMAND REGISTER, CR4-(n)

D4	D3	D2	D1	D0
X	STS-1/($\overline{DS3}$)_(n))	E3_(n)	LLB_(n)	RLB_(n)
x	x	x	x	x

Table 4 relates the values of these two bit-fields to the selected data rates.

TABLE 4: SELECTING THE DATA RATE FOR CHANNEL(n) VIA THE STS-1/$\overline{DS3}$_(n) AND THE E3_(n) BIT-FIELDS WITHIN THE APPROPRIATE COMMAND REGISTER (HOST MODE)

SELECTED DATA RATE	STS-1/$\overline{DS3}$_(n) (D3)	E3_(n) (D2)
E3	X (Don't Care)	1
DS3	0	0
STS-1	1	0

2.0 THE TRANSMIT SECTION

Figure 13 indicates that the Transmit Section within each Channel of the XRT73LC04A consists of the following blocks:

- Transmit Logic Block
- TxClk_(n) Duty Cycle Adjust Block
- HDB3/(B3ZS) Encoder
- Pulse Shaping Block

The purpose of the Transmit Section is to take TTL/CMOS level data from the terminal equipment and encode it into a format such that it can:

1. Be efficiently transmitted over coaxial cable at E3, DS3, or STS-1 data rates.
2. Be reliably received by the Remote Terminal Equipment at the other end of the E3, DS3, or STS-1 data link.
3. Comply with the applicable pulse template requirements.

2.1 THE TRANSMIT LOGIC BLOCK

The purpose of the Transmit Logic Block is to accept either Dual-Rail or Single-Rail (e.g., a binary data stream) TTL/CMOS level data and timing information from the Terminal Equipment.

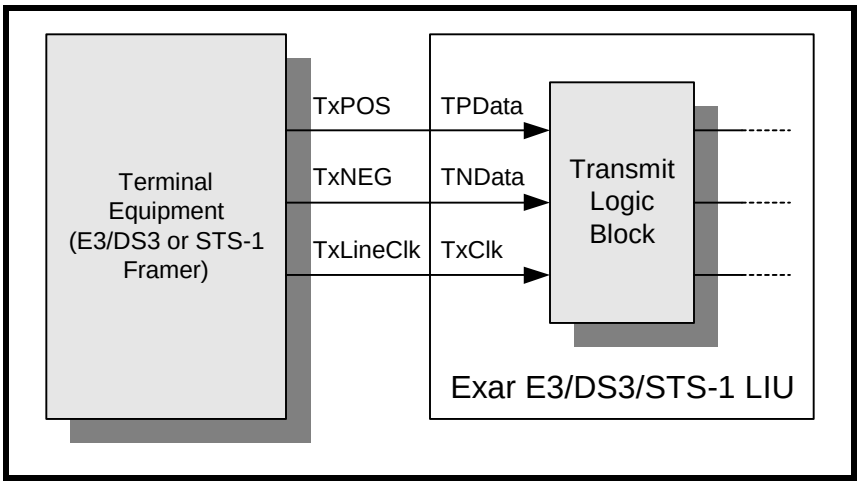
2.1.1 Accepting Dual-Rail Data from the Terminal Equipment

Whenever the XRT73LC04A accepts Dual-Rail data from the Terminal Equipment, it does so via the following input signals:

- TPData_(n)
- TNData_(n)
- TxClk_(n)

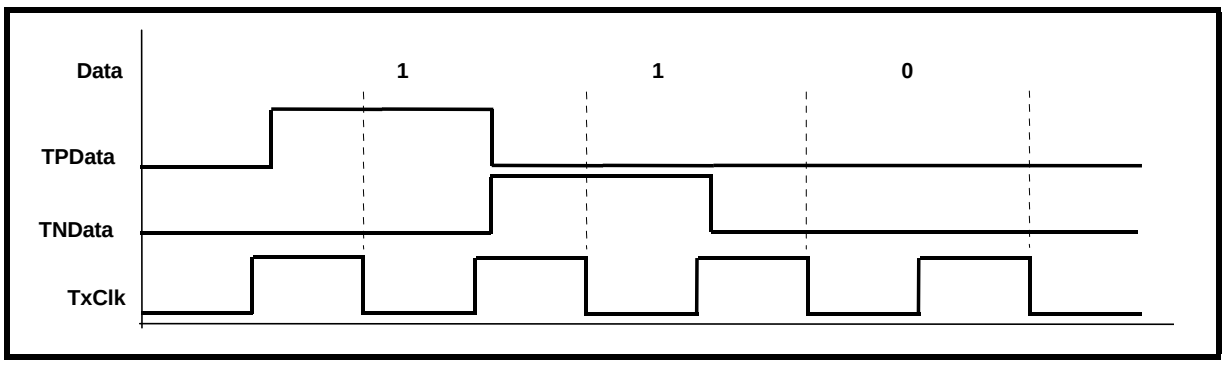
Figure 14 illustrates the typical interface for the transmission of data in a Dual-Rail Format between the Terminal Equipment and the Transmit Section of the XRT73LC04A.

FIGURE 14. THE TYPICAL INTERFACE FOR THE TRANSMISSION OF DATA IN A DUAL-RAIL FORMAT FROM THE TRANSMITTING TERMINAL EQUIPMENT TO THE TRANSMIT SECTION OF A CHANNEL



The manner that the LIU handles Dual-Rail data is described below and illustrated in Figure 15. The Transmit Section (of a Channel) typically samples the data on the TPData_(n) and TNData_(n) input pins on the falling edge of TxClk_(n).

FIGURE 15. THE XRT73LC04A SAMPLES THE DATA ON THE TPDATA AND TNDATA INPUT PINS



TxClk_(n) is the clock signal that is of the selected data rate frequency, E3 = 34.368 MHz, DS3 = 44.736 MHz and STS-1 = 51.84 MHz. If the Transmit Section samples a "1" on the TPData_(n) input pin, then the Transmit Section of the device generates a positive polarity pulse via the TTIP_(n) and TRing_(n) output pins across a 1:1 transformer. If the Transmit Section samples a "1" on the TNData_(n) input pin, then the Transmit Section of the device generates a negative polarity pulse via the TTIP_(n) and TRing_(n) output pins across a 1:1 transformer.

2.1.2 Accepting Single-Rail Data from the Terminal Equipment

To transmit data in a Single-Rail data from the Terminal Equipment, configure the XRT73LC04A in the HOST Mode.

To Configure Channel(n) to accept Single-Rail Data from the Terminal Equipment:

Write a "1" into the (SR/$\overline{DR}$)_(n) bit-field, within Command Register CR3-(n) shown below. (Please refer toTable 2 for the Address of the individual (n) channel.

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
(SR/$\overline{DR}$)_(n)	LOSMUT_(n)	RxOFF	RxClk_(n)INV	Reserved
1	x	x	x	x

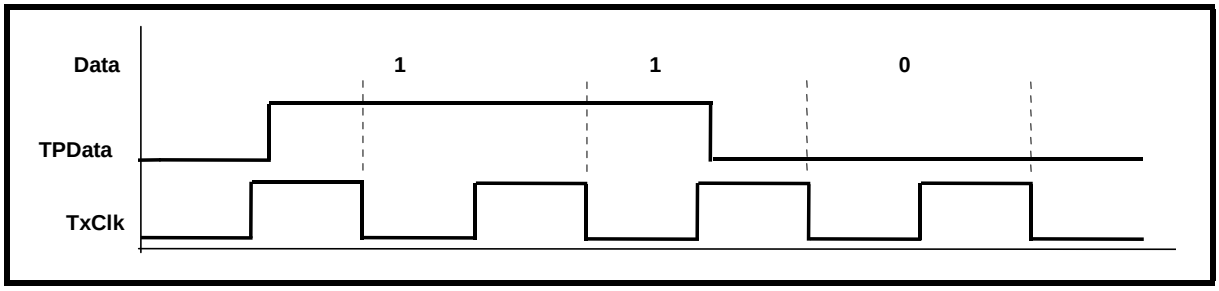
The Transmit Section (of each channel) samples this input pin on the falling edge of the TxClk_(n) clock signal and encodes this data into the appropriate bipolar line signal across the TTIP_(n) and TRing_(n) output pins.

NOTES:

1. *In this mode, the Transmit Logic Block ignores the TNData_(n) input pin.*
2. *If the Transmit Section of a given channel is configured to accept Single-Rail data from the Terminal Equipment, the B3ZS/HDB3 Encoder must be enabled.*

Figure 16 Illustrates the behavior of the TPData_(n) and TxClk_(n) signals when the Transmit Logic Block has been configured to accept Single-Rail data from the Terminal Equipment.

FIGURE 16. THE BEHAVIOR OF THE TPDATA AND TXCLK INPUT SGNALS, WHILE THE TRANSMIT LOGIC BLOCK IS ACCEPTING SINGLE-RAIL DATA FROM THE TERMINAL EQUIPMENT



2.2 THE TRANSMIT CLOCK DUTY CYCLE ADJUST CIRCUITRY

The on-chip Pulse-Shaping circuitry within the Transmit Section of each Channel in the XRT73LC04A generates pulses of the appropriate shapes and width to meet the applicable pulse template requirements. The widths of these output pulses are defined by the width of the half-period pulses within the TxClk_(n) signal.

However, if the widths of the pulses within the TxClk_(n) clock signal are allowed to vary significantly, this could jeopardize the chip's ability to generate Transmit Output pulses of the appropriate width and thereby not meet the Pulse Template requirement specification. Consequently, the chip's ability to generate compliant pulses could depend upon the duty cycle of the clock signal applied to the TxClk_(n) input pin.

The Transmit Clock Duty Cycle Adjust Circuitry accepts clock pulses via the TxClk_(n) input pin at duty cycles ranging from 30% to 70% and converts them to a 50% duty cycle.

2.3 THE HDB3/B3ZS ENCODER BLOCK

The purpose of the HDB3/B3ZS Encoder Block is to aid in the Clock Recovery process at the Remote Terminal Equipment by ensuring an upper limit on the number of consecutive zeros that can exist within the line signal.

2.3.1 B3ZS Encoding

If the XRT73LC04A has been configured to operate in the DS3 or SONET STS-1 Modes, then the HDB3/B3ZS Encoder blocks operate in the B3ZS Mode. When the Encoder is operating in this mode, it parses through and searches the Transmit Binary Data Stream from the Transmit Logic Block for the occur-

rence of three (3) consecutive zeros (e.g., "000"). If the B3ZS Encoder finds an occurrence of three consecutive zeros, then it substitutes these three "0's", with either a "00V" or a "B0V" pattern.

Where:

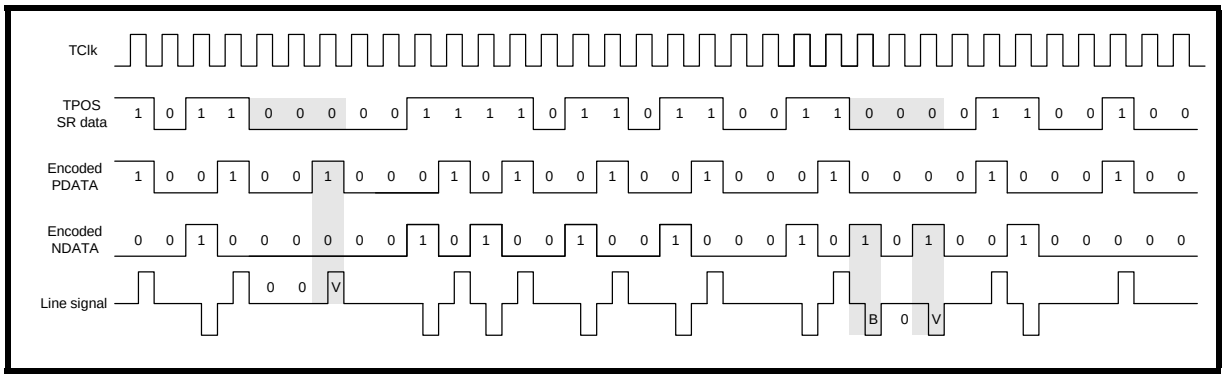
"B" represents a Bipolar pulse that is compliant with the Alternating Polarity requirements of the AMI (Alternate Mark Inversion) line code; and

"V" represents a Bipolar Violation (e.g., a bipolar pulse that violates the Alternating Polarity requirements of the AMI line code).

The B3ZS Encoder decides whether to substitute with either the "00V" or the "B0V" pattern in order to insure that an odd number of bipolar pulses exist between any two consecutive violation pulses.

Figure 17 illustrates the B3ZS Encoder at work with two separate strings of three (or more) consecutive zeros

FIGURE 17. AN EXAMPLE OF B3ZS ENCODING

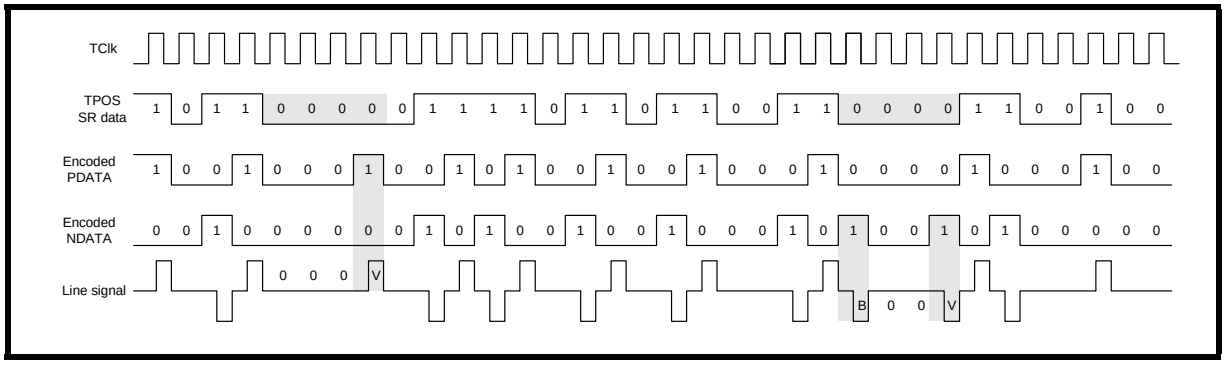


2.3.2 HDB3 Encoding

If the XRT73LC04A is configured to operate in the E3 Mode, then the HDB3/B3ZS Encoder blocks operate in the HDB3 Mode. When the Encoder is operating in this mode, it parses through and searches the Transmit Data Stream from the Transmit Logic Block for the occurrence of four (4) consecutive zeros (e.g., "0000"). If the HDB3 Encoder finds an occurrence of four consecutive zeros, then it substitutes these four "0's", with either a "000V" or a "B00V" pattern. The HDB3 Encoder decides whether to substitute with either the "000V" or the "B00V" pattern in order to insure that an odd number of bipolar pulses exist between any two consecutive violation pulses.

Figure 18 illustrates the HDB3 Encoder at work with two separate strings of four (or more) consecutive zeros.

FIGURE 18. AN EXAMPLE OF HDB3 ENCODING



2.3.3 Disabling the HDB3/B3ZS Encoder

The XRT73LC04A HDB3/B3ZS Encoder can be disabled by two methods.

a. Operating in the Hardware Mode.

The HBD3/B3ZS Encoder blocks within all channels are disabled by setting the $\overline{CS}$/(SR/$\overline{DR}$) input pin to "1".

NOTE: *By executing this step the HDB3/B3ZS Encoder and Decoder blocks in all channels of the XRT73LC04A are globally disabled.*

a. Operating in the HOST Mode.

When the XRT73LC04A is operating in the HOST Mode, then the HDB3/B3ZS Encoders within each channel can be individually enabled or disabled. Disable the HDB3/B3ZS Encoder block within Channel(n) by setting the (SR/$\overline{DR}$)_(n) bit-field within Command Register (CR3-(n)) to "1" as illustrated below.

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
(SR/$\overline{DR}$)_(n)	LOSMUT_(n)	RxOFF	RxClk_(n)INV	Reserved
1	X	X	X	X

NOTE: *This method can only be used if the XRT73LC04A is operating in the HOST Mode.*

If either of these methods are used to disable the HDB3/B3ZS Encoder, then the LIU transmits the data as received via the TPData_(n) and TNData_(n) input pins.

2.4 THE TRANSMIT PULSE SHAPING CIRCUITRY

The Transmit Pulse Shaper Circuitry consists of a Transmit Line Build-Out circuit which can be enabled or disabled by setting the TxLEV_(n) input pin or TxLEV_(n) bit-field to “High”or "Low". The purpose of the Transmit Line Build-Out circuit is to permit configuration of each channel to transmit an output pulse which is compliant to either of the following pulse template requirements when measured at the Digital Cross Connect System. Each of these Bellcore specifications state that the cable length between the Transmit Output and the Digital Cross Connect system can range anywhere from 0 to 450 feet.

The Isolated DSX-3 Pulse Template Requirement per Bellcore GR-499-CORE is illustrated in Figure 19 and the Isolated STSX-1 Pulse Template Requirement per Bellcore GR-253-CORE is illustrated in Figure 20.

FIGURE 19. THE BELLCORE GR-499-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR DS3 APPLICATIONS

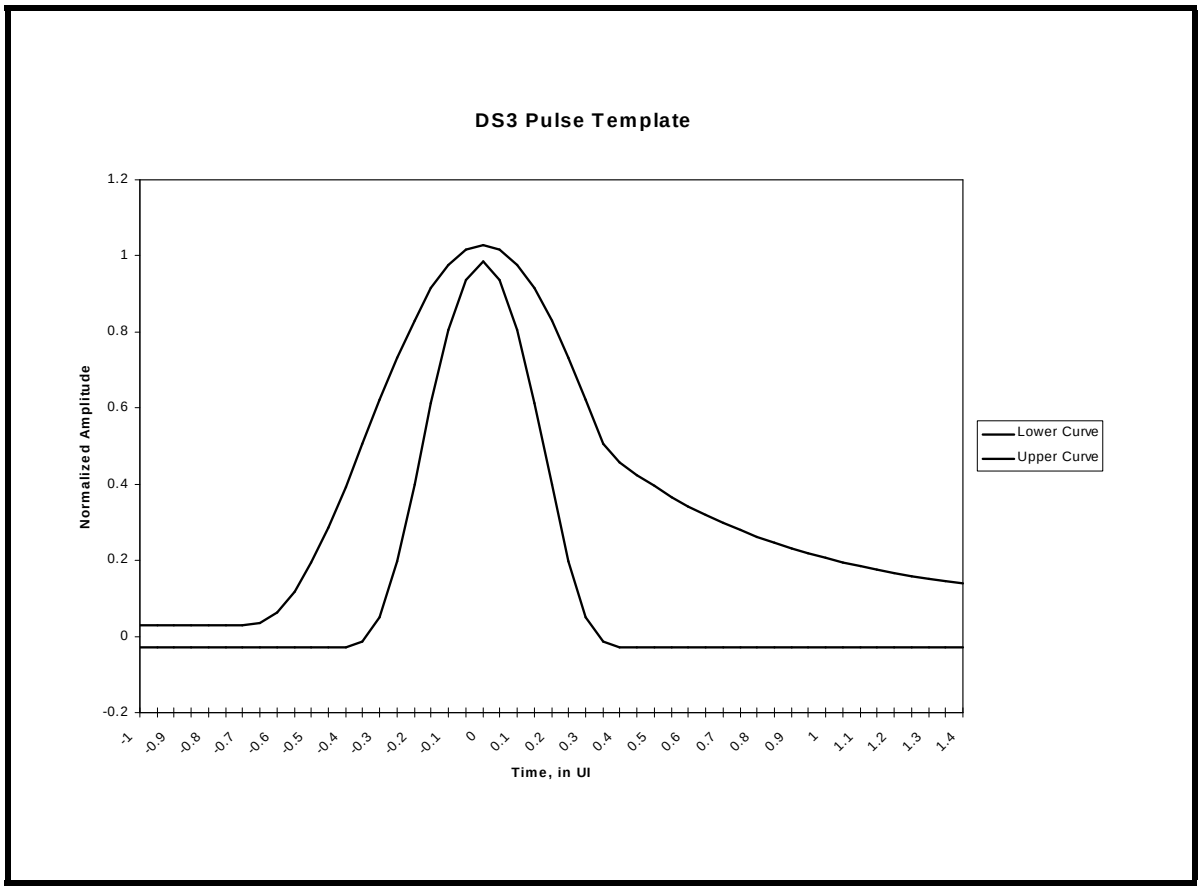
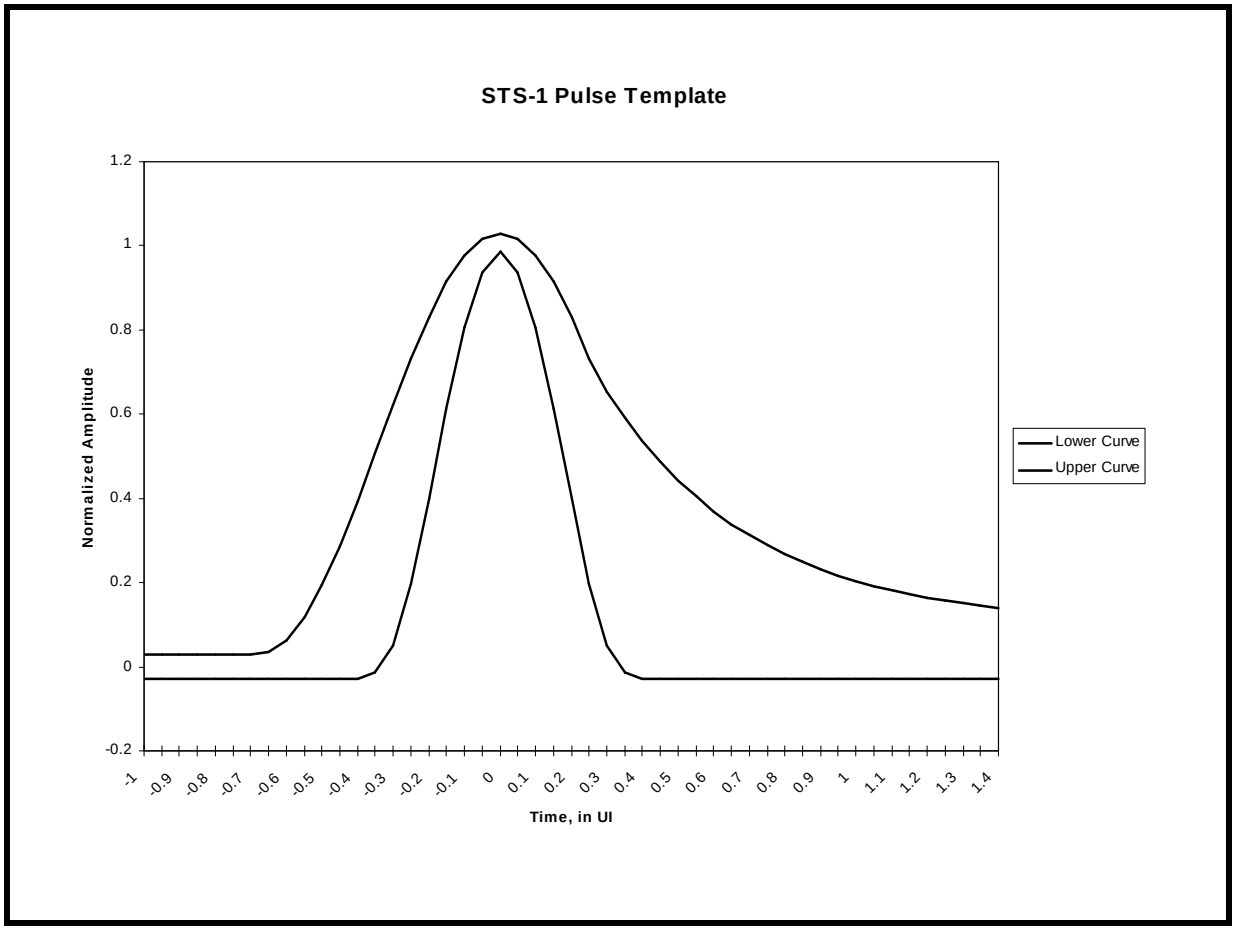


FIGURE 20. THE BELLCORE GR-253-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS



2.4.1 Enabling the Transmit Line Build-Out Circuit

If the Transmit Line Build-Out Circuit is enabled, then the Transmit Section of the Channel outputs shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins.

Enable the Transmit Line Build-Out circuit for each channel by doing the following:

a. Operating in the Hardware Mode

Set the TxLEV_(n) input pin to “Low".

b. Operating in the HOST Mode

Set the TxLEV_(n) bit-field to "0", as illustrated below.

COMMAND REGISTER, CR1-(n)

D4	D3	D2	D1	D0
TxOFF_(n)	TAOS_(n)	TxClkINV_(n)	TxLEV_(n)	Reserved
0	X	X	0	X

2.4.2 Disabling the Transmit Line Build-Out Circuit

If the Transmit Line Build-Out circuit is disabled, then the XRT73LC04A outputs partially shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins.

Disable the Transmit Line Build-Out circuit by doing the following:

a. Operating in the Hardware Mode

Set the TxLEV_(n) input pin to “High".

b. Operating in the HOST Mode

Set the TxLEV_(n) bit-field to "1" as illustrated below.

COMMAND REGISTER, CR1-(n)

D4	D3	D2	D1	D0
TxOFF_(n)	TAOS_(n)	TxClkINV_(n)	TxLEV_(n)	Reserved
0	X	X	1	X

2.4.3 Design Guideline for Setting the Transmit Line Build-Out Circuit

The TxLEV_(n) input pins or bit-fields should be set based upon the overall cable length between the Transmitting Terminal and the Digital Cross Connect system where the pulse template measurements are made.

If the cable length between the Transmitting Terminal and the DSX-3 or STSX-1 is less than 225 feet, enable the Transmit Line Build-Out circuit by setting the TxLEV_(n) input pin or bit-field to "0".

NOTE: *In this case, the configured channel outputs shaped (e.g., not square-wave) pulses onto the line via its TTIP_(n) and TRing_(n) output pins. The shape of this output pulse is such that it complies with the pulse template requirements even when subjected to cable loss ranging from 0 to 225 feet.*

If the cable length between the Transmitting Terminal and the DSX-3 or STSX-1 is greater than 225 feet, disable the Transmit Line Build-Out circuit by setting the TxLEV_(n) input pin or bit-field to "1".

NOTE: *In this case, the configured channel outputs partially shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins. The cable loss that these pulses experience over long cable lengths (e.g., greater than 225 feet) cause these pulses to be properly shaped and comply with the appropriate pulse template requirement.*

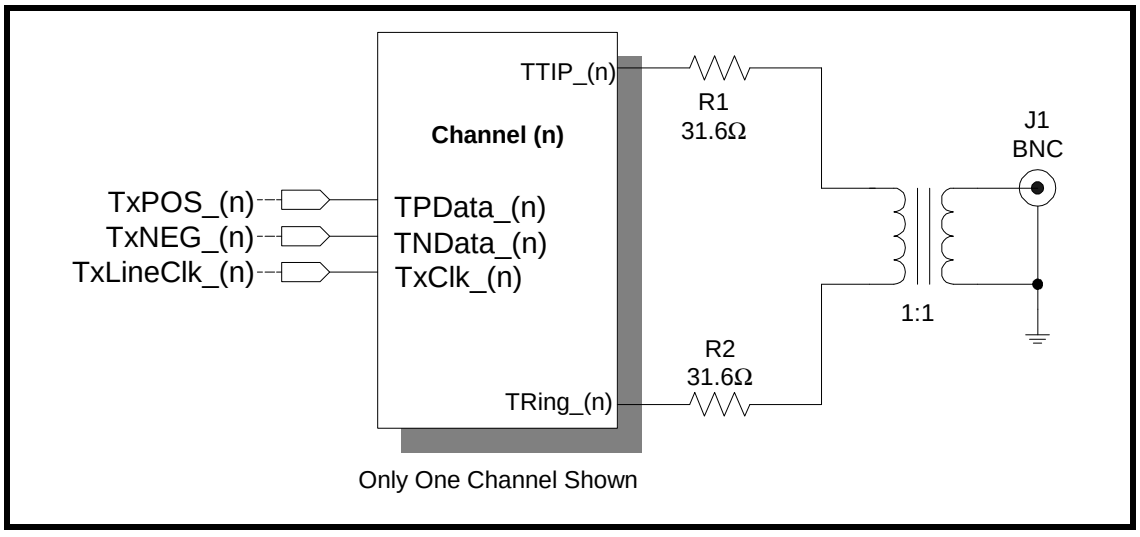
2.4.4 The Transmit Line Build-Out Circuit and E3 Applications

The ITU-T G.703 Pulse Template Requirements for E3 states that the E3 transmit output pulse should be measured at the Secondary Side of the Transmit Output Transformer for Pulse Template compliance. In other words, there is no Digital Cross Connect System pulse template requirement for E3. Consequently, the Transmit Line Build-Out circuit within a given Channel is disabled whenever that channel has been configured to operate in the E3 Mode.

2.5 INTERFACING THE TRANSMIT SECTIONS OF THE XRT73LC04A TO THE LINE

The E3, DS3 and SONET STS-1 specification documents all state that line signals transmitted over coaxial cable are to be terminated with 75 Ohm resistor. Interface the Transmit Section of the XRT73LC04A in the manner illustrated in Figure 21.

FIGURE 21. RECOMMENDED SCHEMATIC FOR INTERFACING THE TRANSMIT SECTION OF THE XRT73LC04A TO THE LINE



TRANSFORMER RECOMMENDATIONS

PARAMETER	VALUE
Turns Ratio	1:1
Primary Inductance	40µH
Isolation Voltage	1500Vrms
Leakage Inductance	0.6µH

PART NUMBER	VENDOR	INSULATION	PACKAGE TYPE
PE-68629	Pulse	3000V	Large Thru-Hole
PE-65966	Pulse	1500V	Small Thru-Hole
PE-65967	Pulse	1500V	Small SMT
T3001	Pulse	1500V	Small SMT
TG01-0406NS	Halo	1500V	Small SMT
TTI 7601-SM	Trans-Power	1500V	Small SMT

TRANSFORMER VENDOR INFORMATION

Pulse

Corporate Office

12220 World Trade Drive
San Diego, CA 92128
Tel: (858)-674-8100
FAX: (858)-674-8262

Europe

1 & 2 Huxley Road
The Surrey Research Park
Guildford, Surrey GU2 5RE
United Kingdom
Tel: 44-1483-401700
FAX: 44-1483-401701

Asia

150 Kampong Ampat
#07-01/02
KA Centre
Singapore 368324
Tel: 65-287-8998
FAX: 65-280-0080

Website: http://www.pulseeng.com

Halo Electronics

Corporate Office

P.O. Box 5826
Redwood City, CA 94063
Tel: (650)568-5800
FAX: (650)568-6165

Email: info@haloelectronics.com

Website: http://www.haloelectronics.com

Transpower Technologies, Inc.

Corporate Office

Park Center West Building
9805 Double R Blvd, Suite # 100
Reno, NV 89511
(800)500-5930 or (775)852-0140

Email: info@trans-power.com

Website: http://www.trans-power.com

3.0 THE RECEIVE SECTION

Figure 13 indicates the Receive Section consists of the following blocks:

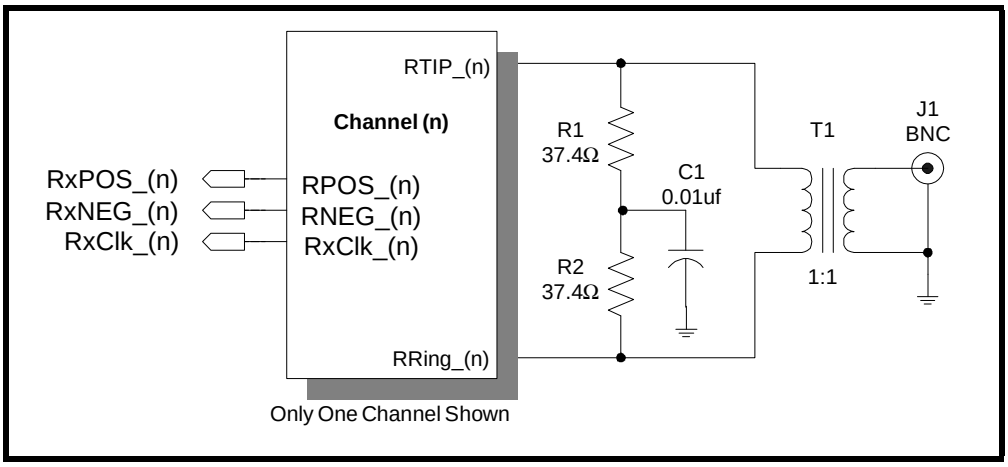
- AGC/Equalizer
- Peak Detector
- Slicer
- Clock Recovery PLL
- Data Recovery
- HDB3/B3ZS Decoder

The purpose of the Receive Section is to take an incoming attenuated/distorted bipolar signal from the line and encode it back into the TTL/CMOS format where it can be received and processed by the Terminal Equipment.

3.1 INTERFACING THE RECEIVE SECTIONS OF THE XRT73LC04A TO THE LINE

The design of the Receive Circuitry should be transformer-coupled to the Receive Section to the line. The specification documents for E3, DS3, and STS-1 all specify 75 Ohm termination loads when transmitting over coaxial cable. The recommended method to interface the Receive Section to the line in a manner is shown in Figure 22.

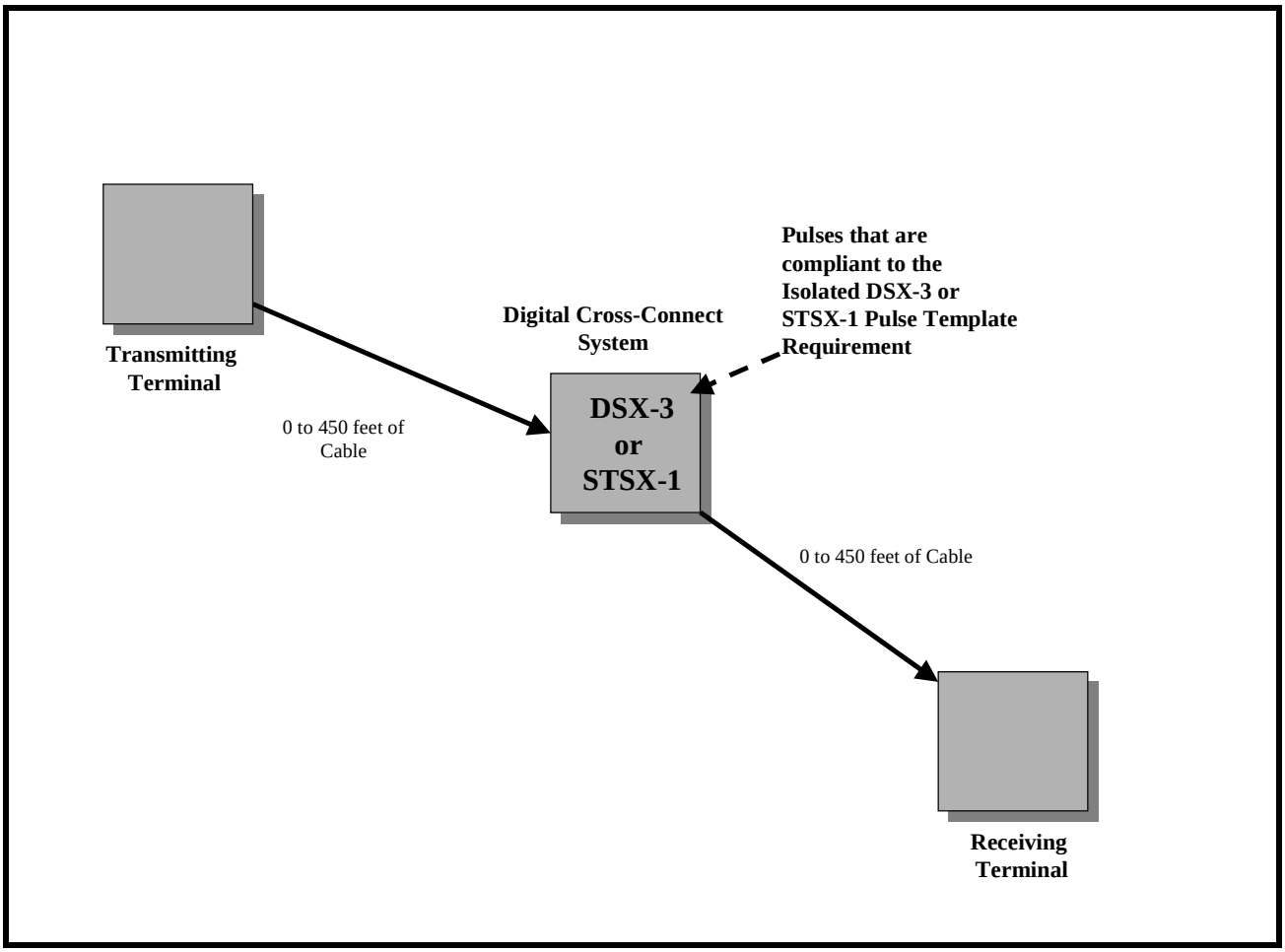
FIGURE 22. RECOMMENDED SCHEMATIC FOR INTERFACING THE RECEIVE SECTION OF THE XRT73LC04A TO THE LINE (TRANSFORMER-COUPLING)



3.2 THE RECEIVE EQUALIZER BLOCK

The purpose of this block is to equalize the incoming distorted signal due to cable loss. The Receive Equalizer attempts to restore the shape of the line signal so that the transmitted data and clock can be recovered reliably.

FIGURE 23. THE TYPICAL APPLICATION FOR THE SYSTEM INSTALLER



3.2.1 Guidelines for Setting the Receive Equalizer

This data sheet presents guidelines for setting the Receive Equalizer, for the following conditions.

1. If the overall cable length, from the local Receiving Terminal to the Remote Transmitting Terminal is NOT known.
2. If the overall cable length, from the Local Receiving Terminal to the remote Transmitting Terminal is known.

3.2.1.1 If the Overall Cable Length is NOT Known

This section presents recommendations on what state to set the Receive Equalizer when the overall cable-length, from the local Receiving Terminal to the remote Transmitting Terminal is NOT known. For DS3, STS-1 and E3 applications, enable the Receive Equalizer by setting either the REQEN_(n) input pin "high" or the REQEN_(n) bit-field to "1". The remainder of this section provides an explanation why we recommend enabling the Receive Equalizer for these applications.

3.2.1.1.1 The Use of the Receive Equalizer in a Typical DS3 or STS-1 Application

Most System Manufacturers of equipment supporting DS3 and STS-1 lines, interface their equipment to either a DSX-3 or STSX-1 Cross-Connect. While installing their equipment the Transmit Line Build-Out circuit is set to the proper setting that makes the transmit output pulse compliant with the Isolated DSX-3 or STSX-1 Pulse Template requirements. For the XRT73LC04A, this is achieved by setting the TXLEV_(n) input pin or bit-field to the appropriate level.

When the System Manufacturer is interfacing the Receive Section of the XRT73LC04A to the Cross-Connect, they should be aware of the following facts:

1. All DS3 or STS-1 line signals that are present at either the DSX-3 or the STSX-1 Cross Connect are required to meet the Isolated Pulse Template Requirements per Bellcore GR-499-CORE for DS3 applications, or Bellcore GR-253-CORE for STS-1 applications.
2. Bellcore documents state that the amplitude of these pulses at the DSX-3 or STSX-1 location can range in amplitude from 360mVpk to 850mVpk.

Bellcore documents stipulate that the Receiving Terminal must be able to receive the pulse template compliant line signal over a cable length of 0 to 450 feet from the DSX-3 or the STSX-1 Cross-Connect location.

These facts are reflected in Figure 23.

Design Considerations for DS3 and STS-1 Applications

When installing equipment into environments depicted in Figure 23, the system installation personnel may be able to determine the cable length between the local terminal equipment and the DSX-3/STSX-1 Cross-Connect Patch-Panel. The cable length between the local terminal equipment and the DSX-3/STSX-1 Cross-Connect Patch Panel ranges between 0 and 450 feet.

It is extremely unlikely that the system installation personnel will know the cable length between the DSX-3/STSX-1 Cross-Connect Patch-Panel and the remote terminal equipment. Therefore, we recommend that the Receive Equalizer be enabled by setting the REQEN_(n) input pin or bit-field to “1”.

The only time that the Receive Equalizer should be disabled is when there is an off-chip equilizer in the Receive path between the DSX-3/STSX-1 Cross-Connect and the RTIP_(n)/RRING_(n) input pins, or in applications where the Receiver is directly monitoring the transmit output signal directly.

3.2.1.2 Design Considerations for E3 Applications

In E3 System installation, it is recommended that the Receive Equalizer of the XRT73LC04A be enabled by pulling the REQEN_(n) input pins “High” or by setting the REQEN_(n) bit-fields to “1”.

NOTE: *The results of extensive testing indicates that when the Receive Equalizer is enabled, the XRT73LC04A is capable of receiving an E3 line signal with anywhere from 0 to 12dB of cable loss over the Industrial Temperature range.*

- **Design Considerations for E3 Applications or if the Overall Cable Length is known**

If during System Installation the overall cable length is known, then in order to optimize the performance of the XRT73LC04A in terms of receive intrinsic jitter, etc., enable or disable the Receive Equalizer based upon the following recommendations:

The Receive Equalizer should be turned ON if the Receive Section of a given channel is going to receive a line signal with an overall cable length of 300 feet or greater. Conversely, turn OFF the Receive Equalizer if the Receive Section of a given channel is going to receive a line signal over a cable length of less than 300 feet.

NOTES:

1. *If the Receive Equalizer block is turned ON when it is receiving a line signal over short cable length, the received line signal may be over-equalized which could degrade performance by increasing the amount of jitter that exists in the recovered data and clock signals or by creating bit-errors*
2. *The Receive Equalizer has been designed to counter the frequency-dependent cable loss that a line signal experiences as it travels from the transmitting terminal to the receiving terminal. However, the Receive Equalizer was not designed to counter flat loss where all of the Fourier frequency components within the line signal are subject to the same amount of attenuation. Flat loss is handled by the AGC block.*

Disable the Receive Equalizer block by doing either of the following.

a. Operating in the Hardware Mode

Setting the REQEN_(n) input pin “Low".

b. Operating in the HOST Mode

Writing a "0" to the REQEN_(n) bit-field within Command Register CR2, as illustrated below.

COMMAND REGISTER CR-2(n)

D4	D3	D2	D1	D0
Reserved	Reserved	ALOSDIS_(n)	DLOSDIS_(n)	REQEN_(n)
X	X	X	X	0

3.3 Clock Recovery PLL

The purpose of the Clock Recovery PLL is to track the incoming Dual-Rail data stream and to derive and generate a recovered clock signal.

It is important to note that the Clock Recovery PLL requires a line rate clock signal at the EXClk_(n) input pin.

The Clock Recovery PLL operates in one of two modes:

- The Training Mode.
- The Data/Clock Recovery Mode

3.3.1 The Training Mode

If a given channel is not receiving a line signal via the RTIP and RRing input pins, or if the frequency difference between the line signal and that applied via the EXClk_(n) input pin exceeds 0.5%, then the channel operates in the Training Mode. When the channel is operating in the Training Mode, it does the following:

a. Declare a Loss of Lock indication by toggling its respective RLOL_(n) output pin “High".

b. Output a clock signal via the RxClk_(n) output pins which is derived from the signal applied to the EXClk_(n) input pin.

3.3.2 The Data/Clock Recovery Mode

If the frequency difference between the line signal and that applied via the EXClk_(n) input pin is less than 0.5%, then the channel operates in the Data/Clock Recovery mode. In this mode, the Clock Recovery PLL locks onto the line signal via the RTIP and RRing input pins.

3.4 The HDB3/B3ZS Decoder

The Remote Transmitting Terminal typically encodes the line signal into some sort of Zero Suppression Line Code (e.g., HDB3 for E3, and B3ZS for DS3 and STS-1). The purpose of this encoding activity was to aid in the Clock Recovery process of this data within the Near-End Receiving Terminal. However, once the data has made it across the E3, DS3 or STS-1 Transport Medium and has been recovered by the Clock Recovery PLL, it is now necessary to restore the original content of the data. Hence, the purpose of the HDB3/B3ZS Decoding block is to restore the data transmitted over the E3, DS3 or STS-1 line to its original content prior to Zero Suppression Coding.

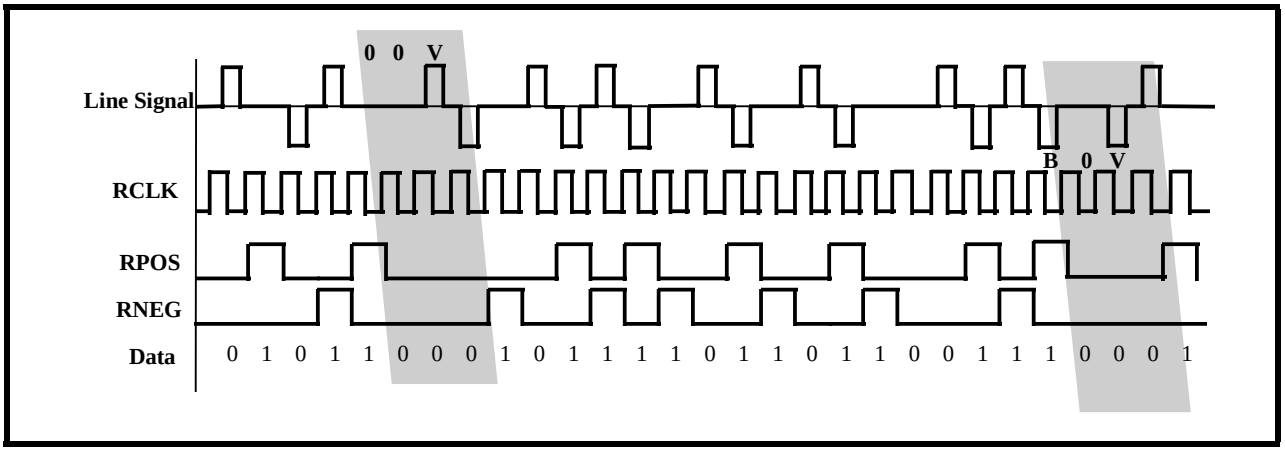
3.4.1 B3ZS Decoding (DS3/STS-1 Applications)

If the XRT73LC04A is configured to operate in the DS3 or STS-1 Modes, then the HDB3/B3ZS Decoding Blocks performs B3ZS Decoding. When the Decoders are operating in this mode, each of the Decoders parses through its respective incoming Dual-Rail data and checks for the occurrence of either a “00V" or a "B0V" pattern. If the B3ZS Decoder detects this particular pattern, then it substitutes these bits with a "000" pattern.

Note: *If the B3ZS Decoder detects any bipolar violations that is not in accordance with the B3ZS Line Code format, or if the B3ZS Decoder detects a string of 3 (or more) consecutive "0's" in the incoming line signal, then the B3ZS Decoder flags this event as a Line Code Violation by pulsing the LCV output pin “High".*

Figure 24 illustrates the B3ZS Decoder at work with two separate Zero Suppression patterns in the incoming Dual-Rail Data Stream.

Figure 24. An Example of B3ZS Decoding



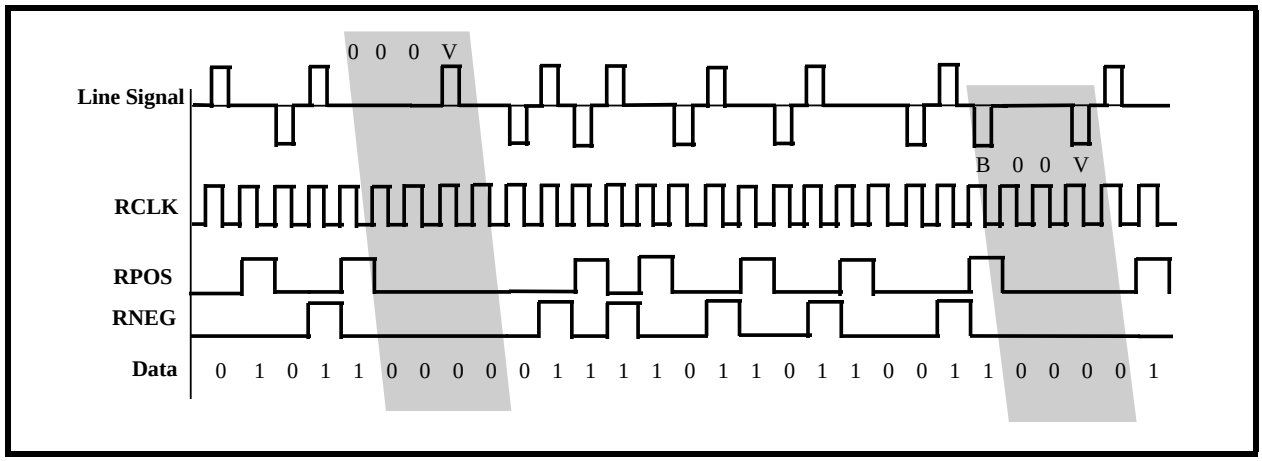
3.4.2 HDB3 Decoding (E3 Applications)

If the XRT73LC04A is configured to operate in the E3 Mode, then each of the HDB3/B3ZS Decoding Blocks performs HDB3 Decoding. When the Decoders are operating in this mode, they each parse through the incoming Dual-Rail data and check for the occurrence of either a "000V" or a "B00V" pattern. If the HDB3

Decoder detects this particular pattern, then it substitutes these bits with a “0000" pattern.

Figure 25 illustrates the HDB3 Decoder at work with two separate Zero Suppression patterns, in the incoming Dual-Rail Data Stream.

FIGURE 25. AN EXAMPLE OF HDB3 DECODING



NOTE: *If the HDB3 Decoder detects any bipolar violation (e.g., "V") pulses that is not in accordance with the HDB3 Line Code format, or if the HDB3 Decoder detects a string of 4 (or more) "0's" in the incoming line signal, then the HDB3 Decoder flags this event as a Line Code Violation by pulsing the LCV output pin “High".*

3.4.3 Configuring the HDB3/B3ZS Decoder

The XRT73LC04A can enable or disable the HDB3/B3ZS Decoder blocks by either of the following means.

a. Operating in the HOST Mode

Enable the HDB3/B3ZS Decoder block of Channel(n) by writing a "0" into the (SR/$\overline{DR}$)_(n) bit-field within Command Register CR3-(n), as illustrated below.

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
(SR/$\overline{DR}$)_(n)	LOSMUT_(n)	RxOFF	RxClk_(n)INV	Reserved
0	X	X	X	X

b. Operating in the Hardware Mode

To globally enable all HDB3/B3ZS Decoder blocks, pull the $\overline{CS}$/(SR/$\overline{DR}$)_(n) input pin "Low". To globally disable all HDB3/B3ZS Decoder blocks and configure the device to transmit and receive in an AMI format by pulling the $\overline{CS}$/(SR/$\overline{DR}$)_(n) input pin "High".

3.5 LOS DECLARATION/CLEARANCE

Each channel contains circuitry that monitors the following two parameters associated with the incoming line signals.

1. The amplitude of the incoming line signal via the RTIP and RRing inputs.
2. The number of pulses detected in the incoming line signal within a certain amount of time.

If a given channel determines that the incoming line signal is missing either due to insufficient amplitude or a lack of pulses in the incoming line signal, then it declares a Loss of Signal (LOS) condition. The channel declares the LOS condition by toggling its respective RLOS_(n) output pin “High" and by setting its corresponding RLOS_(n) bit field within Command Register 0 (or Command Register 8) to "1".

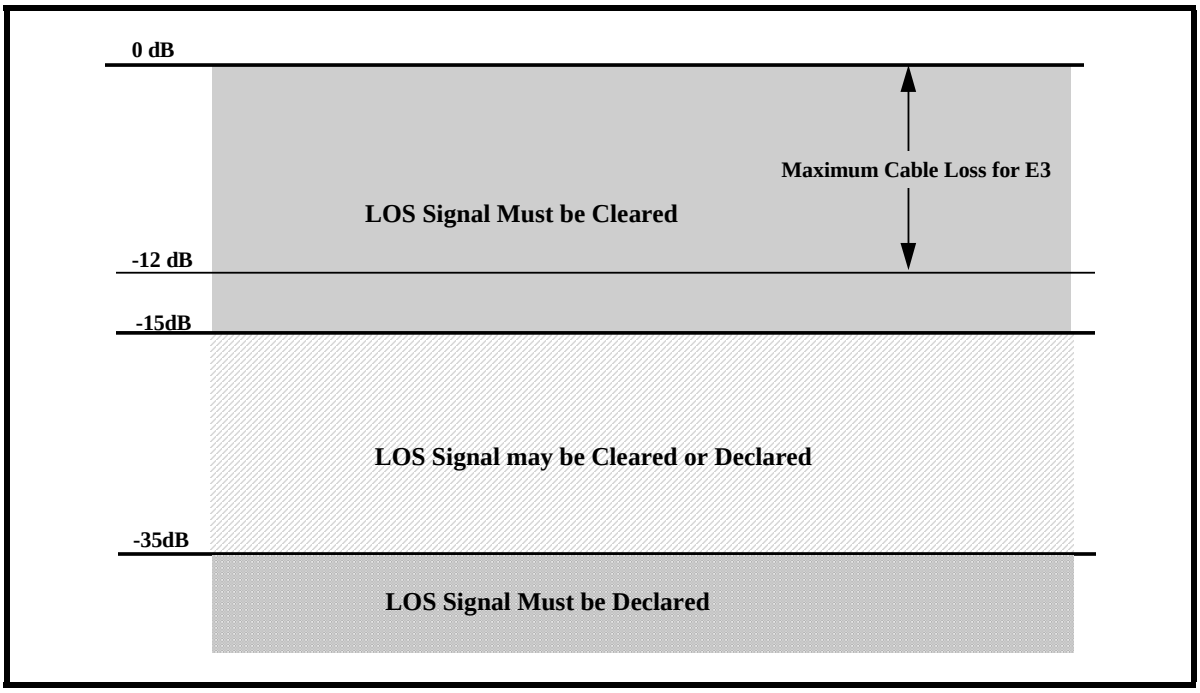
Conversely, if the channel determines that the incoming line signal has been restored (e.g., there is sufficient amplitude and pulses in the incoming line signal), then it clears the LOS condition by toggling its respective RLOS_(n) output pin “Low" and setting its corresponding RLOS_(n) bit-field to "0".

In general, the LOS Declaration/Clearance scheme that is employed in the XRT73LC04A is based upon ITU-T Recommendation G.775 for both E3 and DS3 applications.

3.5.1 The LOS Declaration/Clearance Criteria for E3 Applications

When the XRT73LC04A is operating in the E3 Mode, a given channel declares an LOS Condition if its receive line signal amplitude drops to -35dB or below. Further, the channel clears the LOS Condition if its receive line signal amplitude rises back to -15dB or above. Figure 26 illustrates the signal levels at which each channel of the XRT73LC04A declares and clears LOS.

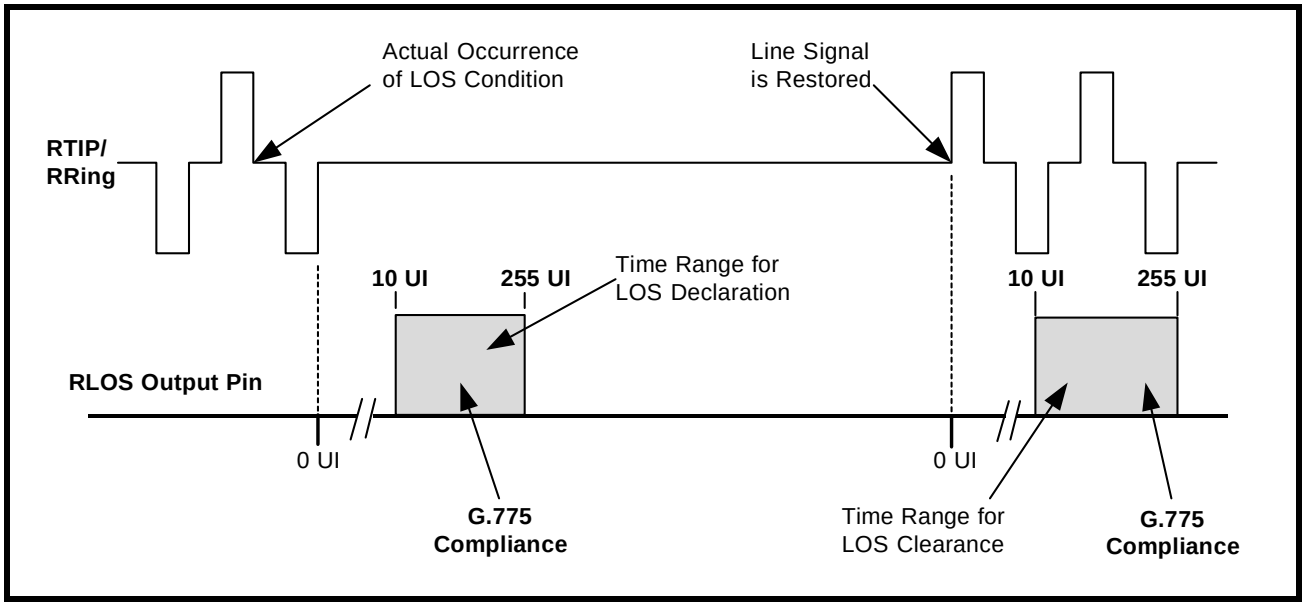
FIGURE 26. THE SIGNAL LEVELS THAT THE XRT73LC04A DECLARES AND CLEARS LOS



Timing Requirements associated with Declaring and Clearing the LOS Indicator

The XRT73LC04A was designed to meet the ITU-T G.775 specification timing requirements for declaring and clearing the LOS indicator. In particular, a channel declares an LOS between 10 and 255 UI (or E3 bit-periods) after the actual time the LOS condition occurred. Further, the channel clears the LOS indicator within 10 to 255 UI after restoration of the incoming line signal. Figure 27 illustrates the LOS Declaration and Clearance behavior in response to the Loss of Signal event and then the restoration of the signal.

FIGURE 27. THE BEHAVIOR OF THE LOS OUTPUT INDICATOR IN RESPONSE TO THE LOSS OF SIGNAL AND THE RESTORATION OF SIGNAL



3.5.2 The LOS Declaration/Clearance Criteria for DS3 and STS-1 Applications

When the XRT73LC04A is operating in the DS3 or STS-1 Mode, then each channel declares and clears LOS based upon the following two criteria.

- Analog LOS (ALOS) Declaration/Clearance Criteria
- Digital LOS (DLOS) Declaration/Clearance Criteria

In the DS3 Mode, the LOS output (RLOS) is simply the logical "OR" of the ALOS and DLOS states.

1. The Analog LOS (ALOS) Declaration/Clearance Criteria

A channel declares an Analog LOS (ALOS_(n)) Condition if the amplitude of the incoming line signal drops below a specific amplitude as defined by the voltage at the LOSTHR input pin, and whether the Receive Equalizer is enabled or not.

Table 5 presents the various voltage levels at the LOSTHR input pin, the state of the Receive Equalizer and the corresponding ALOS (Analog LOS) threshold amplitudes.

TABLE 5: THE ALOS (ANALOG LOS) DECLARE AND CLEAR THRESHOLDS FOR A GIVEN SETTING OF LOSTHR AND REQEN (DS3 AND STS-1 APPLICATIONS)

APPLICATION	REQEN SETTING	LOSTHR SETTING	SIGNAL LEVEL TO DECLARE ALOS	SGNAL LEVEL TO CLEAR ALOS
DS3	1	1	≤22mV	≥90mV
	0	1	≤17mV	≤70mV
STS-1	1	1	≤25mV	≥115mV
	0	1	≤20mV	≤90mV

Declaring ALOS

A channel(n) declares ALOS_(n) whenever the amplitude of the receive line signal falls below the Signal Level to Declare ALOS levels, as specified inTable 5.

Clearing ALOS_(n)

A channel(n) clears ALOS_(n) whenever the amplitude of the receive line signal increases above the Signal Level to Clear ALOS levels, as specified in Table 5.

There is approximately a 2dB hysteresis in the received signal level that exists between declaring and

clearing ALOS_(n) in order to prevent chattering in the RLOS_(n) output signal.

Monitoring the State of ALOS_(n)

If the XRT73LC04A is operating in the HOST Mode, the state of ALOS_(n) of Channel(n) can be polled or monitored by reading in the contents of Command Register CR0. .

COMMAND REGISTER CR0-(n)

D4	D3	D2	D1	D0
RLOL_(n)	RLOS_(n)	ALOS_(n)	DLOS_(n)	DMO_(n)
Read Only	Read Only	Read Only	Read Only	Read Only

If the ALOS_(n) bit-field contains a "1", then the corresponding Channel(n) is currently declaring an ALOS condition. Conversely, if the ALOS_(n) bit-field contains a "0", then the channel is not currently declaring an ALOS condition.

Disabling the ALOS Detector

For debugging purposes, it may be useful to disable the ALOS Detector. If the XRT73LC04A is operating in the HOST Mode, disable the Channel(n) ALOS Detector by writing a "1" into the ALOSDIS_(n) bit-field in Command Register CR2.

COMMAND REGISTER CR2-(n)

D4	D3	D2	D1	D0
Reserved	Reserved	ALOSDIS_(n)	DLOSDIS_(n)	REQEN_(n)
X	X	1	X	X

2. The Digital LOS (DLOS) Declaration/Clearance Criteria

A given channel(n) declares a Digital LOS (DLOS_(n)) condition if the XRT73LC04A detects 160±32 or more consecutive "0's" in the incoming data.

The channel clears DLOS if it detects four consecutive sets of 32 bit-periods, each of which contains at least 10 "1's" (e.g., average pulse density of greater than 33%).

Monitoring the State of DLOS

If the XRT73LC04A is operating in the HOST Mode the state of DLOS_(n) of Channel(n) can be polled or monitored by reading in the contents of Command Register CR0.

COMMAND REGISTER CR0-(n)

D4	D3	D2	D1	D0
RLOL_(n)	RLOS_(n)	ALOS_(n)	DLOS_(n)	DMO_(n)
Read Only	Read Only	Read Only	Read Only	Read Only

If the DLOS_(n) bit-field contains a “1”, then the corresponding channel(n) is currently declaring a DLOS condition. If the DLOS_(n) bit-field contains a “0”, then the channel(n) is currently declaring the DLOS condition.

Disabling the DLOS Detector

For debugging purposes, it is useful to disable the DLOS_(n) detector. If the XRT73LC04A is operating in the HOST Mode, the DLOS Detector can be disabled by writing a “1” into the DLOSDIS_(n) bit-field in Command Register CR2.

COMMAND REGISTER CR2-(n)

D4	D3	D2	D1	D0
Reserved	Reserved	ALOSDIS_(n)	DLOSDIS_(n)	REQEN_(n)
X	X	X	1	X

NOTE: *Setting both the ALOSDIS_(n) and DLOSDIS_(n) bit-fields to "1" disables LOS Declaration by Channel(n).*

3.5.3 Muting the Recovered Data while the LOS is being Declared

In some applications it is not desirable for a channel within the E3/DS3/STS-1 LIU to recover data and route it to the Receiving Terminal while the channel is declaring an LOS condition. Consequently, the XRT73LC04A includes an LOS Muting feature. This feature, if enabled, causes a given channel to halt transmission of the recovered data to the Receiving Terminal while the LOS condition is "true". In this case, the RPOS_(n) and RNEG_(n) output pins are forced to "0". Once the LOS condition has been cleared, then the channel(n) resumes normal transmission of the recovered data to the Receiving Terminal.

This feature is available whenever XRT73LC04A is operating in the HOST Mode or Hardware Mode.

a. Operating in the Hardware Mode.

The Muting upon LOS feature is enabled by pulling the LOSMUTEN output pin “High". This enables the Muting upon LOS feature globally for all channels.

b. Operating in the HOST Mode.

The Muting upon LOS feature for each Channel can be enabled by writing a "1" into the LOSMUT_(n) bit-field within Command Register 3.

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
(SR/$\overline{DR}$)_(n)	LOSMUT_(n)	RxOFF	RxClk_(n)INV	Reserved
X	1x	x	x	x

NOTE: *This step only enables the Muting upon LOS feature within Channel(n).*

3.6 ROUTING THE RECOVERED TIMING AND DATA INFORMATION TO THE RECEIVING TERMINAL EQUIPMENT

Each channel ultimately takes the Recovered Timing and Data information, converts it into CMOS levels and routes it to the Receiving Terminal Equipment via the RPOS_(n), RNEG_(n) and RxClk_(n) output pins.

Each channel can deliver the recovered data and clock information to the Receiving Terminal in either a Single-Rail or Dual-Rail format.

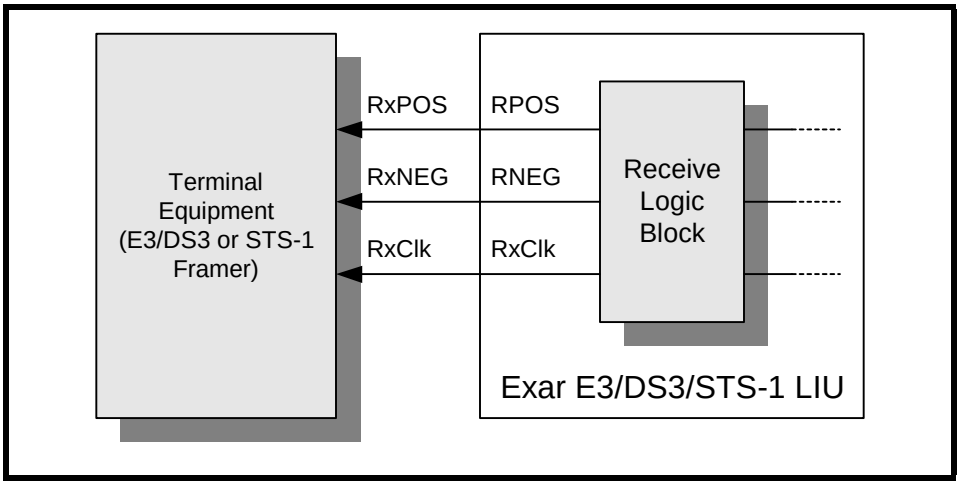
3.6.1 Routing Dual-Rail Format Data to the Receiving Terminal Equipment

Whenever a channel delivers Dual-Rail format to the Terminal Equipment, it does so via the following signals.

- RPOS_(n)
- RNEG_(n)
- RxClk_(n)

Figure 28 illustrates the typical interface for the transmission of data in a Dual-Rail Format from the Receive Section of a channel to the Receiving Terminal Equipment.

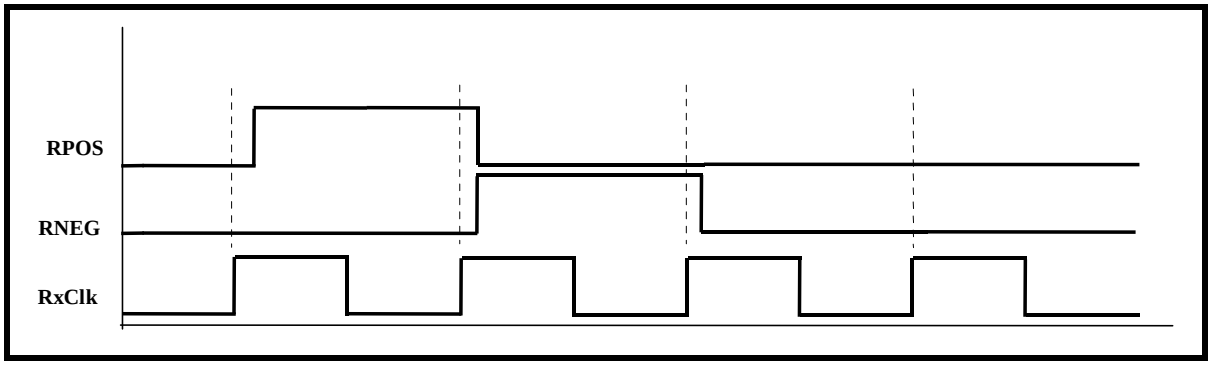
FIGURE 28. THE TYPICAL INTERFACE FOR THE TRANSMISSION OF DATA IN A DUAL-RAIL FORMAT, FROM THE RECEIVE SECTION OF THE XRT73LC04A TO THE RECEIVING TERMINAL EQUIPMENT



The manner that a given channel transmits Dual-Rail data to the Receiving Terminal Equipment is described below and illustrated in Figure 29. Each channel(n) typically updates the data on the

RPOS_(n) and RNEG_(n) output pins on the rising edge of RxClk_(n).

FIGURE 29. HOW THE XRT73LC04A OUTPUTS DATA ON THE RPOS AND RNEG OUTPUT PINS



RxClk_(n) is the Recovered Clock signal from the incoming Received line signal. As a result, these clock signals are typically 34.368 MHz for E3 applications, 44.736 MHz for DS3 applications and 51.84 MHz for SONET STS-1 applications.

In general, if a given channel received a positive-polarity pulse in the incoming line signal via the RTIP_(n) and RRing_(n) input pins, then the channel pulses its corresponding RPOS_(n) output pin “High". Conversely, if the channel received a negative-polarity pulse in the incoming line signal via the RTIP_(n) and RRing_(n) input pins, then the channel(n) pulses its corresponding RNEG_(n) output pin “High".

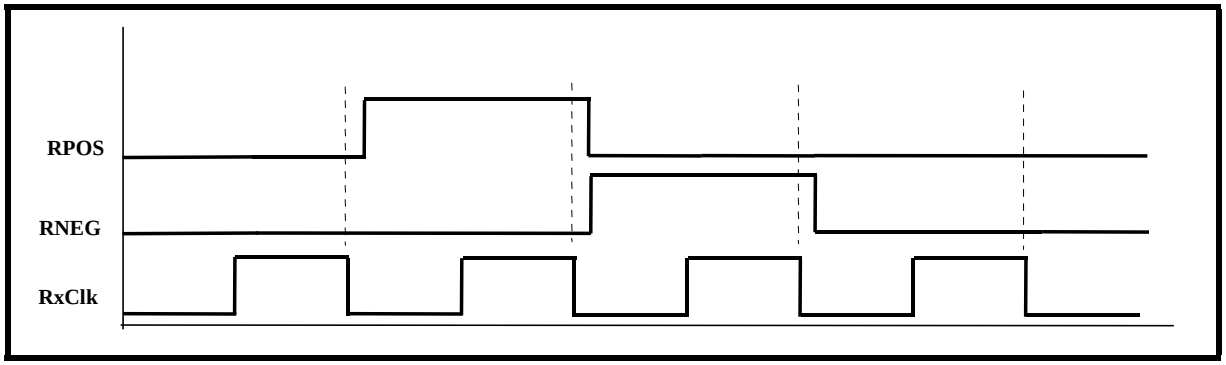
Inverting the RxClk_(n) outputs

Each channel can invert the RxClk_(n) signals with respect to the delivery of the RPOS_(n) and RNEG_(n) output data to the Receiving Terminal Equipment. This feature may be useful for those customers whose Receiving Terminal Equipment logic design is such that the RPOS_(n) and RNEG_(n) data must be sampled on the rising edge of RxClk_(n). Figure 30 illustrates the behavior of the RPOS_(n), RNEG_(n) and RxClk_(n) signals when the RxClk_(n) signal has been inverted.

In the Hardware Mode:

Setting the RxClkINV pin “High” results in all channels of the XRT73LC04A to output the recovered data on RPOS_(n) and RNEG_(n) on the falling edge of RxClk_(n). Setting this pin “Low” results in the recovered data on RPOS_(n) and RNEG_(n) to output on the rising edge of RxClk_(n).

FIGURE 30. THE BEHAVIOR OF THE RPOS, RNEG, AND RXCLK SIGNALS WHEN RXCLK IS INVERTED



a. Operating in the HOST Mode

In order to configure a channel(n) to invert the RxClk_(n) output signal, the XRT73LC04A must be operating in the HOST Mode.

To invert RxClk_(n), associated with Channel(n), write a "1" into the RxClk_(n)INV bit-field within Command Register CR-3.

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
(SR/$\overline{DR}$)_(n)	LOSMUT_(n)	RxOFF	RxClk_(n)INV	Reserved
X	X	X	1	X

b. Operating in the Hardware Mode

Setting the RxClkINV input pin “High" inverts all the RxClk_(n) output signals.

3.6.2 Routing Single-Rail Format (Binary Data Stream) data to the Receive Terminal Equipment

To route Single-Rail format data (e.g., a binary data stream) from the Receive Section of a channel to the Receiving Terminal Equipment, do the following.

a. Operating in the HOST Mode

To configure Channel(n) to output Single-Rail data to the Terminal Equipment, write a "1" into the (SR/$\overline{DR}$)_(n) bit-field within Command Register CR3-(n).

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
(SR/$\overline{DR}$)_(n)	LOSMUT_(n)	RxOFF	RxClk_(n)INV	Reserved
1	X	X	X	X

The configured channel outputs Single-Rail data to the Receiving Terminal Equipment via its corresponding RPOS_(n) and RxClk_(n) output pins, as illustrated in Figure 31 and Figure 32.

b. Operating in the Hardware Mode

The XRT73LC04A is configure to output Dual-Rail data from the Receive Sections of all channels by pulling the (SR/$\overline{DR}$) pin to GND.

The XRT73LC04A is configure to output Single-Rail data from the Receive Sections of all channels by pulling the (SR/$\overline{DR}$) pin to VDD.

NOTE: *When the XRT73LC04A is operating in the Hardware Mode, the setting of the (SR/$\overline{DR}$) input pin applies globally to all channels.*

FIGURE 31. THE TYPICAL INTERFACE FOR THE TRANSMISSION OF DATA IN A SINGLE-RAIL FORMAT FROM THE RECEIVE SECTION OF THE XRT73LC04A TO THE RECEIVING TERMINAL EQUIPMENT

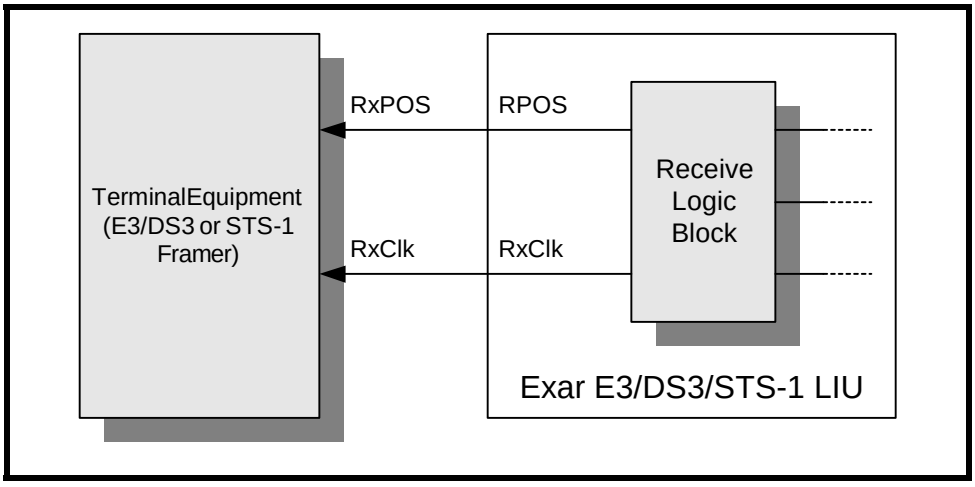
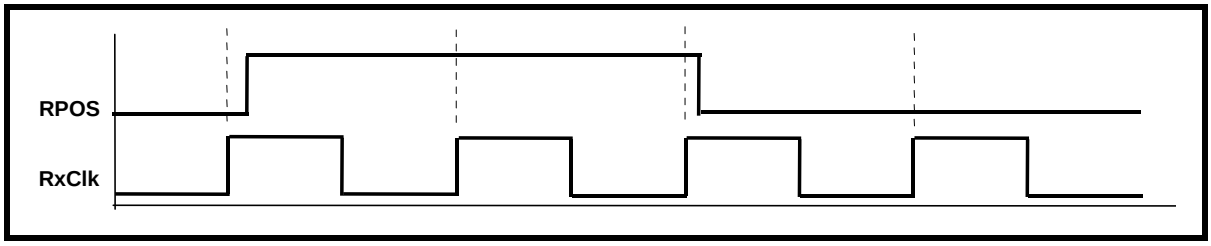


FIGURE 32. THE BEHAVIOR OF THE RPOS AND RXCLK OUTPUT SIGNALS WHILE THE XRT73LC04A IS TRANSMITTING SINGLE-RAIL DATA TO THE RECEIVING TERMINAL EQUIPMENT



NOTE: The RNEG_(n) output pin is internally tied to Ground whenever this feature is implemented.

3.7 SHUTTING OFF THE RECEIVE SECTION

The Receive Section of each channel in the XRT73LC04A can be shut off. This feature may come in handy in some redundant system designs. Particularly, in those designs where the Receive Termination within the Secondary LIU Line Card has been switched-out and is not receiving any traffic in parallel with the Primary Line Card. In this case, having the LIU on the Secondary Line Card consume the normal amount of current is a waste of power. This feature can permit powering down the Receive Section of the LIU's on the Secondary Line Card which reduces their power consumption by approximately 80%

a. Operating in the Hardware Mode

Shut off the Receive Sections by pulling the RxOFF input pin "High". Turn on the Receiver Sections by pulling the RxOFF input pin to "Low".

b. Operating in the HOST Mode

Shut off the Receive Sections by writing a "1" into the RxOFF bit-field within Command Register CR3-(n).

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
(SR/$\overline{DR}$)_(n)	LOSMUT_(n)	RxOFF	RxClk_(n)INV	Reserved
X	X	1	X	X

Turn on the Receive Section of Channel(n) by writing a "0" into the RxOFF bit-field within Command Register CR3-(n).

4.0 DIAGNOSTIC FEATURES OF THE XRT73LC04A

The XRT73LC04A supports equipment diagnostic activities by supporting the following Loop-Back modes within each channel.

- Analog Local Loop-Back.
- Digital Local Loop-Back
- Remote Loop-Back

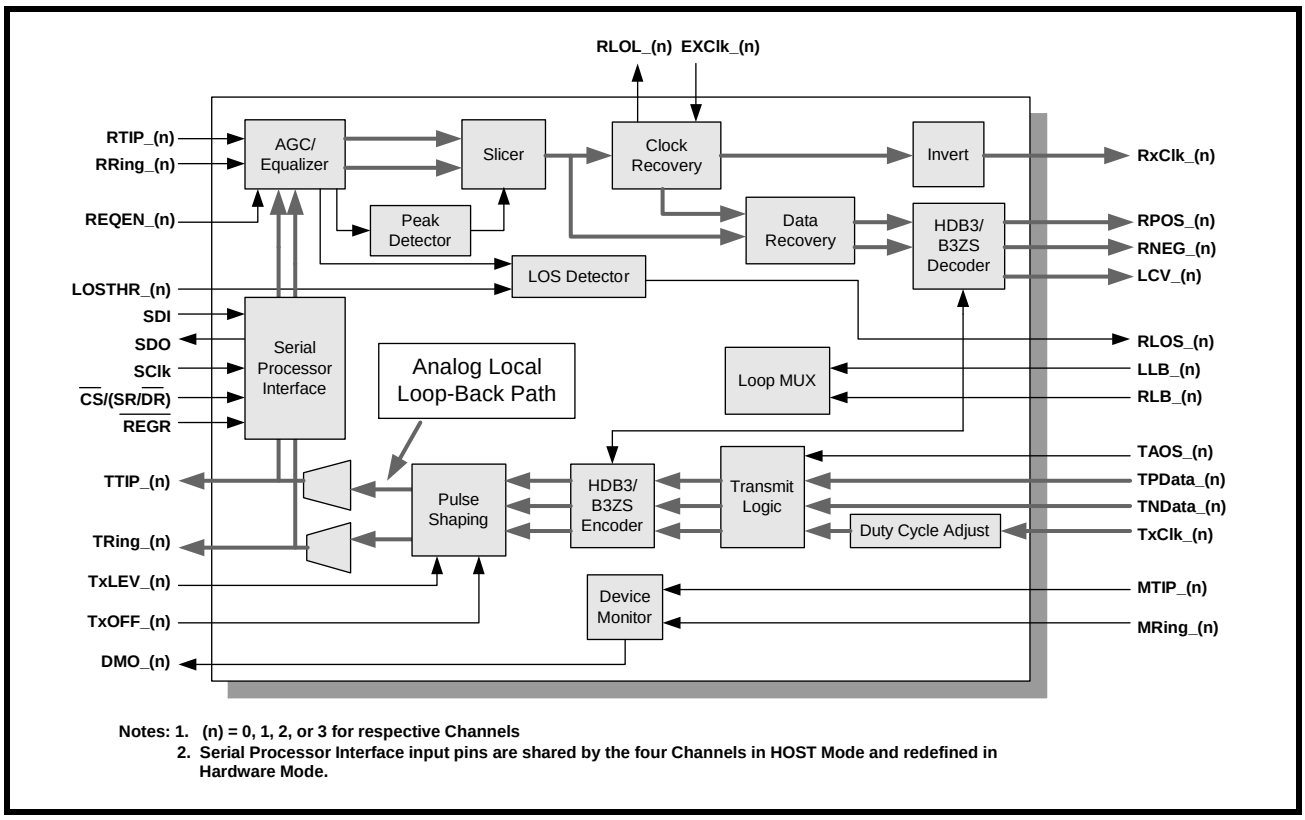
NOTE: *In this data sheet we use the convention that Channel(n) refers to either channel 0, 1, 2 or 3. Similarly, specific input and output pins uses this convention to denote which channel it is associated with.*

4.1 THE ANALOG LOCAL LOOP-BACK MODE

When a given channel is configured to operate in the Analog Local Loop-Back Mode, the channel ignores any signals that are input to its RTIP_(n) and RRing_(n) input pins. The Transmitting Terminal Equipment transmits clock and data into this channel via the TPData_(n), TNData_(n) and TxClk_(n) input pins. This data is processed through the Transmit Clock Duty Cycle Adjust PLL and the HDB3/B3ZS Encoder. Finally, this data is output to the line via the TTIP_(n) and TRing_(n) output pins. Additionally, this data which is being output via the TTIP_(n) and TRing_(n) output pins is also looped back into the Attenuator/Receive Equalizer Block. Consequently, this data is processed through the entire Receive Section of the channel. After this post-Loop-Back data has been processed through the Receive Section it outputs to the Near-End Receiving Terminal Equipment via the RPOS_(n), RNEG_(n) and RxClk_(n) output pins.

Figure 33 illustrates the path that the data takes when the channel is configured to operate in the Analog Local Loop-Back Mode.

FIGURE 33. A CHANNEL OPERATING IN THE ANALOG LOCAL LOOP-BACK MODE



Notes: 1. (n) = 0, 1, 2, or 3 for respective Channels
2. Serial Processor Interface input pins are shared by the four Channels in HOST Mode and redefined in Hardware Mode.

Configure a given channel to operate in the Analog Local Loop-Back Mode by employing either one of the following two steps

a. Operating in the HOST Mode

NOTE: *See Table 2 for a description of Command Registers and Addresses for the different channels.*

To configure Channel (n) to operate in the Analog Local Loop-Back Mode, write a “1" into the LLB_(n) bit-field and a "0" into the RLB_(n) bit-field within Command Register CR4.

COMMAND REGISTER CR4-(n)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$_(n)	E3_(n)	LLB_(n)	RLB_(n)
X	X	X	1	0

b. Operating in the Hardware Mode

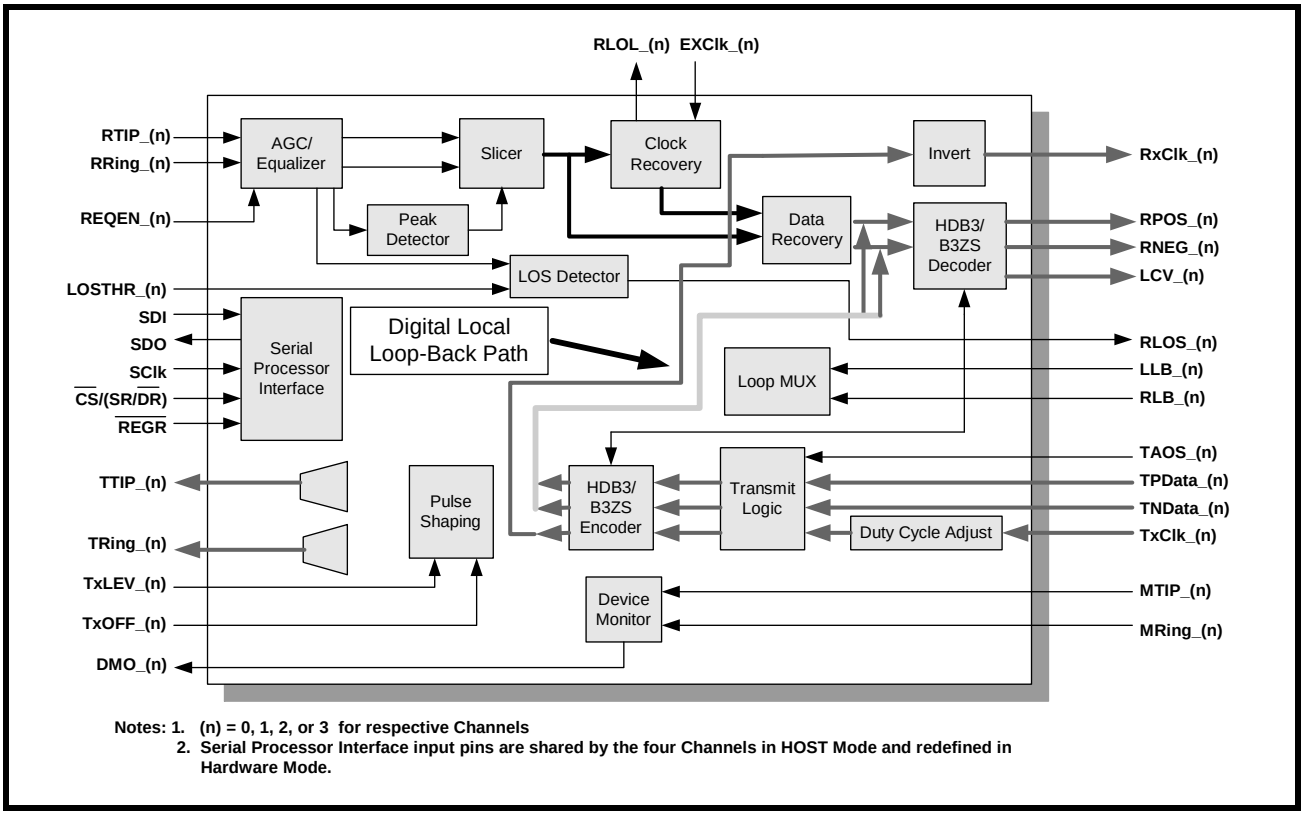
To configure Channel (n) to operate in the Analog Local Loop-Back Mode, set the LLB_(n) input pin (pin 76, 84, 97 or 105) “High" and the RLB_(n) input pin (pin 77, 85, 96 or 104) "Low".

4.2 The Digital Local Loop-Back Mode.

When a given channel is configured to operate in the Digital Local Loop-Back Mode, the channel ignores any signals that are input to the RTIP and RRing input pins. The Transmitting Terminal Equipment transmits clock and data into the XRT73LC04A via the TPData, TNData and TxClk input pins. This data is processed through the Transmit Clock Duty Cycle Adjust PLL and the HDB3/B3ZS Encoder block. At this point, this data is looped back to the HDB3/B3ZS Decoder block. After this post-Loop-Back data has been processed through the HDB3/B3ZS Decoder block, it outputs to the Near-End Receiving Terminal Equipment via the RPOS, RNEG and RxClk output pins.

Figure 34 illustrates the path that the data takes when the chip is configured to operate in the Digital Local Loop-Back Mode.

Figure 34. The Digital Local Loop-Back path within a given channel



Notes: 1. (n) = 0, 1, 2, or 3 for respective Channels
2. Serial Processor Interface input pins are shared by the four Channels in HOST Mode and redefined in Hardware Mode.

Configure a channel to operate in the Digital Local Loop-Back Mode by employing either one of the following two-steps:

a. Operating in the Host Mode

To configure Channel (n) to operate in the Digital Local Loop-Back Mode, write a "1" into both the LLB and RLB bit-fields within Command Register CR4-(n).

COMMAND REGISTER CR4-(n)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$_(n)	E3_(n)	LLB_(n)	RLB_(n)
X	X	X	1	1

b. Operating in the Hardware Mode.

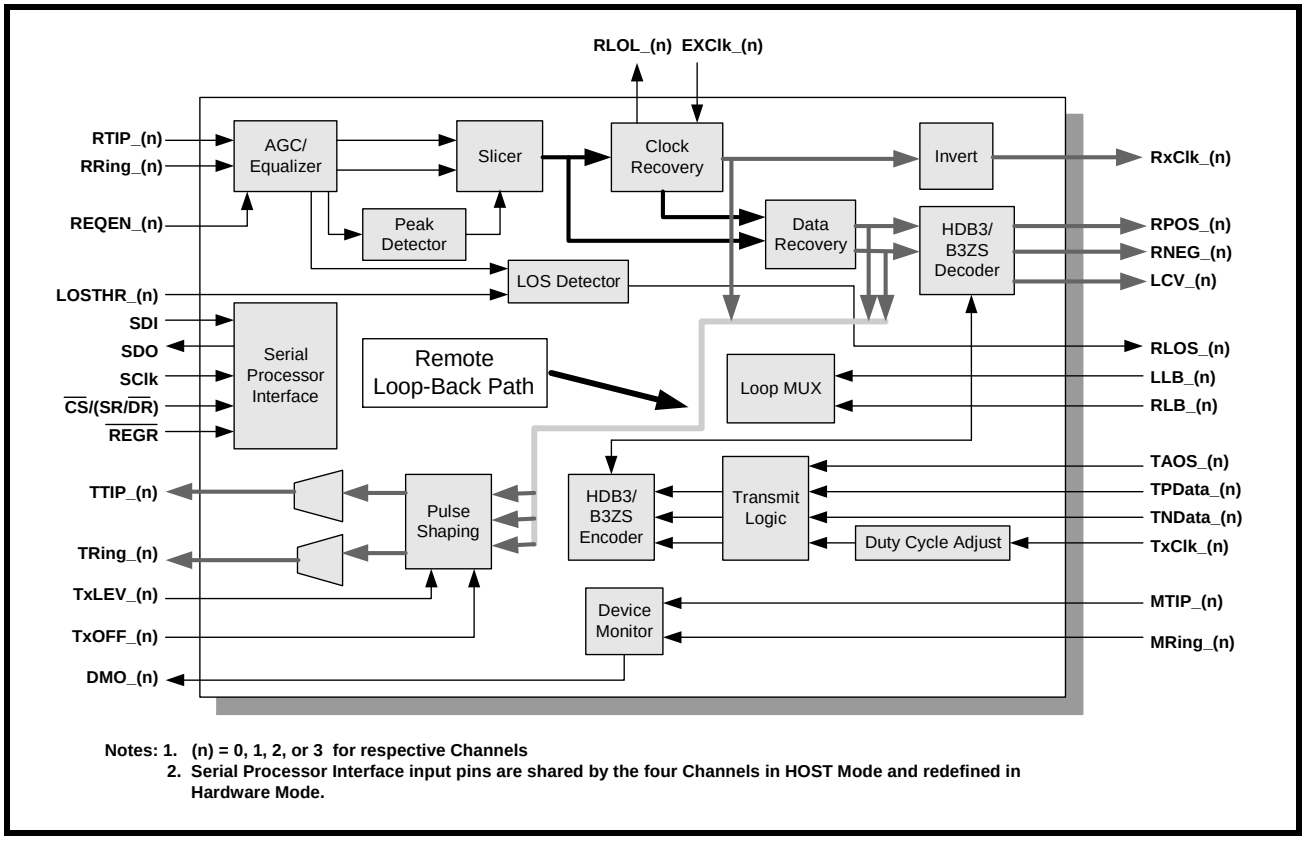
To configure Channel (n) to operate in the Digital Local Loop-Back Mode, pull both the LLB input pin and the RLB input pin "High".

4.3 The Remote Loop-Back Mode

When a given channel is configured to operate in the Remote Loop-Back Mode, the channel ignores any signals that are input to the TPData and TNData input pins. The channel receives the incoming line signal via the RTIP and RRing input pins. This data is processed through the entire Receive Section and is output to the Receive Terminal Equipment via the RPOS, RNEG and RxClk output pins. Additionally, this data is also internally looped back into the Pulse-Shaping block within the Transmit Section. At this point, this data is routed through the remainder of the Transmit Section of the channel and transmitted out onto the line via the TTIP_(n) and TRing_(n) output pins.

Figure 35 illustrates the path that the data takes when the chip is configured to operate in the Remote Loop-Back Mode.

Figure 35. The Remote Loop-Back path, within a given channel



Notes: 1. (n) = 0, 1, 2, or 3 for respective Channels
2. Serial Processor Interface input pins are shared by the four Channels in HOST Mode and redefined in Hardware Mode.

Configure a channel to operate in the Remote Loop-Back Mode by employing either one of the following two steps

a. Operating in the HOST Mode

To configure Channel (n) to operate in the Remote Loop-Back Mode, write a "1" into the RLB bit-field, and a "0" into the LLB bit-field, within Command Register CR4.

COMMAND REGISTER CR4-(n)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$_(n)	E3_(n)	LLB_(n)	RLB_(n)
X	X	X	0	1

b. Operating in the Hardware Mode

To configure Channel(n) to operate in the Remote Loop-Back Mode, pull both the RLB_(n) input pin to “High" and the LLB_(n) input pin to "Low".

4.4 TxOFF Features

The Transmit Section of each Channel in the XRT73LC04A can be shut off. When this feature is invoked, the Transmit Section of the configured channel is shut-off and the Transmit Output signals (e.g., TTIP_(n) and TRing_(n)) is tri-stated. This feature is useful for system redundancy conditions or during diagnostic testing.

a. Operating in the Hardware Mode

Shut off the Transmit Driver concurrently within all Channels by toggling the TxOFF input pin “High". Turn on the Transmit Driver by toggling the TxOFF input pin “Low".

b. Operating in the HOST Mode

Turn off the Transmit Driver within Channel(n) by setting the TxOFF_(n) bit-field within Command Register CR1-(n) to "1".

COMMAND REGISTER CR1-(n)

D4	D3	D2	D1	D0
TxOFF_(n)	TAOS_(n)	TxClkINV_(n)	TxLEV_(n)	Reserved
1	X	X	X	X

Writing a "0" into this bit-field enables the Channel(n)Transmit Driver.

NOTE: *In order to permit a system designed for redundancy to quickly shut-off a defective line card and turn-on the back-up line card, the XRT73LC04A was designed such that either Transmitter can quickly be turned-on or turned-off by toggling the TxOFF input pins. This approach is much quicker then setting the TxOFF_(n) bit-fields via the Microprocessor Serial Interface.*

Table 6 presents a Truth Table which relates the setting of the TxOFF external pin and bit-field for a channel to the state of the Transmitter. This table applies to all Channels of the XRT73LC04A.

TABLE 6: THE RELATIONSHIP BETWEEN THE TxOFF INPUT PIN, THE TxOFF BIT FIELD AND THE STATE OF THE TRANSMITTER

STATE OF THE TxOFF INPUT PIN	STATE OF THE TxOFF BIT FIELD	STATE OF THE TRANSMITTER
LOW	0	ON (Transmitter is Active)
LOW	1	OFF (Transmitter is Tri-Stated)
HIGH	0	OFF (Transmitter is Tri-Stated)
HIGH	1	OFF (Transmitter is Tri-Stated)

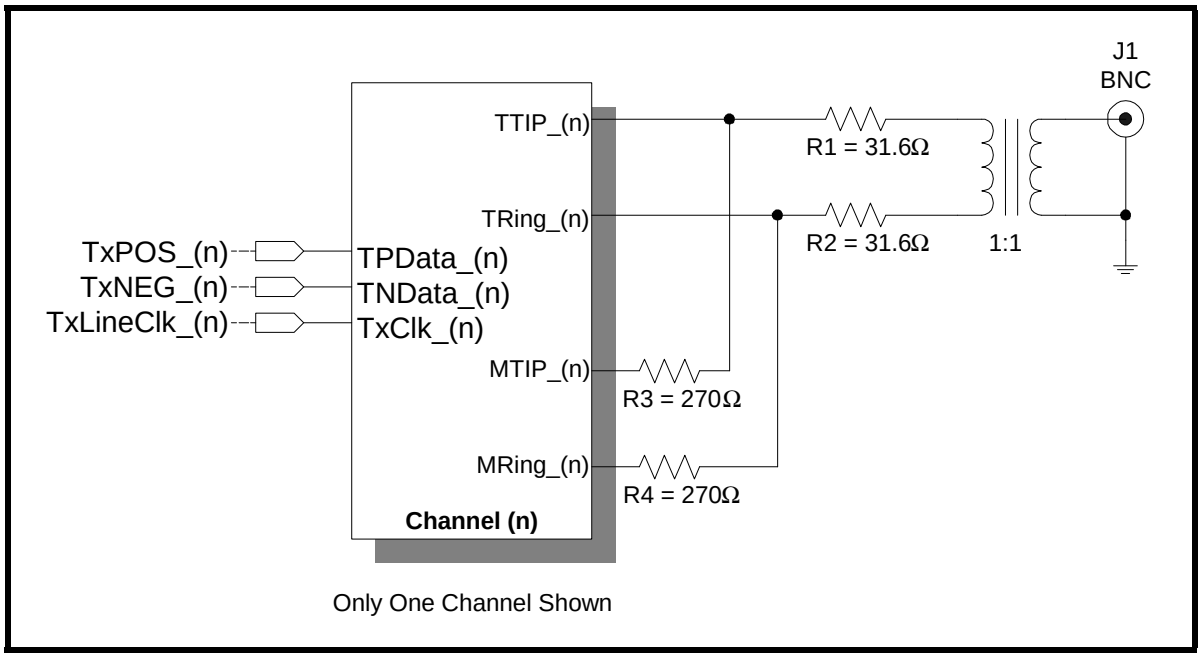
To control the state of all transmitters via the Microprocessor Serial interface, connect the TxOFF input pin to GND.

4.5 The Transmit Drive Monitor Features

The Transmit Drive Monitor is used to monitor the line in the Transmit Direction for the occurrence of fault conditions such as a short circuit on the line, a defective Transmit Drive in the XRT73LC04A or another LIU.

Activate the Channel(n) Transmit Drive Monitor by connecting the MTIP_(n) pin to the TTIP_(n) line through a 270 Ohm resistor connected in series, and connecting the MRing_(n) pin to the TRing_(n) line through a 270 Ohm resistor connected in series. Such an approach is illustrated in Figure 36.

FIGURE 36. THE XRT73LC04A EMPLOYING THE TRANSMIT DRIVE MONITOR FEATURES



When the Transmit Drive Monitor circuitry within a given line is connected to the line, as illustrated in Figure 36, then it monitors the line for transitions. As long as the Transmit Drive Monitor circuitry detects transitions on the line via the MTIP_(n) and MRing_(n) pins, then it keeps the DMO (Drive Monitor Output) signal "Low". If the Transmit Drive Monitor circuit detects no transitions on the line for 128±32 TxClk periods, then the DMO (Drive Monitor Output) signal toggles "High".

NOTE: *The Transmit Drive Monitor circuit does not have to be used to operate the Transmit Section of the XRT73LC04A. This is purely a diagnostic feature.*

4.6 THE TAOS (TRANSMIT ALL ONES) FEATURE

The XRT73LC04A can command any channel to transmit an all “1’s" pattern onto the line by toggling a single input pin or by setting a single bit-field within one of the Command Registers to "1".

NOTE: *When this feature is activated, the Transmit Section of the configured channel overwrites the Terminal Equipment data with this all “1’s" pattern.*

a. Operating in the Hardware Mode

Configure Channel(n) to transmit an all “1’s" pattern by toggling the TAOS_(n) input pin (pin 45, 46, 135 or 136) “High". Terminate the all “1’s" pattern by toggling the TAOS_(n) input pin “Low".

b. Operating in the HOST Mode

Configure Channel(n) to transmit an all “1’s" pattern by writing to Command Register CR1-(n) and setting the TAOS_(n) bit-field (bit D3) to "1".

COMMAND REGISTER CR1-(n)

D4	D3	D2	D1	D0
TxOFF_(n)	TAOS_(n)	TxClkINV_(n)	TxLEV_(n)	Reserved
0	1	X	X	X

Terminate the all “1’s" pattern by writing to Command Register CR1-(n) and setting the TAOS_(n) bit-field (D3) to "0".

5.0 THE MICROPROCESSOR SERIAL INTERFACE

The on-chip Command Registers of XRT73LC04A DS3/E3/STS-1 Line Interface Unit IC are used to configure the XRT73LC04A into a wide-variety of modes. This section discusses the following:

1. The description of the Command Registers.
2. A description on how to use the Microprocessor Serial Interface.

5.1 DESCRIPTION OF THE COMMAND REGISTERS

(repeated as Table 7), lists the Command Registers, their Addresses and their bit-formats.

TABLE 7: HEXADECIMAL ADDRESSES AND BIT FORMATS OF XRT73LC04A COMMAND REGISTERS

			REGISTER BIT-FORMAT				
ADDRESS	COMMAND REGISTER	TYPE	D4	D3	D2	D1	D0
CHANNEL 0							
0x00	CR0-0	RO	RLOL_0	RLOS_0	ALOS_0	DLOS_0	DMO_0
0x01	CR1-0	R/W	TxOFF_0	TAOS_0	TxClkINV_0	TxLEV_0	Reserved
0x02	CR2-0	R/W	Reserved	Reserved	ALOSDIS_0	DLOSDIS_0	REQEN_0
0x03	CR3-0	R/W	(SR/$\overline{DR}$)_0	LOSMUT_0	RxOFF	RxClk_0INV	Reserved
0x04	CR4-0	R/W	Reserved	STS-1/$\overline{DS3}$_0	E3_0	LLB_0	RLB_0
0x05	CR5-0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6-0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7-0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
CHANNEL 1							
0x08	CR0-1	RO	RLOL_1	RLOS_1	ALOS_1	DLOS_1	DMO_1
0x09	CR1-1	R/W	TxOFF_1	TAOS_1	TxClkINV_1	TxLEV_1	Reserved
0x0A	CR2-1	R/W	Reserved	Reserved	ALOSDIS_1	DLOSDIS_1	REQEN_1
0x0B	CR3-1	R/W	SR/$\overline{DR}$_1	LOSMUT_1	RxOFF	RxClk_1INV	Reserved
0x0C	CR4-1	R/W	Reserved	STS-1/$\overline{DS3}$_1	E3_1	LLB_1	RLB_1
0x0D	CR5-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0E	CR6-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0F	CR7-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
CHANNEL 2							
0x10	CR0-2	RO	RLOL_2	RLOS_2	ALOS_2	DLOS_2	DMO_2
0x11	CR1-2	R/W	TxOFF_2	TAOS_2	TxClkINV_2	TxLEV_2	Reserved
0x12	CR2-2	R/W	Reserved	Reserved	ALOSDIS_2	DLOSDIS_2	REQEN_2
0x13	CR3-2	R/W	SR/$\overline{DR}$_2	LOSMUT_2	RxOFF	RxClk_2INV	Reserved
0x14	CR4-2	R/W	Reserved	STS-1/$\overline{DS3}$_2	E3_2	LLB_2	RLB_2
0x15	CR5-2	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x16	CR6-2	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x17	CR7-2	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

TABLE 7: HEXADECIMAL ADDRESSES AND BIT FORMATS OF XRT73LC04A COMMAND REGISTERS

			REGISTER BIT-FORMAT				
ADDRESS	COMMAND REGISTER	TYPE	D4	D3	D2	D1	D0
CHANNEL 3							
0x18	CR0-3	RO	RLOL_3	RLOS_3	ALOS_3	DLOS_3	DMO_3
0x19	CR1-3	R/W	TxOFF_3	TAOS_3	TxClkINV_3	TxLEV_3	Reserved
0x1A	CR2-3	R/W	Reserved	Reserved	ALOSDIS_3	DLOSDIS_3	REQEN_3
0x1B	CR3-3	R/W	SR/$\overline{DR}$_3	LOSMUT_3	RxOFF	RxClk_3INV	Reserved
0x1C	CR4-3	R/W	Reserved	STS-1/$\overline{DS3}$_3	E3_3	LLB_3	RLB_3
0x1D	CR5-3	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x1E	CR6-3	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x1F	CR7-3	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

Address

The register addresses are presented in the **Hexadecimal** format.

Type:

The Command Registers are either Read-Only (RO) type of registers or Read/Write (R/W) type of registers. Each channel of the XRT73LC04A has eight command registers, CR0-(n) through CR7-(n) where (n) = 0, 1, 2 or 3. The associated addresses for each channel are presented in , (repeated as Table 7).

NOTE: *The default value for each of the bit-fields within these register is "0".*

5.2 DESCRIPTION OF BIT-FIELDS FOR EACH COMMAND REGISTER

5.2.1 Command Register - CR0-(n)

The bit-format and default values for Command Register CR0-(n) are listed below followed by the function of each of these bit-fields.

COMMAND REGISTER CR0-(n)

D4	D3	D2	D1	D0
RLOL_(n)	RLOS_(n)	ALOS_(n)	DLOS_(n)	DMO_(n)
1	1	1	1	1

Bit D4 - RLOL_(n) (Receive Loss of Lock Status - Channel(n))

This Read-Only bit-field reflects the lock status of the Channel(n) Clock Recovery Phase-Locked-Loop

This bit-field is set to “0” if the Channel(n) Clock Recovery PLL is in lock with the incoming line signal.

This bit-field is set to "1" if the Clock Recovery PLL is out of lock with the incoming line signal.

Bit D3 - RLOS_(n) (Receive Loss of Signal Status - Channel(n))

This Read-Only bit-field indicates whether or not the Channel(n) of the Receiver is currently declaring an LOS (Loss of Signal) Condition.

This bit-field is set to "0" if Channel(n) is not currently declaring the LOS Condition.

This bit-field is set to "1" if Channel(n) is declaring an LOS Condition.

Bit D2 - ALOS_(n) (Analog Loss of Signal Status - Channel(n))

This Read-Only bit-field indicates whether or not the Channel(n) Analog LOS Detector is currently declaring an LOS condition.

This bit-field is set to "0" if the Analog LOS Detector within Channel(n) is NOT currently declaring an LOS condition. This bit-field is set to "1" if the Analog LOS Detector is currently declaring an LOS condition.

NOTE: *The purpose is to isolate the Detector (e.g., either the Analog LOS or the Digital LOS detector) that is declaring the LOS condition. This feature may be useful for troubleshooting/debugging purposes*

Bit D1 - DLOS_(n) (Digital Loss of Signal Status - Channel(n))

This Read-Only bit-field indicates whether or not the Channel(n) Digital LOS Detector is currently declaring an LOS condition.

This bit-field is set to "0" if the Channel(n) Digital LOS Detector is NOT currently declaring an LOS condi-

tion. This bit-field is set to "1" if the Channel(n) Digital LOS Detector is currently declaring an LOS condition.

NOTE: The purpose is to isolate the Detector (e.g., either the Analog LOS or the Digital LOS detector) that is declaring the LOS condition. This feature may be useful for troubleshooting/debugging purposes.

Bit D0 - DMO_(n) (Drive Monitor Output Status - Channel(n))

This Read-Only bit-field reflects the status of the DMO output pin.

5.2.2 Command Register CR1

The bit-format and default values for Command Register CR1-(n) are listed below followed by the function of each of these bit-fields..

COMMAND REGISTER CR1-(n)

D4	D3	D2	D1	D0
TxOFF_(n)	TAOS_(n)	TxClkINV_(n)	TxLEV_(n)	Reserved
0	0	0	0	0

Bit D4 - TxOFF_(n) (Transmitter OFF - Channel(n))

This Read/Write bit-field is used to turn off the Channel(n) Transmitter.

Writing a "1" to this bit field turns off the Transmitter and tri-state the Transmit Output. Writing a "0" to this bit-field turns on the Transmitter.

Bit D3 - TAOS_(n) (Transmit All OneS - Channel(n))

This Read/Write bit-field is used to command the Channel(n) Transmitter to generate and transmit an all “1’s” pattern onto the line.

Writing a "1" to this bit-field commands the Transmitter to transmit an all “1’s” pattern onto the line. Writing a "0" to this bit-field commands normal operation.

Bit D2 - TxClkINV_(n) (Transmit Clock Invert - Channel(n))

This Read/Write bit-field is used to configure the Transmitter to sample the signal at the TPData and TNData pins on the rising edge or falling edge of TxClk (the Transmit Line Clock signal).

Writing a "1" to this bit-field configures the Transmitter to sample the TPData and TNData input pins on the rising edge of TxClk. Writing a “0" to this bit-field configures the Transmitter to sample the TPData and TNData input pins on the falling edge of TxClk.

Bit D1 - TxLEV_(n) (Transmit Line Build-Out Enable/Disable Select - Channel(n))

This Read/Write bit-field is used to enable or disable the Channel(n) Transmit Line Build-Out circuit.

Setting this bit-field "High" disables the Channel(n) Line Build-Out circuit. In this mode, Channel(n) outputs partially-shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins.

Setting this bit-field "Low" enables the Channel(n) Line Build-Out circuit. In this mode, Channel(n) outputs shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins.

In order to comply with the Isolated DSX-3/STSX-1 Pulse Template Requiremnts per Bellcore GR-499-CORE or GR-253-CORE:

a. Set this bit-field to "1" if the cable length between the Cross-Connect and the transmit output of Channel(n) is greater than 225 feet.

b. Set this bit-field to "0" if the cable length between the Cross-Connect and the transmit output of Channel(n) is less than 225 feet.

This bit-field is active only if the XRT73LC04A is configured to operate in the DS3 or SONET STS-1 Modes.

If the cable length is greater than 225 feet, set this bit-field to "1" in order to increase the amplitude of the Transmit Output Signal. If the cable length is less than 225 feet, set this bit-field to "0".

NOTE: This option is only available when the XRT73LC04A is operating in the DS3 or STS-1 Mode.

5.2.3 Command Register CR2-(n)

The bit-format and default values for Command Register CR2-(n) are listed below followed by the function of each of these bit fields.

COMMAND REGISTER CR2-(n)

D4	D3	D2	D1	D0
Reserved	Reserved	ALOSDIS_(n)	DLOSDIS_(n)	REQEN_(n)
X	0	0	0	0

Bit D4 - Reserved

Bit D3 - Reserved

Bit D2 - ALOSDIS_(n) (Analog LOS Disable - Channel(n))

This Read/Write bit-field is used to enable or disable the Channel(n) Analog LOS Detector.

Writing a "0" to this bit-field enables the Analog LOS Detector. Writing a "1" to this bit-field disables the Analog LOS Detector.

NOTE: *If the Analog LOS Detector is disabled, then the RLOS input pin is only asserted by the DLOS (Digital LOS Detector).*

Bit D1 - DLOSDIS_(n) (Digital LOS Disable - Channel(n))

This Read/Write bit-field to used to enable or disable the Channel(n) Digital LOS Detector .

Writing a "0" to this bit-field enables the Digital LOS Detector. Writing a "1" to this bit-field disables the Digital LOS Detector.

NOTE: *If the Digital LOS Detector is disabled, then the RLOS input pin is only asserted by the ALOS (Analog LOS Detector).*

Bit D0 - REQEN_(n) (Receive Equalization Enable - Channel(n))

This Read/Write bit-field is used to enable or disable the internal Channel(n) Receive Equalizer.

Writing a "1" to this bit-field enables the Internal Equalizer. Writing a "0" to this bit-field disables the Internal Equalizer.

5.2.4 Command Register CR3-(n)

The bit-format and default values for Command Register CR3-(n) are listed below followed by the function of each of these bit fields.

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
SR/$\overline{DR}$_(n)	LOSMUT_(n)	RxOFF	RxClk_(n)INV	Reserved
0	0	0	0	0

Bit D4 - SR/$\overline{DR}$ (Single-Rail/Dual-Rail Data Output - Channel(n))/(B3ZS/HDB3 Encoder/Decoder-Disable - Channel(n))

This Read/Write bit-field is used to configure Channel(n) to output the received data from the Remote Terminal in a binary or Dual-Rail format and Enable or Disable the B3ZS/HDB3 Encoder and Decoder blocks.

Writing a "1" to this bit-field enables the B3ZS/HDB3 Encoder and Decoder blocks. Writing a "0" to this bit-field disables the B3ZS/HDB3 Encoder and Decoder blocks.

NOTE: *This Encoder/Decoder performs HDB3 Encoding/ Decoding if the XRT73LC04A is operating in the E3 Mode. Otherwise, it performs B3ZS Encoding/Decoding.*

.Writing a "1" to this bit-field also configures Channel(n) to output data to the Terminal Equipment in a binary (Single-Rail) format via the RPOS_(n) output pin, RNEG_(n) is grounded. Writing a "0" to this bit-field configures Channel(n) to output data to the Terminal Equipment in a Dual-Rail format via both the RPOS_(n) and RNEG_(n) output pins.

Bit D3 - LOSMUT_(n) (Recovered Data Muting, during LOS Condition - Channel(n))

This Read/Write bit-field is used to configure Channel(n) to not output any recovered data from the line while it is declaring an LOS condition.

Writing a "0" to this bit-field configures the chip to output recovered data even while the XRT73LC04A is declaring an LOS condition. Writing a "1" to this bit-field configures the chip to NOT output the recovered data while an LOS condition is being declared.

NOTE: *In this mode, RPOS_(n) and RNEG_(n) is set to "0", asynchronously.*

Bit D2 - RxOFF (Receive Section - Shut OFF Select)

This Read/Write bit-field is used to shut-off the Receive Sections. The purpose is to conserve power consumption when this device is the back-up device in a Redundancy System.

Writing a "1" into this bit-field shuts off the Receive Sections. Writing a "0" into this bit-field turns on the Receive Sections.

Bit D1 - RxClk_(n)INV (Invert RxClk_(n))

This Read/Write bit-field is used to configure the Channel(n) Receiver to output the recovered data on either the rising edge or the falling edge of the RxClk_(n) clock signal.

Writing a "0" to this bit-field configures the Receiver to output the recovered data on the rising edge of the RxClk_(n) output signal. Writing a "1" to this bit-field configures the Receiver to output the recovered data on the falling edge of the RxClk_(n) output signal.

Bit D0 - Reserved

This bit-field has no defined functionality

Command Register CR4-(n)

The bit-format and default values for Command Register CR4 are listed below followed by the function of each of these bit-fields.

COMMAND REGISTER CR4-(n)

D4	D3	D2	D1	D0
Reserved	STS-1/$\overline{DS3}$_(n)	E3_(n)	LLB_(n)	RLB_(n)
0	0	0	0	0

Bit D4 - Reserved

This bit-field has no defined functionality

Bit D3 - STS-1/($\overline{DS3}$_(n)) - Channel(n) - Mode Select

This Read/Write bit field is used to configure Channel(n) to operate in either the SONET STS-1 Mode or the DS3 Mode.

Writing a "0" into this bit-field configures Channel(n) to operate in the DS3 Mode. Writing a "1" into this bit-field configures Channel(n) to operate in the SONET STS-1 Mode.

NOTE: *This bit-field is ignored if the E3_(n) bit-field (e.g., D2 within this Command Register) is set to "1".*

Bit D2 - E3 Mode Select - Channel(n)

This Read/Write bit-field is used to configure Channel(n) to operate in the E3 Mode.

Writing a "0" into this bit-field configures Channel(n) to operate in either the DS3 or SONET STS-1 Mode as specified by the setting of the DS3 bit-field within this Command Register. Writing a "1" into this bit-field configures Channel(n) to operate in the E3 Mode.

Bit D1 - LLB_(n) (Local Loop-Back - Channel(n))

This Read/Write bit-field along with RLB_(n) is used to configure Channel(n) to operate in any one of a variety of Loop-Back modes.

Table 8 relates the contents of LLB_(n) and RLB_(n) and the corresponding Loop-Back mode for Channel(n).

Bit D0 - RLB_(n) (Remote Loop-Back - Channel(n))

This Read/Write bit-field, along with LLB_(n), is used to configure Channel(n) to operate in any one of a variety of Loop-Back modes.

Table 8 relates the contents of LLB_(n) and RLB_(n) and the corresponding Loop-Back mode for Channel(n).

TABLE 8: CONTENTS OF LLB_(n) AND RLB_(n) AND THE CORRESPONDING LOOP-BACK MODE FOR CHANNEL(n)

LLB_(n)	RLB_(n)	LOOP-BACK MODE (FOR CHANNEL(n))
0	0	None
1	0	Analog Loop-Back Mode (See Section 4.1 for details)
1	1	Digital Loop-Back Mode (See Section 4.2 for details)
0	1	Remote Loop-Back Mode (See Section 4.3 for details)

5.3 OPERATING THE MICROPROCESSOR SERIAL INTERFACE.

The XRT73LC04A Serial Interface is a simple four wire interface that is compatible with many of the microcontrollers available in the market. This interface consists of the following signals:

- $\overline{CS}$ - Chip Select (Active Low)
- SClk - Serial Clock
- SDI - Serial Data Input
- SDO - Serial Data Output

Using the Microprocessor Serial Interface

The following instructions for using the Microprocessor Serial Interface are best understood by referring to the diagram in Figure 37 and the timing diagram in Figure 38.

In order to use the Microprocessor Serial Interface, a clock signal must be first applied to the SClk input pin. Then, initiate a Read or Write operation by asserting the active-low Chip Select input pin $\overline{CS}$. It is important to assert the $\overline{CS}$ pin (e.g., toggle it “Low") at least 5ns prior to the very first rising edge of the clock signal.

Once the $\overline{CS}$ input pin has been asserted, the type of operation and the target register address must now be specified. Provide this information to the Microprocessor Serial Interface by writing eight serial bits of data into the SDI input.

NOTE: Each of these bits is clocked into the SDI input on the rising edge of SClk.

Bit 1 - R/W (Read/Write) Bit

This bit is clocked into the SDI input, on the first rising edge of SClk after $\overline{CS}$ has been asserted. This bit indicates whether the current operation is a Read or Write operation. A "1" in this bit specifies a Read operation, a "0" in this bit specifies a Write operation.

Bits 2 through 6: The five (5) bit Address Values (labeled A0, A1, A2 , A3 and A4)

The next five rising edges of the SClk signal clocks in the 5-bit address value for this particular Read or Write operation. The address selects the Command Register in the XRT73LC04A that the user is either reading data from or writing data to. The address bits must be supplied to the SDI input pin in ascending order with the LSB (least significant bit) first.

Bit 7:

A5 must be set to "0", as shown in Figure 37.

Bit 8 - A6

The value of A6 is a don't care.

Once these first 8 bits have been written into the Microprocessor Serial Interface, the subsequent action depends upon whether the current operation is a Read or Write operation.

Read Operation

Once the last address bit (A4) has been clocked into the SDI input, the Read operation proceeds through an idle period lasting two SClk periods. On the falling edge of SClk Cycle #8 (see Figure 37) the serial data output signal (SDO) becomes active. At this point, reading the data contents of the addressed Command Register at Address [A4, A3, A2, A1, A0] via the SDO output pin can begin. The Microprocessor Serial Interface outputs this five bit data word (D0 through D4) in ascending order with the LSB first on the falling edges of the SClk pin. Consequently, the data on the SDO output pin is sufficiently stable for reading by the Microprocessor on the very next rising edge of the SClk pin.

Write Operation

Once the last address bit (A4) has been clocked into the SDI input, the Write operation proceeds through an idle period lasting two SClk periods. Prior to the rising edge of SClk Cycle # 9 (see Figure 37). Apply the desired eight bit data word to the SDI input pin via the Microprocessor Serial Interface. The Microprocessor Serial Interface latches the value on the SDI input pin on the rising edge of SClk. Apply this word (D0 through D7) serially, in ascending order with the LSB first.

Simplified Interface Option

The design of the circuitry connecting to the Microprocessor Serial Interface can be simplified by tying both the SDO and SDI pins together and reading data from and/or writing data to this combined signal. This simplification is possible because only one of these signals are active at any given time. The inactive signal is tri-stated.

NOTES:

1. *A5 is always "0"*
2. *R/W = "1" for Read Operations*
3. *R/W = "0" for Write Operations*
4. *Shaded box denotes a “don't care” value*

FIGURE 37. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE

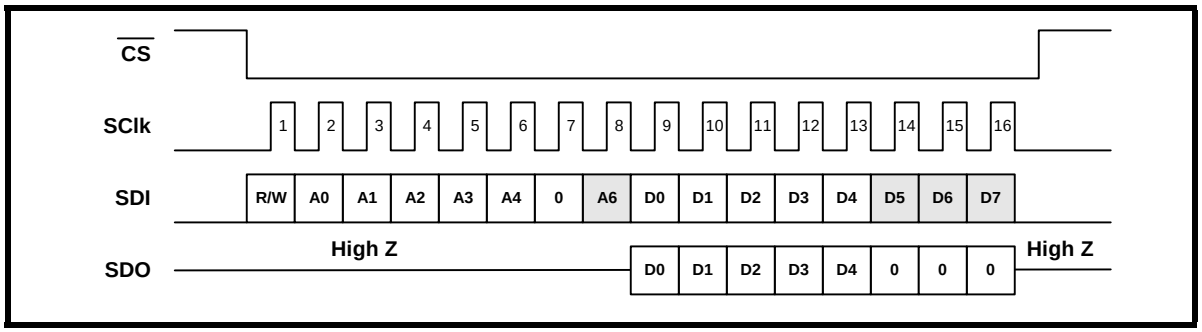
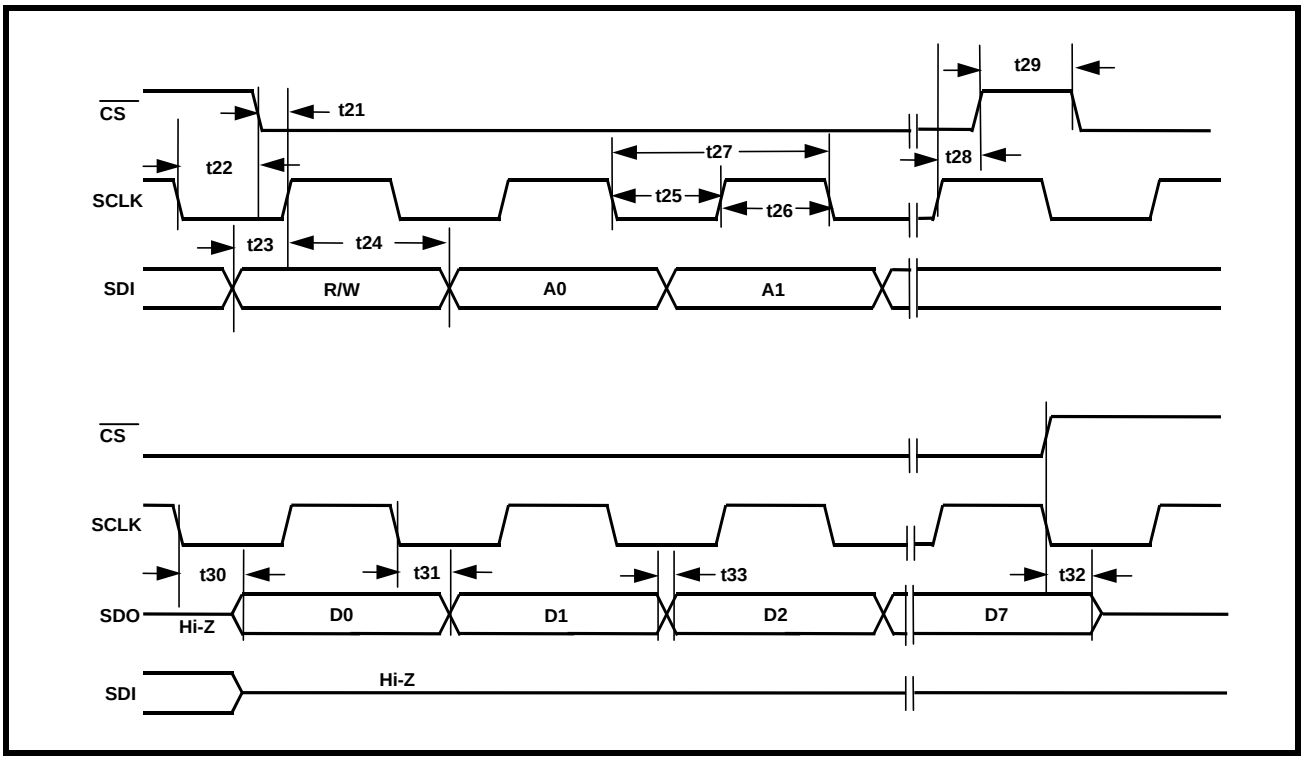


FIGURE 38. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

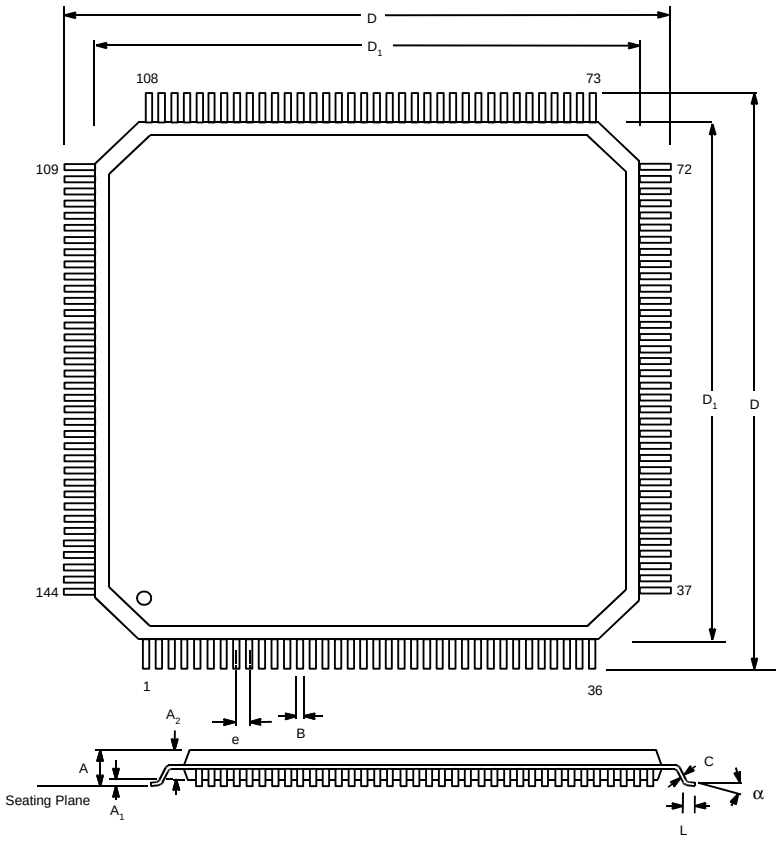


ORDERING INFORMATION

PART #	PACKAGE	OPERATING TEMPERATURE RANGE
XRT73LC04AIV	144 Pin LQFP 20 x 20 x 1.4mm	-40℃ to +8 5℃
THERMAL INFORMATION	Theta-J_A = 24°C/W	Theta-J_C = 5.5°C/W

PACKAGE DIMENSIONS

144 LEAD QUAD FLAT PACK
(20 x 20 x 1.4 mm LQFP)
rev. 1.00



Note: *The control dimension is the millimeter column*

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.055	0.063	1.4	1.6
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.858	0.874	21.8	22.2
D1	0.783	0.791	19.9	20.1
e	0.020 BSC		0.50 BSC	
L	0.018	0.03	0.45	0.75
α	0º	7º	0º	7º
β	0.490	0.510	12.45	12.96

REVISION HISTORY

REV #	DATE	CHANGES MADE
1.0.0	July 2003	Final Release. Changed Theta-JA and Theta-JC. ICC in electrical tables returned to 500mA max for the 4-channel device. Changed TQFP to LQFP.
1.0.1	October 2003	Changed the default register setting for LOSMUT_(n) in CR3.
1.0.2	September 2008	Updated datasheet Headers. Corrected Figure 12 block diagram typo. Redefined t_{22} Serial Processor Interface timing.