



SP508

**Rugged 20Mbps, 8 Channel Multi-Protocol Transceiver
with Programmable DCE/DTE and Termination Resistors**

FEATURES

- 20Mbps Differential Transmission Rates
- 15kV ESD Tolerance for Analog I/Os
- Internal Transceiver Termination Resistors for V.11/V.35
- Interface Modes:
 - ✓ RS-232 (V.28) ✓ EIA-530 (V.10 & V.11)
 - ✓ X.21 (V.11) ✓ EIA-530A (V.10 & V.11)
 - ✓ RS-449/V.36 ✓ V.35
(V.10 & V.11)
- Software Selectable Protocols with 3-Bit Word
- Eight Drivers and Eight Receivers
- V.35/V.11 Receiver Termination Network Disable Option
- Internal Line or Digital Loopback Testing
- Adheres to NET1/NET2 and TBR-2 Requirements

Now Available in Lead Free Packaging

Refer to page 7 for pinout

- Easy Flow-Through Pinout
- +5V Only Operation
- Individual Driver/Receiver Enable/Disable Controls
- Operates in DTE or DCE Mode

APPLICATIONS

- Router
- Frame Relay
- CSU
- DSU
- PBX
- Secure Communication Terminals

DESCRIPTION

The SP508 is a monolithic device that supports eight (8) popular serial interface standards for Wide Area Network (WAN) connectivity. The SP508 is fabricated using a low power BiCMOS process technology, and incorporates a Sipex regulated charge pump allowing +5V only operation. Sipex's patented charge pump provides a regulated output of $\pm 5.8V$, which will provide enough voltage for compliant operation in all modes. Eight (8) drivers and eight (8) receivers can be configured via software for any of the above interface modes at any time. The SP508 requires no additional external components for compliant operation for all of the eight (8) modes of operation other than four capacitors used for the internal charge pump. All necessary termination is integrated within the SP508 and is switchable when V.35 drivers and V.35 receivers, or when V.11 receivers are used. The SP508 provides the controls and transceiver availability for operating as either a DTE or DCE.

Additional features with the SP508 include internal loopback that can be initiated in any of the operating modes by use of the LOOPBACK pin. While in loopback mode, receiver outputs are internally connected to driver inputs creating an internal signal path bypassing the serial communications controller for diagnostic testing. The SP508 also includes a latch enable pin with the driver and receiver address decoder. The internal V.11 or V.35 receiver termination can be switched off using a control pin (TERM_OFF) for monitoring applications. All eight (8) drivers and receivers in the SP508 include separate enable pins for added convenience. The SP508 is ideal for WAN serial ports in networking equipment such as routers, access concentrators, network muxes, DSU/CSU's, networking test equipment, and other access devices.

Applicable U.S. Patents-5,306,954; and others patents pending

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V _{CC}	+7V
Input Voltages:	
Logic	-0.3V to (V _{CC} +0.5V)
Drivers	-0.3V to (V _{CC} +0.5V)
Receivers	±15.5V
Output Voltages:	
Logic	-0.3V to (V _{CC} +0.5V)
Drivers	±12V
Receivers	-0.3V to (V _{CC} +0.5V)
Storage Temperature	-65°C to +150°C
Power Dissipation	1520mW
(derate 19.0mW/°C above +70°C)	
Package Derating:	
θ _{JA}	52.7 °C/W
θ _{JC}	6.5 °C/W

STORAGE CONSIDERATIONS

Due to the relatively large package size, storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 48 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for four hours at 125°C in order to remove moisture prior to soldering. Sipex ships the 100-pin LQFP in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH.

ELECTRICAL SPECIFICATIONS

T_A = 0°C to +70°C and V_{CC} = +4.75V to +5.25V unless otherwise noted. The ♦ denotes the specifications which applies to full temperature range of -40°C to +85°C, unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.	UNITS		CONDITIONS
LOGIC INPUTS						
V _{IL}			0.8	Volts	♦	
V _{IH}	2.0			Volts	♦	
LOGIC OUTPUTS						
V _{OL}		2.4	0.4	Volts	♦	I _{OUT} = -3.2mA
V _{OH}				Volts	♦	I _{OUT} = 1.0mA
V.28 DRIVER						
DC Parameters						
Outputs						
Open Circuit Voltage			±15	Volts	♦	per <i>Figure 1</i>
Loaded Voltage	±5.0		±15	Volts	♦	per <i>Figure 2</i>
Short-Circuit Current			±100	mA	♦	per <i>Figure 4</i> , V _{OUT} =0V
Power-Off Impedance	300			Ω	♦	per <i>Figure 5</i>
AC Parameters						
Outputs						
Transition Time			1.5	μs	♦	per <i>Figure 6</i> ; +3V to -3V
Instantaneous Slew Rate			30	V/μs	♦	per <i>Figure 3</i>
Propagation Delay						
t _{PHL}	0.5	1	5	μs	♦	
t _{PLH}	0.5	1	5	μs	♦	
Max. Transmission Rate	120	230		kbps	♦	
V.28 RECEIVER						
DC Parameters						
Inputs						
Input Impedance	3		7	kΩ	♦	per <i>Figure 7</i>
Open-Circuit Bias			+2.0	Volts	♦	per <i>Figure 8</i>
HIGH Threshold		1.7	3.0	Volts	♦	
LOW Threshold	0.8	1.2		Volts	♦	
AC Parameters						
Propagation Delay						
t _{PHL}	50	100	500	ns	♦	V _{CC} = +5V for AC parameters
t _{PLH}	50	100	500	ns	♦	

ELECTRICAL SPECIFICATIONS

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ and $V_{CC} = +4.75\text{V}$ to $+5.25\text{V}$ unless otherwise noted. The ♦ denotes the specifications which applies to full temperature range of -40°C to $+85^\circ\text{C}$, unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.	UNITS		CONDITIONS
V.28 RECEIVER (cont) AC Parameters (cont.) Max. Transmission Rate	120	235		kbps		
V.10 DRIVER DC Parameters Outputs Open Circuit Voltage Test-Terminated Voltage Short-Circuit Current Power-Off Current AC Parameters Outputs Transition Time Propagation Delay t_{PHL} t_{PLH} Max. Transmission Rate	± 4.0 $0.9V_{OC}$		± 6.0 ± 150 ± 100 200 30 30 120	Volts Volts mA μA ns ns ns kbps	♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦	per <i>Figure 9</i> per <i>Figure 10</i> per <i>Figure 11</i> per <i>Figure 12</i> $V_{CC} = +5\text{V}$ for AC parameters per <i>Figure 13</i> ; 10% to 90%
V.10 RECEIVER DC Parameters Inputs Input Current Input Impedance Sensitivity AC Parameters Propagation Delay t_{PHL} t_{PLH} Max. Transmission Rate	-3.25 4		$+3.25$ ± 0.3 60 60 120	mA k Ω Volts ns ns kbps	♦ ♦ ♦ ♦ ♦ ♦ ♦	per <i>Figures 14</i> and <i>15</i> $V_{CC} = +5\text{V}$ for AC parameters
V.11 DRIVER DC Parameters Outputs Open Circuit Voltage Test Terminated Voltage Balance Offset Short-Circuit Current Power-Off Current AC Parameters Outputs Transition Time Propagation Delay t_{PHL} t_{PLH} Differential Skew $(t_{phl} - t_{plh})$ Max. Transmission Rate Channel to Channel Skew	± 2.0 $0.5V_{OC}$		± 6.0 $0.67V_{OC}$ ± 0.4 $+3.0$ ± 150 ± 100 10 30 30 5 20 2	Volts Volts Volts Volts mA μA ns ns ns ns Mbps ns	♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦	per <i>Figure 16</i> per <i>Figure 17</i> per <i>Figure 17</i> per <i>Figure 17</i> per <i>Figure 18</i> per <i>Figure 19</i> $V_{CC} = +5\text{V}$ for AC parameters per <i>Fig. 21</i> and <i>36</i> ; 10% to 90% Using $C_L = 50\text{pF}$; per <i>Figures 33</i> and <i>36</i> per <i>Figures 33</i> and <i>36</i> per <i>Figures 33</i> and <i>36</i>
V.11 RECEIVER DC Parameters Inputs Common Mode Range Sensitivity	-7		$+7$ ± 0.2	Volts Volts	♦ ♦	

ELECTRICAL SPECIFICATIONS

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ and $V_{CC} = +4.75\text{V}$ to $+5.25\text{V}$ unless otherwise noted. The \blacklozenge denotes the specifications which applies to full temperature range of -40°C to $+85^\circ\text{C}$, unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.11 RECEIVER (cont)					
DC Parameters (cont.)					
Input Current	-3.25		±3.25	mA	\blacklozenge per <i>Figure 20</i> and <i>22</i> , power on or off
Current w/ 100 Ω Termination			±60.75	mA	\blacklozenge per <i>Figure 23</i> and <i>24</i>
Input Impedance	4			k Ω	\blacklozenge
AC Parameters					
Propagation Delay					$V_{CC} = +5\text{V}$ for AC parameters Using $C_L = 50\text{pF}$;
t_{PHL}		30	60	ns	\blacklozenge per <i>Figures 33</i> and <i>38</i>
t_{PLH}		30	60	ns	\blacklozenge per <i>Figures 33</i> and <i>38</i>
Skew($t_{PHL} - t_{PLH}$)		5	10	ns	\blacklozenge per <i>Figure 33</i>
Max. Transmission Rate	20			Mbps	\blacklozenge
Channel to Channel Skew		2		ns	\blacklozenge
V.35 DRIVER					
DC Parameters					
Outputs					
Test Terminated Voltage	±0.44		±0.66	Volts	\blacklozenge per <i>Figure 25</i>
Offset			±0.6	Volts	\blacklozenge per <i>Figure 25</i>
Output Overshoot	-0.2V _{ST}		+0.2V _{ST}	Volts	\blacklozenge per <i>Figure 25</i> ; $V_{ST} = \text{Steady state value}$
Source Impedance	50		150	Ω	\blacklozenge per <i>Figure 27</i> ; $Z_S = V_2/V_1 \times 50$
Short-Circuit Impedance	135		165	Ω	\blacklozenge per <i>Figure 28</i>
AC Parameters					
Outputs					
Transition Time		7	20	ns	\blacklozenge per <i>Figure 29</i> ; 10% to 90%
Propagation Delay					
t_{PHL}		30	60	ns	\blacklozenge per <i>Figure 33</i> and <i>36</i> ; $C_L = 20\text{pF}$
t_{PLH}		30	60	ns	\blacklozenge per <i>Figure 33</i> and <i>36</i> ; $C_L = 20\text{pF}$
Differential Skew		5	10	ns	\blacklozenge per <i>Figure 33</i> and <i>36</i> ; $C_L = 20\text{pF}$
($t_{PHL} - t_{PLH}$)					
Max. Transmission Rate	20			Mbps	\blacklozenge
Channel to Channel Skew		5		ns	\blacklozenge
V.35 RECEIVER					
DC Parameters					
Inputs					
Sensitivity		±50	±200	mV	\blacklozenge
Source Impedance	90		110	Ω	\blacklozenge per <i>Figure 30</i> ; $Z_S = V_2/V_1 \times 50\Omega$
Short-Circuit Impedance	135		165	Ω	\blacklozenge per <i>Figure 31</i>
AC Parameters					
Propagation Delay					$V_{CC} = +5\text{V}$ for AC parameters
t_{PHL}		30	60	ns	\blacklozenge per <i>Figure 33</i> and <i>38</i> ; $C_L = 20\text{pF}$
t_{PLH}		30	60	ns	\blacklozenge per <i>Figure 33</i> and <i>38</i> ; $C_L = 20\text{pF}$
Skew($t_{PHL} - t_{PLH}$)		5	10	ns	\blacklozenge per <i>Figure 33</i> ; $C_L = 20\text{pF}$
Max. Transmission Rate	20			Mbps	\blacklozenge
Channel to Channel Skew		2		ns	\blacklozenge
TRANSCEIVER LEAKAGE CURRENT					
Driver Output 3-State Current		500		μA	per <i>Figure 32</i> ; Drivers disabled T_X & R_X disabled, 0.4V - V_O - 2.4V
Rcvr Output 3-State Current		1	10	μA	
POWER REQUIREMENTS					
V_{CC}	4.75	5.00	5.25	Volts	All I_{CC} values are with $V_{CC} = +5\text{V}$ $f_{IN} = 120\text{kbps}$; Drivers active & loaded $f_{IN} = 10\text{Mbps}$; Drivers active & loaded $f_{IN} = 10\text{Mbps}$; Drivers active & loaded V.35 @ $f_{IN} = 10\text{Mbps}$, V.28 @ 20kbps $f_{IN} = 10\text{Mbps}$; Drivers active & loaded
I_{CC} (Shutdown Mode)		1		μA	
(V.28/RS-232)		95		mA	
(V.11/RS-422)		230		mA	
(EIA-530 & RS-449)		270		mA	
(V.35)		170		mA	
(EIA-530A)		200		mA	

OTHER AC CHARACTERISTICS

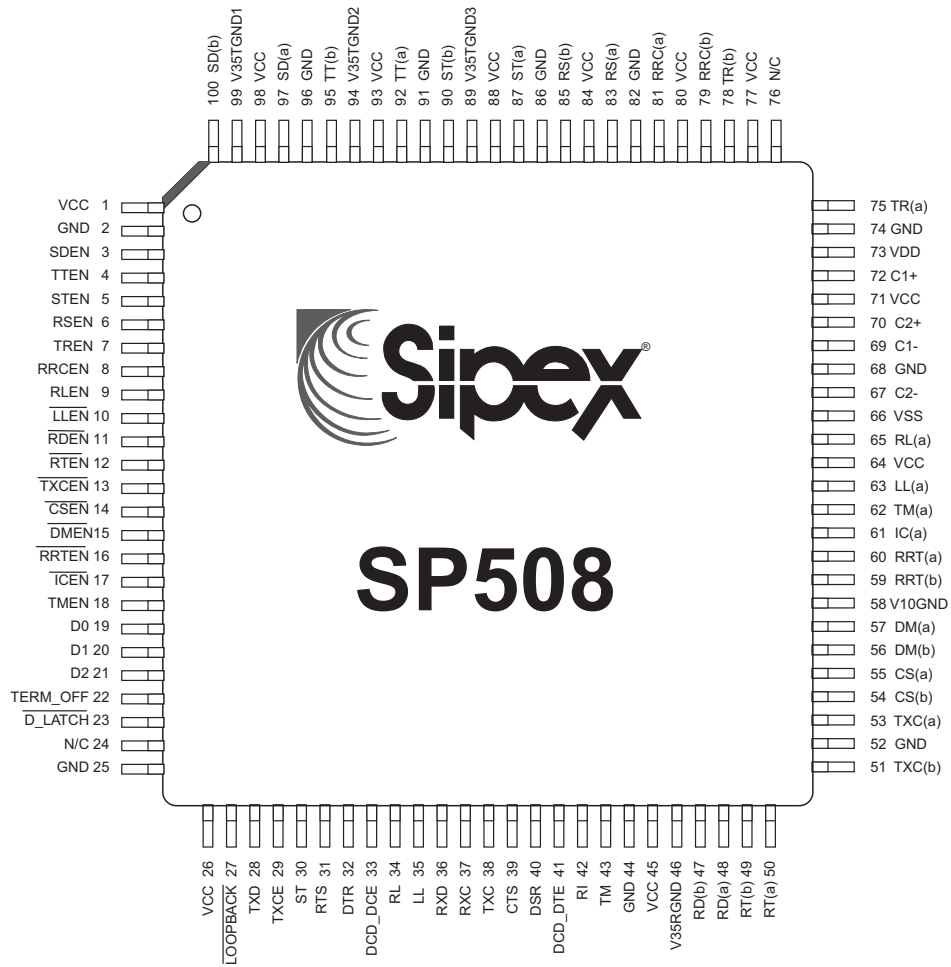
$T_A = +25^\circ\text{C}$ and $V_{CC} = +5.0\text{V}$ unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232/V.28					
t_{PZL} : Tri-state to Output LOW		0.11	5.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_2 closed
t_{PZH} : Tri-state to Output HIGH		0.11	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.05	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_2 closed
t_{PHZ} : Output HIGH to Tri-state		0.05	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_2 closed
RS-423/V.10					
t_{PZL} : Tri-state to Output LOW		0.07	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_2 closed
t_{PZH} : Tri-state to Output HIGH		0.05	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.55	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_2 closed
t_{PHZ} : Output HIGH to Tri-state		0.12	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_2 closed
RS-422/V.11					
t_{PZL} : Tri-state to Output LOW		0.04	10.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 37; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.05	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 37; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.03	2.0	μs	$C_L = 15\text{pF}$, Fig. 34 & 37; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.11	2.0	μs	$C_L = 15\text{pF}$, Fig. 34 & 37; S_2 closed
V.35					
t_{PZL} : Tri-state to Output LOW		0.85	10.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 37; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.36	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 37; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.06	2.0	μs	$C_L = 15\text{pF}$, Fig. 34 & 37; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.05	2.0	μs	$C_L = 15\text{pF}$, Fig. 34 & 37; S_2 closed
RECEIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232/V.28					
t_{PZL} : Tri-state to Output LOW		0.05	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 40; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.05	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 40; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.65	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 40; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.65	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 40; S_2 closed
RS-423/V.10					
t_{PZL} : Tri-state to Output LOW		0.04	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 40; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.03	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 40; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.03	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 40; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.03	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 40; S_2 closed

OTHER AC CHARACTERISTICS (Continued)

$T_A = +25^\circ\text{C}$ and $V_{CC} = +5.0\text{V}$ unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-422/V.11					
t_{PZL} : Tri-state to Output LOW		0.04	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 39 ; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.03	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 39 ; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.03	2.0	μs	$C_L = 15\text{pF}$, Fig. 35 & 39 ; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.03	2.0	μs	$C_L = 15\text{pF}$, Fig. 35 & 39 ; S_2 close
V.35					
t_{PZL} : Tri-state to Output LOW		0.04	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 39 ; S_1 closed
t_{PZH} : Tri-state to Output HIGH		0.03	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 39 ; S_2 closed
t_{PLZ} : Output LOW to Tri-state		0.03	2.0	μs	$C_L = 15\text{pF}$, Fig. 35 & 39 ; S_1 closed
t_{PHZ} : Output HIGH to Tri-state		0.03	2.0	μs	$C_L = 15\text{pF}$, Fig. 35 & 39 ; S_2 closed
TRANSCEIVER TO TRANSCEIVER SKEW (per Figures 32, 33, 36, 38)					
RS-232 Driver		100		ns	$[(t_{\text{phl}})_{\text{Tx1}} - (t_{\text{phl}})_{\text{Txn}}]$
		100		ns	$[(t_{\text{plh}})_{\text{Tx1}} - (t_{\text{plh}})_{\text{Txn}}]$
RS-232 Receiver		20		ns	$[(t_{\text{phl}})_{\text{Rx1}} - (t_{\text{phl}})_{\text{Rxn}}]$
		20		ns	$[(t_{\text{plh}})_{\text{Rx1}} - (t_{\text{plh}})_{\text{Rxn}}]$
RS-422 Driver		2		ns	$[(t_{\text{phl}})_{\text{Tx1}} - (t_{\text{phl}})_{\text{Txn}}]$
		2		ns	$[(t_{\text{plh}})_{\text{Tx1}} - (t_{\text{plh}})_{\text{Txn}}]$
RS-422 Receiver		2		ns	$[(t_{\text{phl}})_{\text{Rx1}} - (t_{\text{phl}})_{\text{Rxn}}]$
		3		ns	$[(t_{\text{plh}})_{\text{Rx1}} - (t_{\text{plh}})_{\text{Rxn}}]$
RS-423 Driver		5		ns	$[(t_{\text{phl}})_{\text{Tx2}} - (t_{\text{phl}})_{\text{Txn}}]$
		5		ns	$[(t_{\text{plh}})_{\text{Tx2}} - (t_{\text{plh}})_{\text{Txn}}]$
RS-423 Receiver		5		ns	$[(t_{\text{phl}})_{\text{Rx2}} - (t_{\text{phl}})_{\text{Rxn}}]$
		5		ns	$[(t_{\text{plh}})_{\text{Rx2}} - (t_{\text{plh}})_{\text{Rxn}}]$
V.35 Driver		2		ns	$[(t_{\text{phl}})_{\text{Tx1}} - (t_{\text{phl}})_{\text{Txn}}]$
		2		ns	$[(t_{\text{plh}})_{\text{Tx1}} - (t_{\text{plh}})_{\text{Txn}}]$
V.35 Receiver		2		ns	$[(t_{\text{phl}})_{\text{Rx1}} - (t_{\text{phl}})_{\text{Rxn}}]$
		2		ns	$[(t_{\text{plh}})_{\text{Rx1}} - (t_{\text{plh}})_{\text{Rxn}}]$



PIN DESCRIPTION

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	VCC	5V Power Supply Input	51	TxC(b)	TxC Non-Inverting Input
2	GND	Signal Ground	52	GND	Signal Ground
3	SDEN	TxD Driver Enable Input	53	TxC(a)	TxC Inverting Input
4	TTEN	TxCE Driver Enable Input	54	CS(b)	CTS Non-Inverting Input
5	STEN	ST Driver Enable Input	55	CS(a)	CTS Inverting Input
6	RSEN	RTS Driver Enable Input	56	DM(b)	DSR Non-Inverting Input
7	TREN	DTR Driver Enable Input	57	DM(a)	DSR Inverting Input
8	RRCEN	DCD Driver Enable Input	58	GNDV10	V.10 Rx Reference Node
9	RLEN	RL Driver Enable Input	59	RRT(b)	DCD _{DTE} Non-Inverting Input
10	LLEN#	LL Driver Enable Input	60	RRT(a)	DCD _{DTE} Inverting Input
11	RDEN#	RxD Receiver Enable Input	61	IC	RI Receiver Input
12	RTEN#	RxC Receiver Enable Input	62	TM(a)	TM Receiver Input
13	TxCEN#	TxC Receiver Enable Input	63	LL(a)	LL Driver Output
14	CSEN#	CTS Receiver Enable Input	64	VCC	Power Supply Input
15	DMEN#	DSR Receiver Enable Input	65	RL(a)	RL Driver Output
16	RRTEN#	DCD _{DTE} Receiver Enable Input	66	VSS1	-2xVCC Charge Pump Output
17	ICEN#	RI Receiver Enable Input	67	C2N	Charge Pump Capacitor
18	TMEN	TM Receiver Enable Input	68	GND	Signal Ground
19	D0	Mode Select Input	69	C1N	Charge Pump Capacitor
20	D1	Mode Select Input	70	C2P	Charge Pump Capacitor
21	D2	Mode Select Input	71	VCC	Power Supply Input
22	TERM_OFF	Termination Disable Input	72	C1P	Charge Pump Capacitor
23	D_LATCH#	Decoder Latch Input	73	VDD	2xVCC Charge Pump Output
24	NC	No Connect	74	GND	Signal Ground
25	GND	Signal Ground	75	TR(a)	DTR Inverting Output
26	VCC	5V Power Supply Input	76	NC	No Connect
27	LOOPBACK#	Loopback Mode Enable Input	77	VCC	Power Supply Input
28	TxD	TxD Driver TTL Input	78	TR(b)	DTR Non-Inverting Output
29	TxCE	TxCE Driver TTL Input	79	RRC(b)	DCD Non-Inverting Output
30	ST	ST Driver TTL Input	80	VCC	Power Supply Input
31	RTS	RTS Driver TTL Input	81	RRC(a)	DCD Inverting Output
32	DTR	DTR Driver TTL Input	82	GND	Signal Ground
33	DCD_DCE	DCD _{DCE} Driver TTL Input	83	RS(a)	RTS Inverting Output
34	RL	RL Driver TTL Input	84	VCC	Power Supply Input
35	LL	LL Driver TTL Input	85	RS(b)	RTS Non-Inverting Output
36	RxD	RxD Receiver TTL Output	86	GND	Signal Ground
37	RxC	RxC Receiver TTL Output	87	ST(a)	ST Inverting Output
38	TxC	TxC Receiver TTL Output	88	VCC	Power Supply Input
39	CTS	CTS Receiver TTL Output	89	V35TGND3	ST Termination Reference
40	DSR	DSR Receiver TTL Output	90	ST(b)	ST Non-Inverting Output
41	DCD_DTE	DCD _{DTE} Receiver TTL Output	91	GND	Signal Ground
42	RI	RI Receiver TTL Output	92	TT(a)	TxCE Inverting Output
43	TM	TM Receiver TTL Output	93	VCC	5V Power Supply Input
44	GND	Signal Ground	94	V35TGND2	ST Termination Reference
45	VCC	Power Supply Input	95	TT(b)	TxCE Non-Inverting Output
46	V35RGND	Receiver Termination Reference	96	GND	Signal Ground
47	RD(b)	RxD Non-Inverting Input	97	SD(a)	TxD Inverting Output
48	RD(a)	RxD Inverting Input	98	VCC	5V Power Supply Input
49	RT(b)	RxC Non-Inverting Input	99	V35TGND1	ST Termination Reference
50	RT(a)	RxC Inverting Input	100	SD(b)	TxD Non-Inverting Output

SP508 Pin Designation						
SP508CF	SP508CB	DESIG		SP508CF	SP508CB	DESIG
1	A2	VCC		51	N12	TxC(B)
2	B2	GND		52	N13	GND
3	B1	SDEN		53	M14	TxC(A)
4	C2	TTEN		54	M13	CS(B)
5	D1	STEN		55	L14	CS(A)
6	E2	RSEN		56	K14	DM(B)
7	F1	TREN		57	J14	DM(A)
8	F3	RRCEN		58	J12	V10GND
9	G2	RLEN		59	H13	RRT(B)
10	G1	LLEN#		60	H14	RRT(A)
11	G3	RDEN#		61	H12	IC(A)
12	H3	RTEN#		62	G12	TM(A)
13	H1	TxCEN#		63	G14	LL(A)
14	H2	CSEN#		64	G13	VCC
15	J2	DMEN#		65	F14	RL(A)
16	J3	RRTEN#		66	F13	VSS
17	K1	ICEN#		67	F12	C2-
18	K2	TMEN		68	E14	GND
19	L1	D0		69	E13	C1-
20	L2	D1		70	D14	C2+
21	L3	D2		71	D13	VCC
22	M2	TERM_OFF		72	C14	C1+
23	N1	D_LATCH#		73	B14	VDD
24		N/C		74	A14	GND
25	P1	GND		75	A13	TR(A)
26	P2	VCC		76		NC
27	P3	LOOPBACK#		77	A12	VCC
28	N3	TxD		78	B12	TR(B)
29	M3	TxCE		79	C12	RRC(A)
30	N4	ST		80	B11	VCC
31	P4	RTS		81	A11	RRC(A)
32	M4	DTR		82	C11	GND
33	N5	DCD_DCE		83	B10	RS(A)
34	P5	RL		84	A10	VCC
35	M5	LL		85	C10	RS(B)
36	N6	RxD		86	A9	GND
37	M6	RxC		87	C9	ST(A)
38	N7	TxC		88	A8	VCC
39	P7	CTS		89	C8	V35TGND3
40	M7	DSR		90	A7	ST(B)
41	P8	DCD_DTE		91	B7	GND
42	N8	RI		92	A6	TT(A)
43	P9	TM		93	B6	VCC
44	M9	GND		94	C6	V35TGND2
45	P10	VCC		95	A5	TT(B)
46	N10	V35RGND		96	B5	GND
47	M10	RD(B)		97	C5	SD(A)
48	P11	RD(A)		98	B4	VCC
49	N11	RT(B)		99	C4	V35TGND1
50	M11	RT(A)		100	B3	SD(B)

SP508 Driver Table

Driver Output Pin	V.35 Mode	EIA-530 Mode	RS-232 Mode (V.28)	EIA-530A Mode	RS-449 Mode (V.36)	X.21 Mode (V.11)	Shutdown	Suggested Signal
MODE (D0, D1, D2)	001	010	011	100	101	110	111	
T ₁ OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxD(a)
T ₁ OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxD(b)
T ₂ OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxCE(a)
T ₂ OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxCE(b)
T ₃ OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxC_DCE(a)
T ₃ OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxC_DCE(b)
T ₄ OUT(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	RTS(a)
T ₄ OUT(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	RTS(b)
T ₅ OUT(a)	V.28	V.11	V.28	V.10	V.11	V.11	High-Z	DTR(a)
T ₅ OUT(b)	High-Z	V.11	High-Z	High-Z	V.11	V.11	High-Z	DTR(b)
T ₆ OUT(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	DCD_DCE(a)
T ₆ OUT(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	DCD_DCE(b)
T ₇ OUT(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	RL
T ₈ OUT(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	LL

Table 1. Driver Mode Selection

SP508 Receiver Table

Receiver Input Pin	V.35 Mode	EIA-530 Mode	RS-232 Mode (V.28)	EIA-530A Mode	RS-449 Mode (V.36)	X.21 Mode (V.11)	Shutdown	Suggested Signal
MODE (D0, D1, D2)	001	010	011	100	101	110	111	
R ₁ IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	RxD(a)
R ₁ IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	RxD(b)
R ₂ IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	RxC(a)
R ₂ IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	RxC(b)
R ₃ IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxC_DTE(a)
R ₃ IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxC_DTE(b)
R ₄ IN(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	CTS(a)
R ₄ IN(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	CTS(b)
R ₅ IN(a)	V.28	V.11	V.28	V.10	V.11	V.11	High-Z	DSR(a)
R ₅ IN(b)	High-Z	V.11	High-Z	High-Z	V.11	V.11	High-Z	DSR(b)
R ₆ IN(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	DCD_DTE(a)
R ₆ IN(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	DCD_DTE(b)
R ₇ IN(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	RI
R ₈ IN(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	TM

Table 2. Receiver Mode Selection

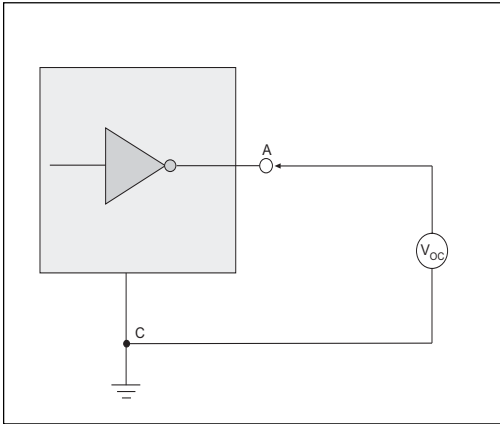


Figure 1. V.28 Driver Output Open Circuit Voltage

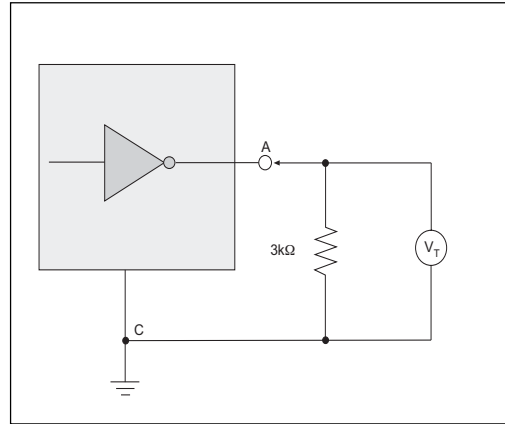


Figure 2. V.28 Driver Output Loaded Voltage

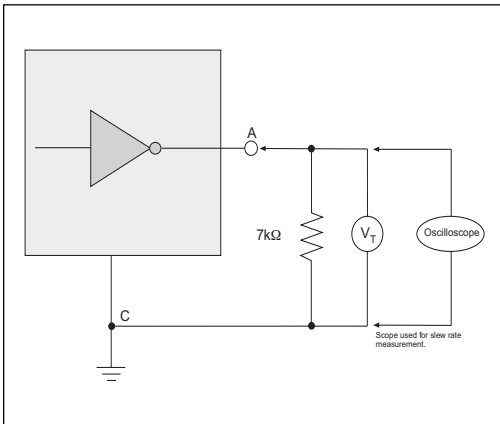


Figure 3. V.28 Driver Output Slew Rate

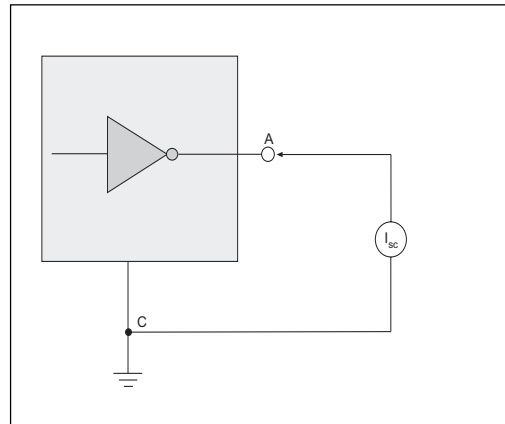


Figure 4. V.28 Driver Output Short-Circuit Current

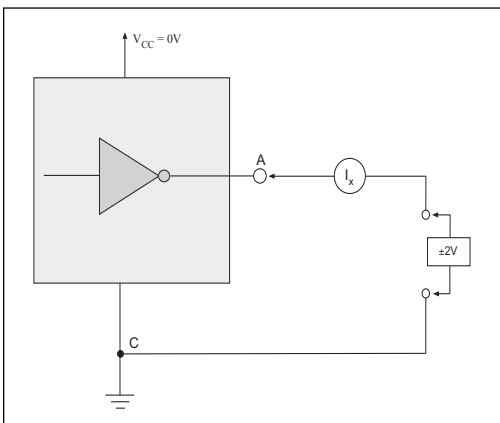


Figure 5. V.28 Driver Output Power-Off Impedance

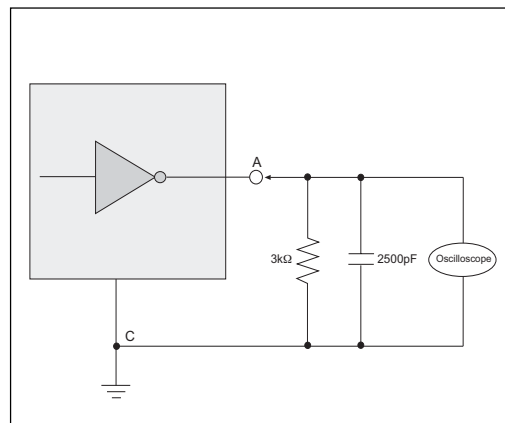


Figure 6. V.28 Driver Output Rise/Fall Times

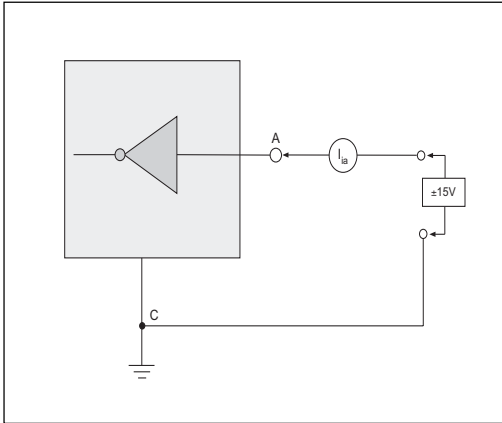


Figure 7. V.28 Receiver Input Impedance

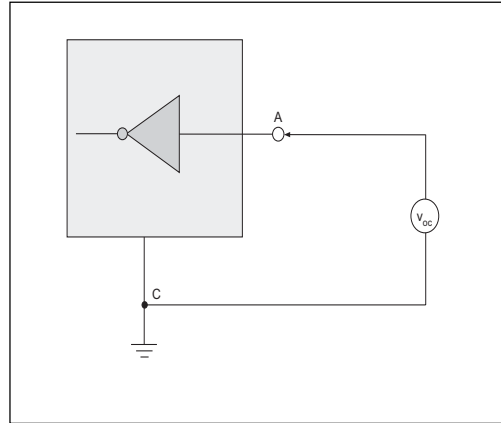


Figure 8. V.28 Receiver Input Open Circuit Bias

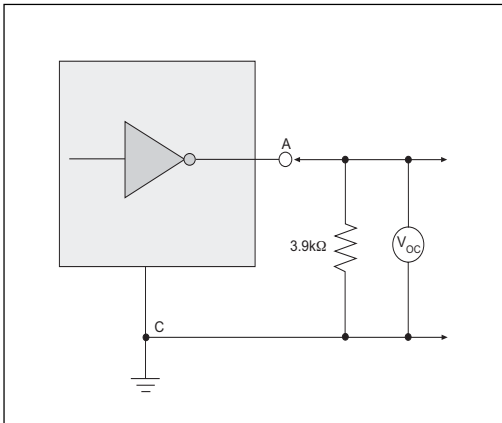


Figure 9. V.10 Driver Output Open-Circuit Voltage

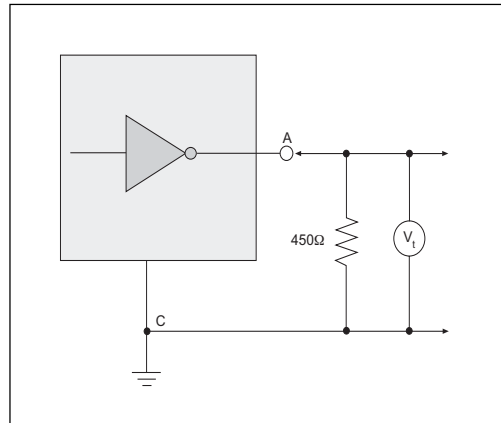


Figure 10. V.10 Driver Output Test Terminated Voltage

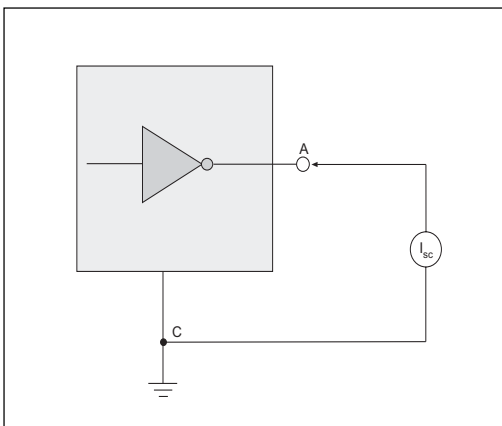


Figure 11. V.10 Driver Output Short-Circuit Current

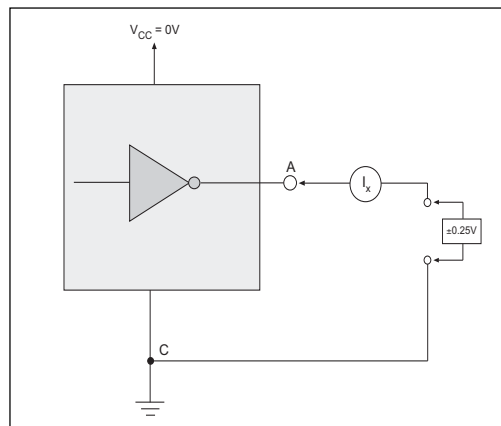


Figure 12. V.10 Driver Output Power-Off Current

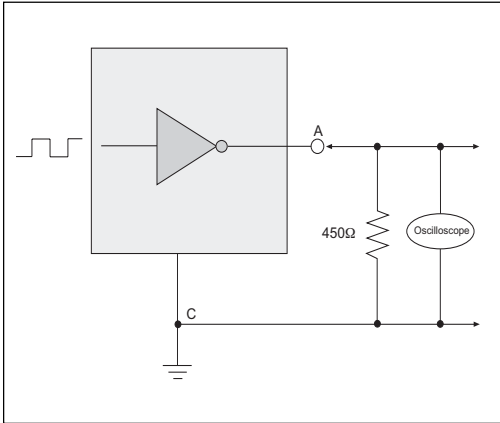


Figure 13. V.10 Driver Output Transition Time

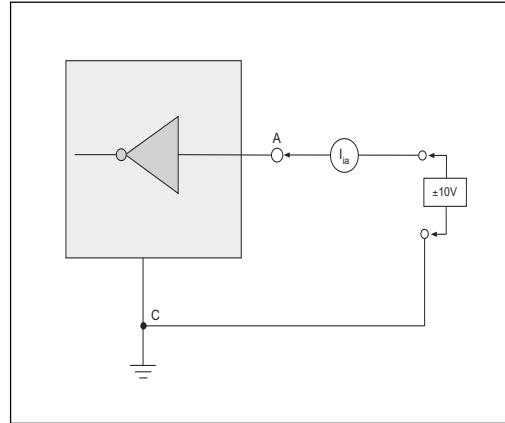


Figure 14. V.10 Receiver Input Current

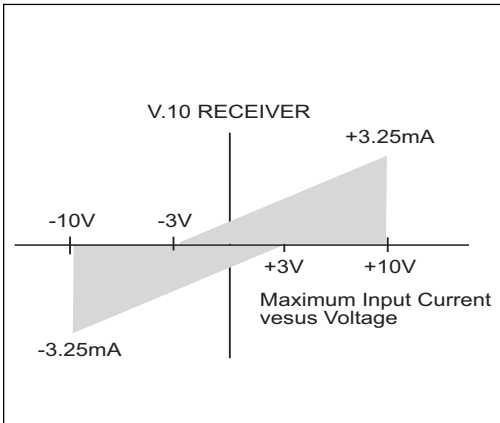


Figure 15. V.10 Receiver Input IV Graph

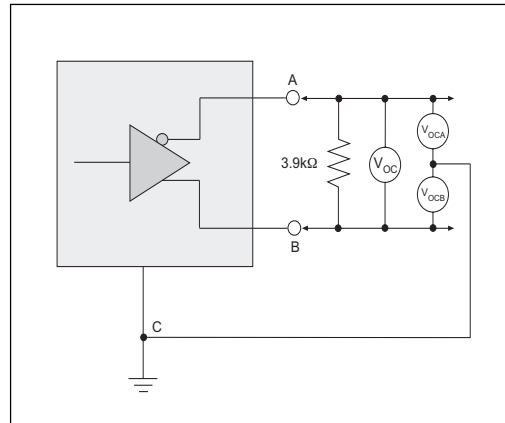


Figure 16. V.11 Driver Output Open-Circuit Voltage

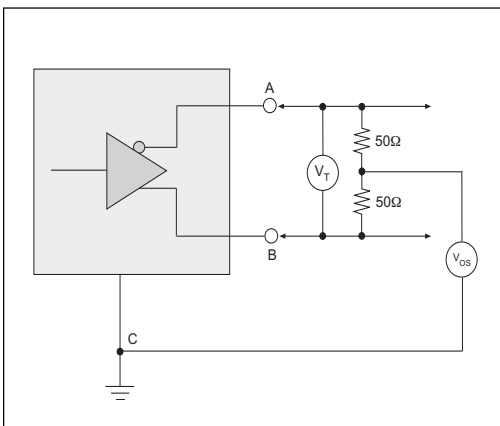


Figure 17. V.11 Driver Output Test Terminated Voltage

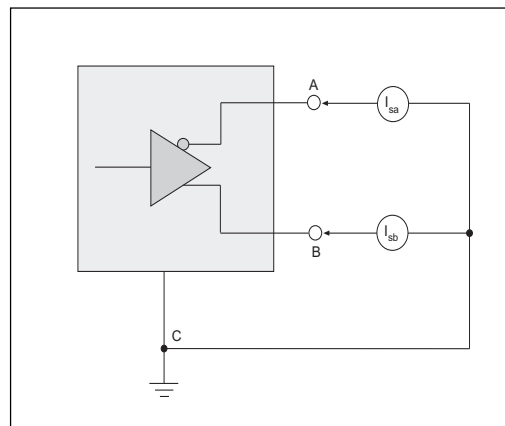


Figure 18. V.11 Driver Output Short-Circuit Current

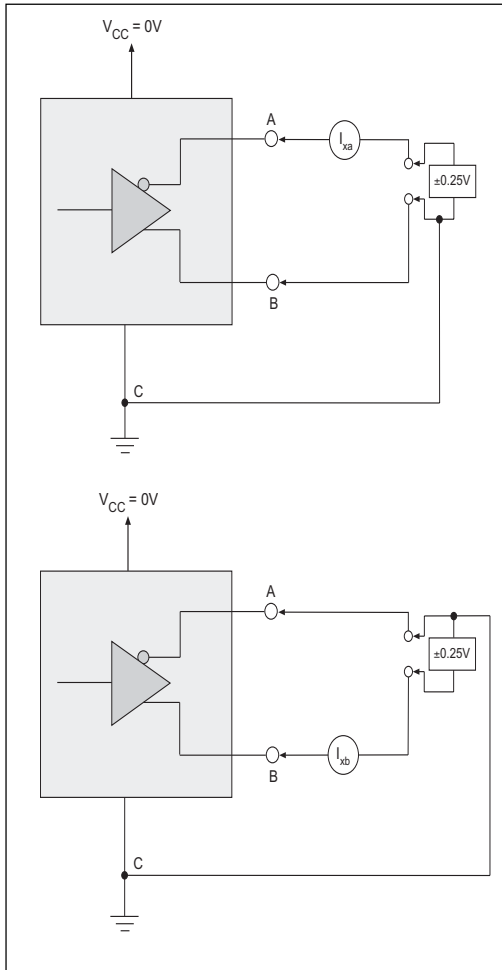


Figure 19. V.11 Driver Output Power-Off Current

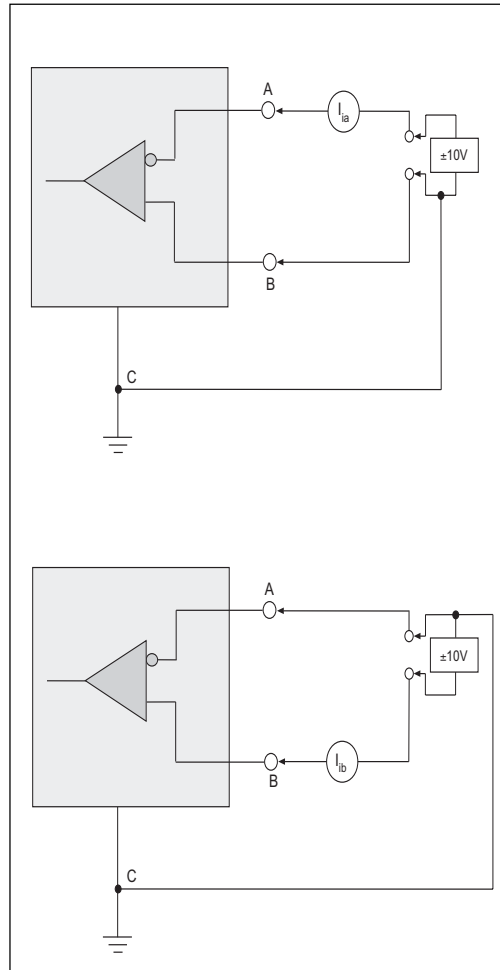


Figure 20. V.11 Receiver Input Current

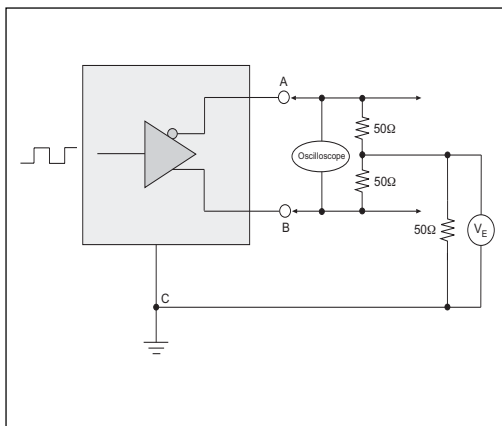


Figure 21. V.11 Driver Output Rise/Fall Time

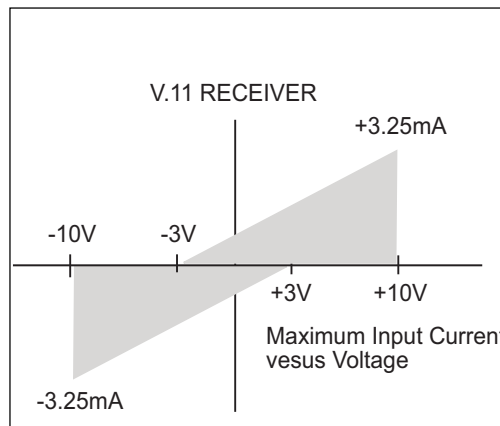


Figure 22. V.11 Receiver Input IV Graph

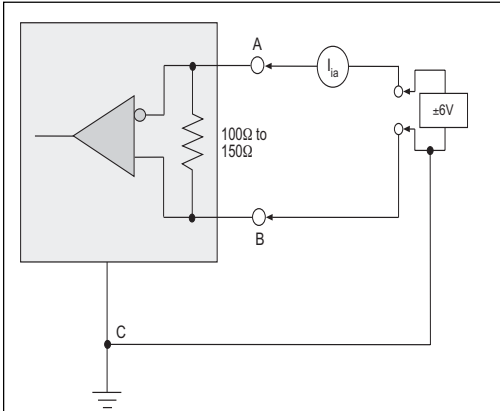


Figure 23. V.11 Receiver Input Current w/ Termination

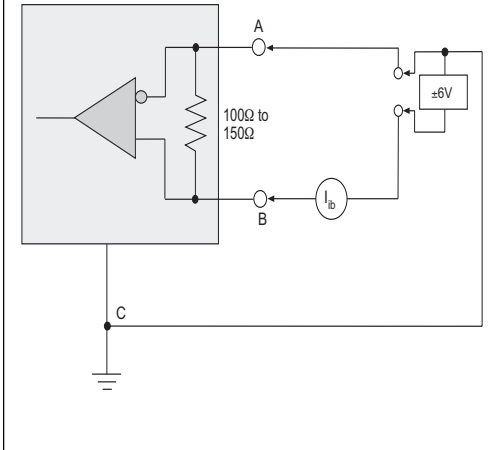


Figure 26. V.35 Driver Output Offset Voltage

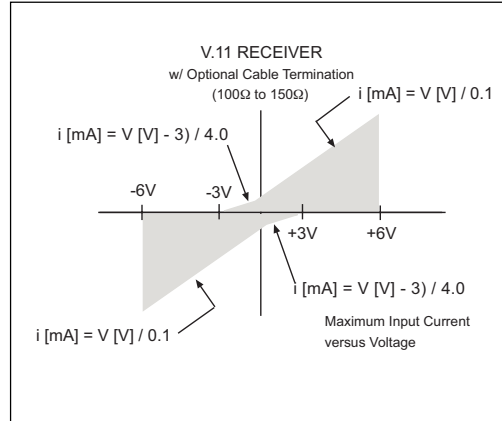


Figure 24. V.11 Receiver Input Graph w/ Termination

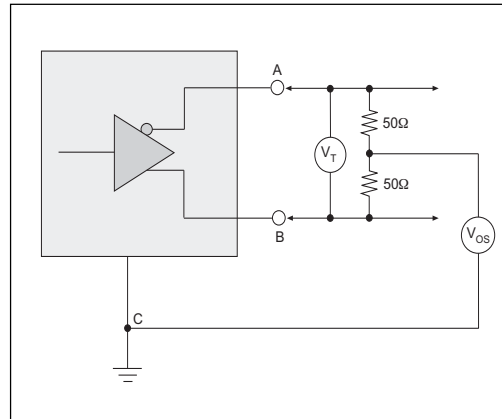


Figure 25. V.35 Driver Output Test Terminated Voltage

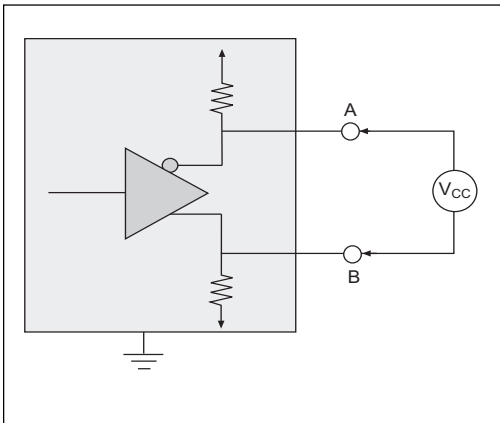


Figure 27. V.35 Driver Output Source Impedance

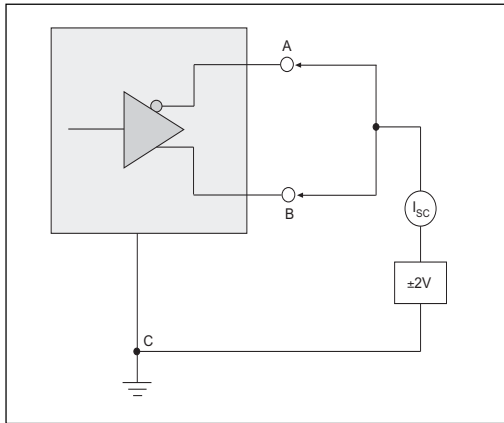


Figure 28. V.35 Driver Output Short-Circuit Impedance

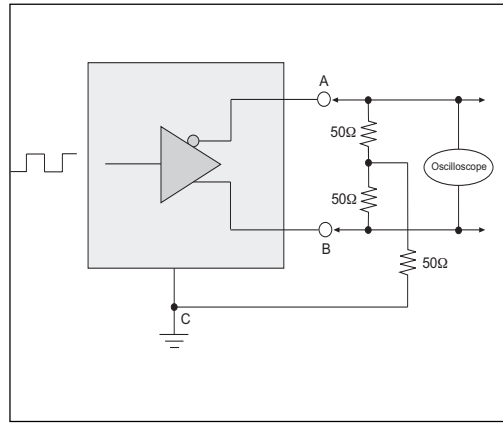


Figure 29. V.35 Driver Output Rise/Fall Time

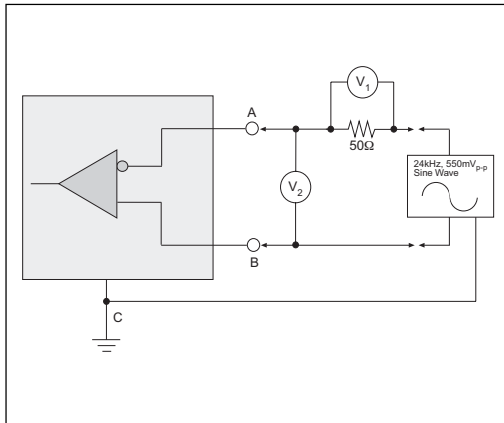


Figure 30. V.35 Receiver Input Source Impedance

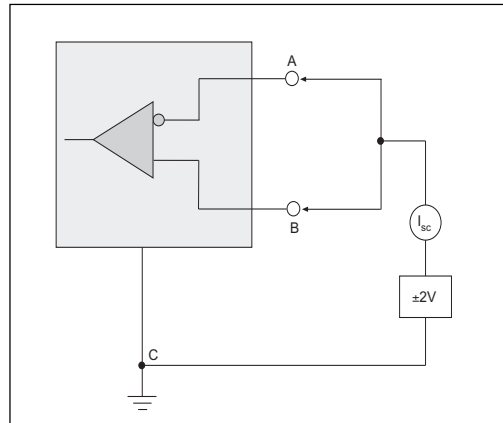


Figure 31. V.35 Receiver Input Short-Circuit Impedance

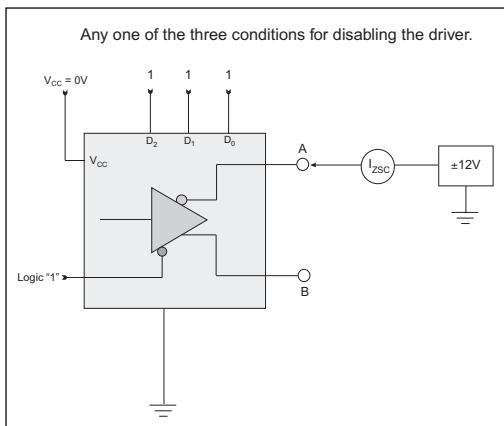


Figure 32. Driver Output Leakage Current Test

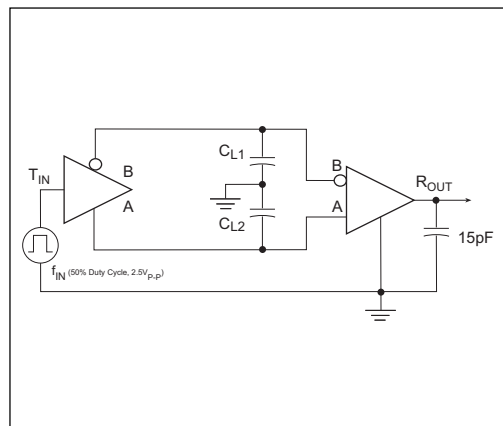


Figure 33. Driver/Receiver Timing Test Circuit

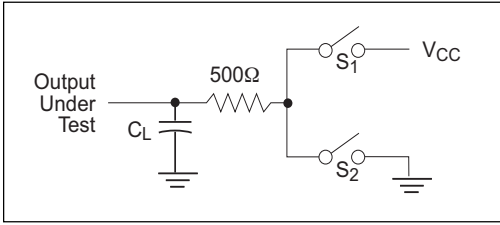


Figure 34. Driver Timing Test Load Circuit

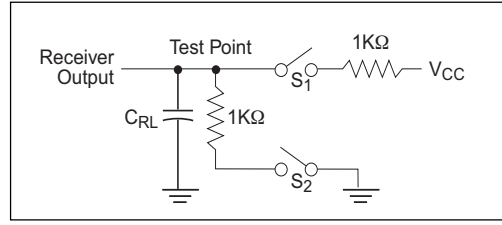


Figure 35. Receiver Timing Test Load Circuit

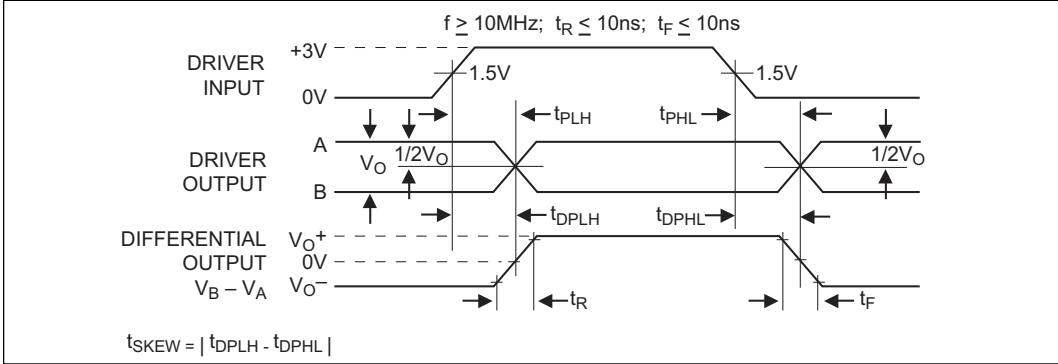


Figure 36. Driver Propagation Delays

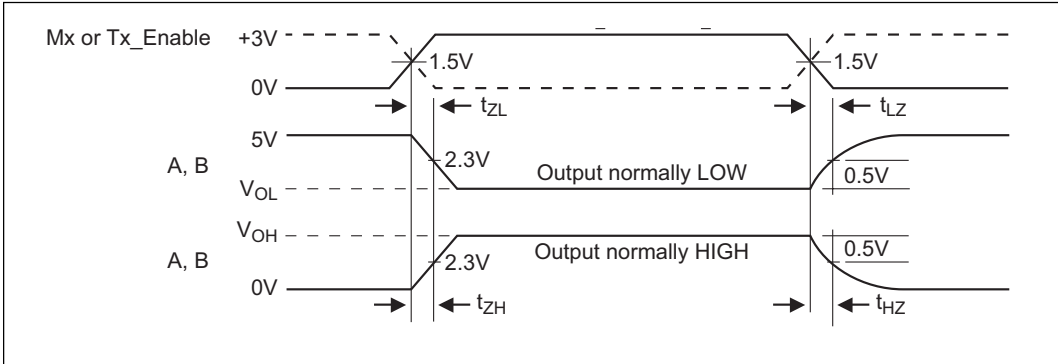


Figure 37. Driver Enable and Disable Times

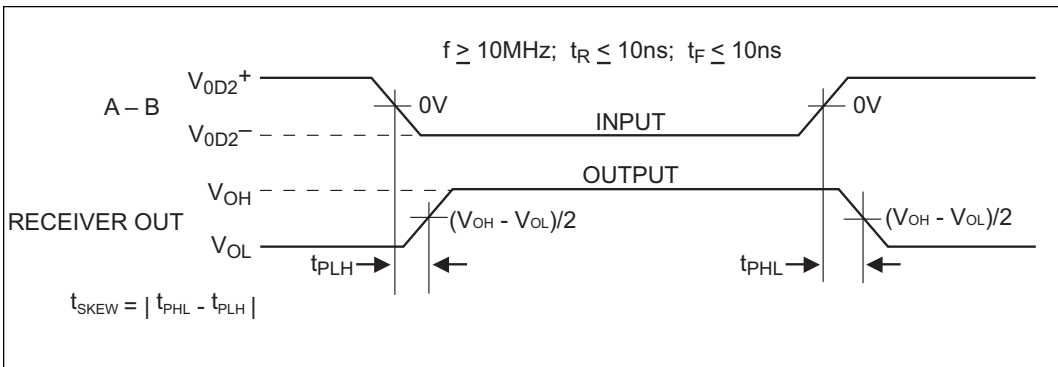


Figure 38. Receiver Propagation Delays

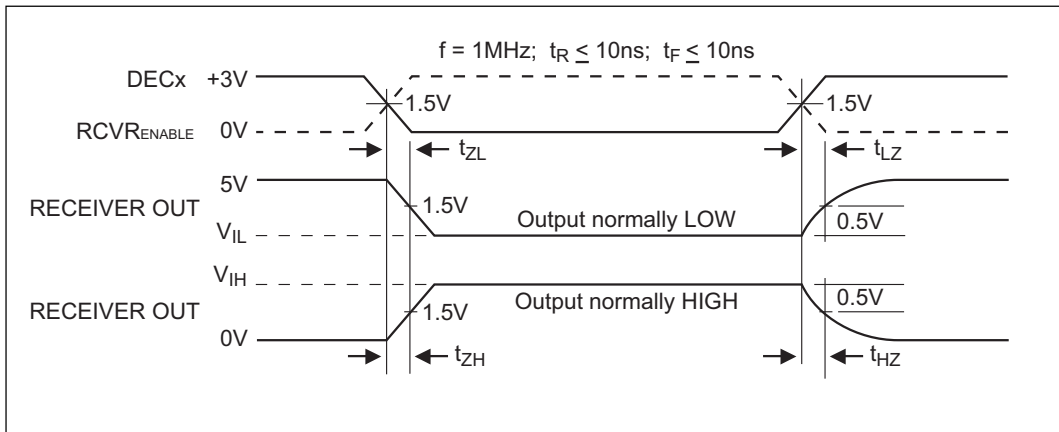


Figure 39. Receiver Enable and Disable Times

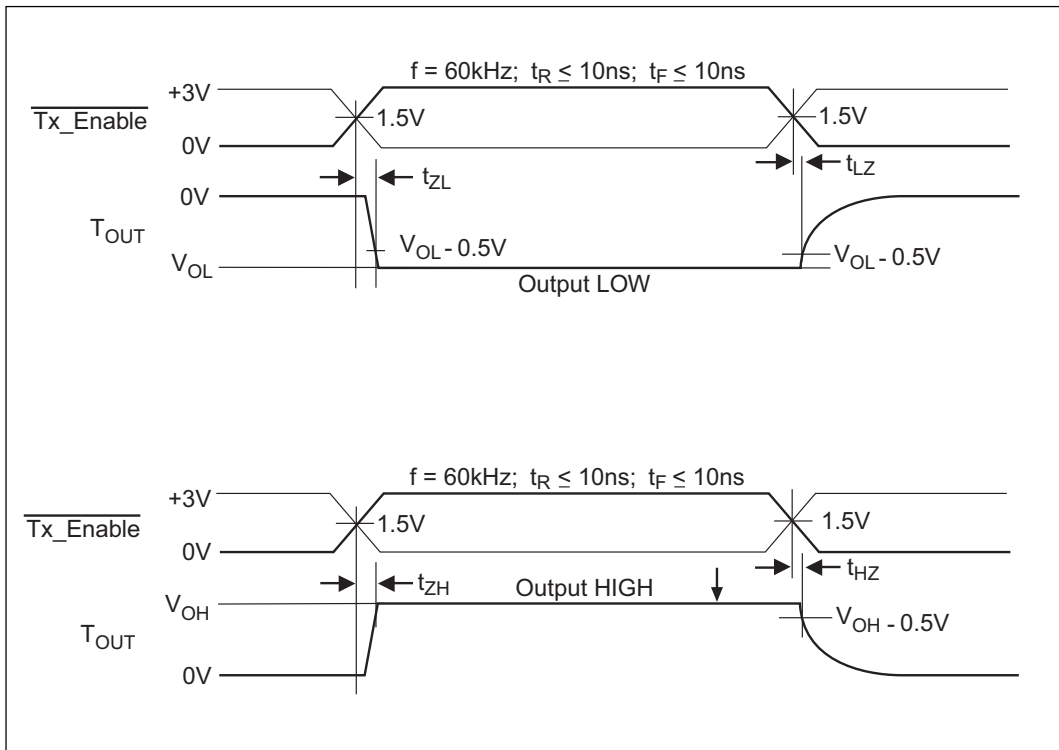


Figure 40. V.28 (RS-232) and V.10 (RS-423) Driver Enable and Disable Times

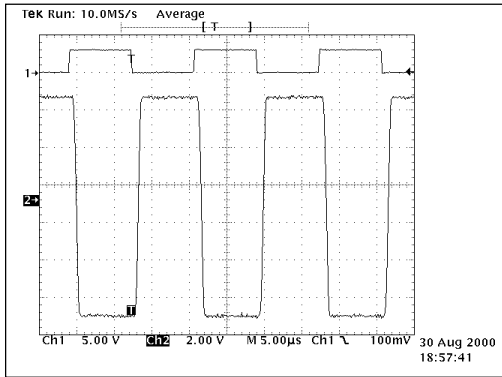


Figure 41. Typical V.28 Driver Output Waveform

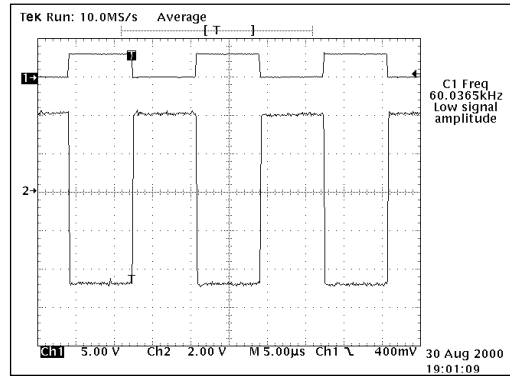


Figure 42. Typical V.10 Driver Output Waveform

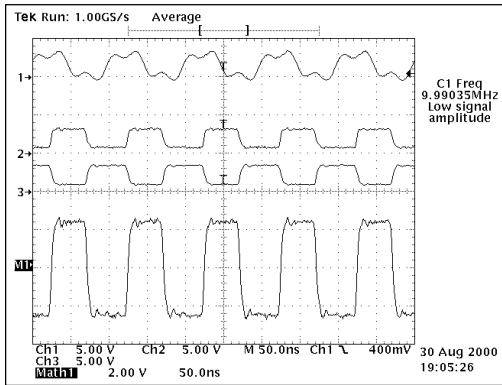


Figure 43. Typical V.11 Driver Output Waveform

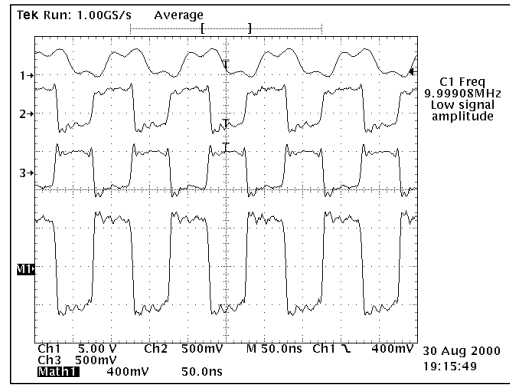


Figure 44. Typical V.35 Driver Output Waveform

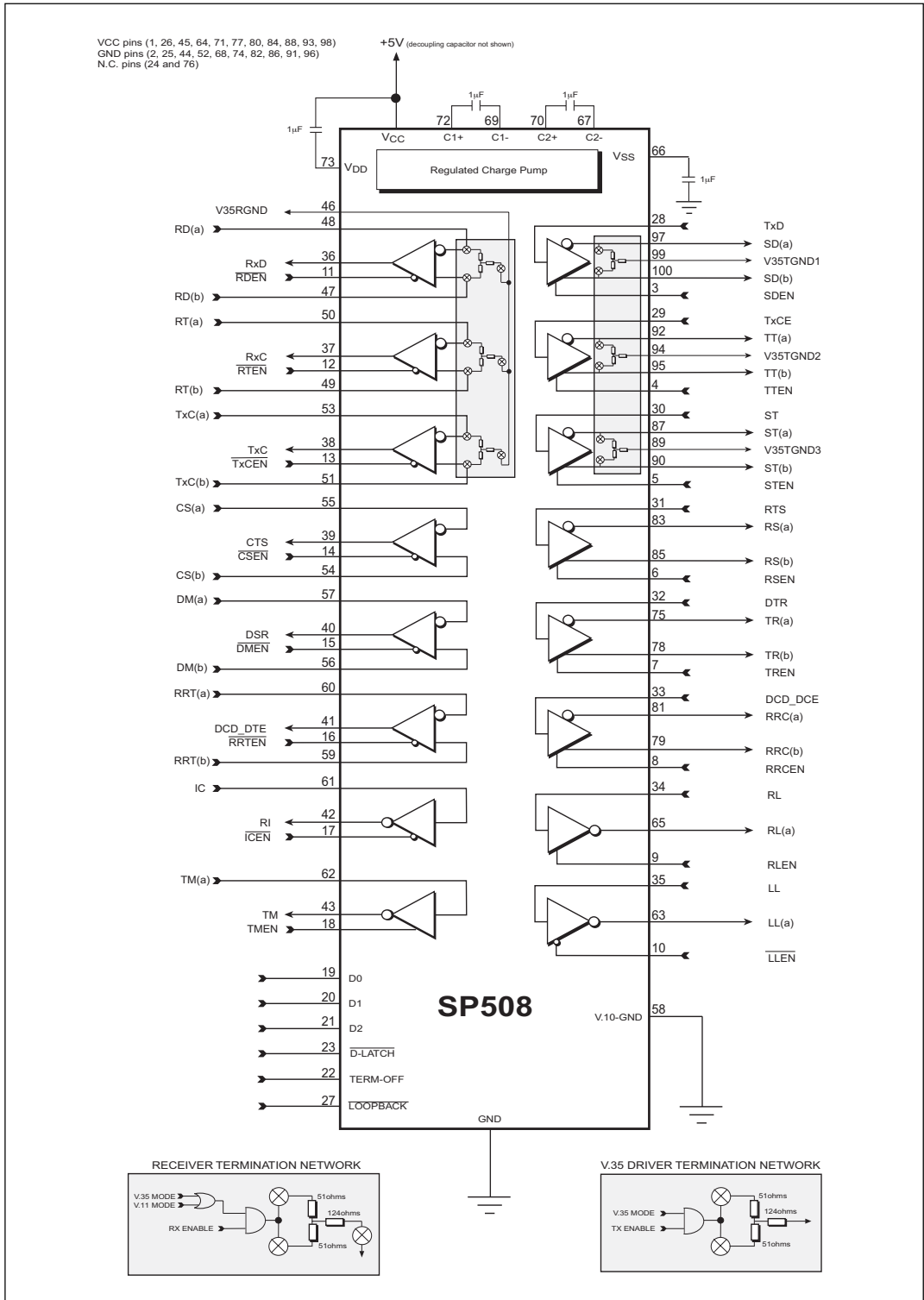


Figure 45. Functional Diagram

FEATURES

The SP508 contains highly integrated serial transceivers that offer programmability between interface modes through software control. The SP508 offers the hardware interface modes for RS-232 (V.28), RS-449/V.36 (V.11 and V.10), EIA-530 (V.11 and V.10), EIA-530A (V.11 and V.10), V.35 (V.35 and V.28) and X.21(V.11). The interface mode selection is done via three control pins, which can be latched via microprocessor control.

The SP508 has eight drivers, eight receivers, and Sipex's patented on-board charge pump (5,306,954) that is ideally suited for wide area network connectivity and other multi-protocol applications. Other features include digital and line loopback modes, individual enable/disable control lines for each driver and receiver, fail-safe when inputs are either open or shorted, individual termination resistor ground paths, separate driver and receiver ground outputs, enhanced ESD protection on driver outputs and receiver inputs.

THEORY OF OPERATION

The SP508 device is made up of 1) the drivers, 2) the receivers, 3) a charge pump, 4) DTE/DCE switching algorithm, and 5) control logic.

Drivers

The SP508 has eight enhanced independent drivers. Control for the mode selection is done via a three-bit control word into D0, D1, and D2. The drivers are prearranged such that for each mode of operation, the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the required signal levels. The mode of each driver in the different interface modes that can be selected is shown in *Table 1*.

There are four basic types of driver circuits – ITU-T-V.28 (RS-232), ITU-T-V.10 (RS-423), ITU-T-V.11 (RS-422), and CCITT-V.35.

The V.28 (RS-232) drivers output single-ended signals with a minimum of $\pm 5V$ (with $3k\Omega$ & $2500pF$ loading), and can operate over 120kbps. Since the SP508 uses a charge pump to generate the RS-232 output rails, the driver outputs will never exceed $\pm 10V$. The V.28 driver architecture is similar to Sipex's standard line of RS-232 transceivers.

The RS-423 (V.10) drivers are also single-ended signals which produce open circuit V_{OL} and V_{OH} measurements of $\pm 4.0V$ to $\pm 6.0V$. When terminated with a 450Ω load to ground, the driver output will not deviate more than 10% of the open circuit value. This is in compliance of the ITU V.10 specification. The V.10 (RS-423) drivers are used in RS-449/V.36, EIA-530, and EIA-530A modes as Category II signals from each of their corresponding specifications. The V.10 drivers are guaranteed to transmit over 120kbps, but can operate at over 1Mbps if necessary.

The third type of drivers are V.11 (RS-422) differential drivers. Due to the nature of differential signaling, the drivers are more immune to noise as opposed to single-ended transmission methods. The advantage is evident over high speeds and long transmission lines. The strength of the driver outputs can produce differential signals that can maintain $\pm 2V$ differential output levels with a load of 100Ω . The signal levels and drive capability of these drivers allow the drivers to also support RS-485 requirements of $\pm 1.5V$ differential output levels with a 54Ω load. The strength allows the SP508 differential driver to drive over long cable lengths with minimal signal degradation. The V.11 drivers are used in RS-449, EIA-530, EIA-530A and V.36 modes as Category I signals which are used for clock and data. Sipex's new driver design over its predecessors allow the SP508 to operate over 20Mbps for differential transmission.

The fourth type of drivers are V.35 differential drivers. There are only three available on the SP508 for data and clock (TxD, TxCE, and TxC in DCE mode). These drivers are current sources that drive loop current through a differential pair resulting in a 550mV differential voltage at the receiver. These drivers also incorporate fixed termination networks for each driver in order to set the V_{OH} and V_{OL} depending on load conditions. This termination network is basically a “Y” configuration consisting of two 51 Ω resistors connected in series and a 124 Ω resistor connected between the two 50 Ω resistors and a V35TGND output. Each of the three drivers and its associated termination will have its own V35TGND output for grounding convenience. Filtering can be done on these pins to reduce common mode noise transmitted over the transmission line by connecting a capacitor to ground.

The drivers also have separate enable pins which simplifies half-duplex configurations for some applications, especially programmable DTE/DCE. The enable pins will either enable or disable the output of the drivers according to the appropriate active logic illustrated on *Figure 45*. The enable pins have internal pull-up and pull-down devices, depending on the active polarity of the receiver, that enable the driver upon power-on if the enable lines are left floating. During disabled conditions, the driver outputs will be at a high impedance 3-state.

The driver inputs are both TTL or CMOS compatible. All driver inputs have an internal pull-up resistor so that the output will be at a defined state at logic LOW (“0”). Unused driver inputs can be left floating. The internal pull-up resistor value is approximately 500k Ω .

Receivers

The SP508 has eight enhanced independent receivers. Control for the mode selection is done via a three-bit control word that is the same as the driver control word. Therefore, the modes for the drivers and receivers are identical in the application.

Like the drivers, the receivers are prearranged for the specific requirements of the synchronous serial interface. As the operating mode of the receivers is changed, the electrical characteristics will change to support the required serial interface

protocols of the receivers. *Table 2* shows the mode of each receiver in the different interface modes that can be selected. There are two basic types of receiver circuits—ITU-T-V.28 (RS-232) and ITU-T-V.11, (RS-422).

The RS-232 (V.28) receiver is single-ended and accepts RS-232 signals from the RS-232 driver. The RS-232 receiver has an operating input voltage range of $\pm 15V$ and can receive signals down to $\pm 3V$. The input sensitivity complies with RS-232 and V.28 at $\pm 3V$. The input impedance is 3k Ω to 7k Ω in accordance to RS-232 and V.28. The receiver output produces a TTL/CMOS signal with a +2.4V minimum for a logic “1” and a +0.4V maximum for a logic “0”. The RS-232 (V.28) protocol uses these receivers for all data, clock and control signals. They are also used in V.35 mode for control line signals: CTS, DSR, LL, and RL. The RS-232 receivers can operate over 120kbps.

The second type of receiver is a differential type that can be configured internally to support ITU-T-V.10 and CCITT-V.35 depending on its input conditions. This receiver has a typical input impedance of 10k Ω and a differential threshold of less than $\pm 200mV$, which complies with the ITU-T-V.11 (RS-422) specifications. V.11 receivers are used in RS-449/V.36, EIA-530, EIA-530A and X.21 as Category I signals for receiving clock, data, and some control line signals not covered by Category II V.10 circuits. The differential V.11 transceiver has improved architecture that allows over 20Mbps transmission rates.

Receivers dedicated for data and clock (RxD, RxC, TxC) incorporate internal termination for V.11. The termination resistor is typically 120 Ω connected between the A and B inputs. The termination is essential for minimizing crosstalk and signal reflection over the transmission line. The minimum value is guaranteed to exceed 100 Ω , thus complying with the V.11 and RS-422 specifications. This resistor is invoked when the receiver is operating as a V.11 receiver, in modes EIA-530, EIA-530A, RS-449/V.36, and X.21.

The same receivers also incorporate a termination network internally for V.35 applications. For V.35, the receiver input termination is a “Y” termination consisting of two 51Ω resistors connected in series and a 124Ω resistor connected between the two 50Ω resistors and V35RGND output. The V35RGND is usually grounded. The receiver itself is identical to the V.11 receiver.

The differential receivers can be configured to be ITU-T-V.10 single-ended receivers by internally connecting the non-inverting input to ground. This is internally done by default from the decoder. The non-inverting input is rerouted to V10GND and can be grounded separately. The ITU-T-V.10 receivers can operate over 1Mbps and are used in RS-449/V.36, E1A-530, E1A-530A and X.21 modes as Category II signals as indicated by their corresponding specifications. All receivers include an enable/disable line for disabling the receiver output allowing convenient half-duplex configurations. The enable pins will either enable or disable the output of the receivers according to the appropriate active logic illustrated on *Figure 45*. The receiver’s enable lines include an internal pull-up or pull-down device, depending on the active polarity of the receiver, that enables the receiver upon power up if the enable lines are left floating. During disabled conditions, the receiver outputs will be at a high impedance state. If the receiver is disabled any associated termination is also disconnected from the inputs.

All receivers include a fail-safe feature that outputs a logic high when the receiver inputs are open, terminated but open, or shorted together. For single-ended V.28 and V.10 receivers, there are internal 5kΩ pull-down resistors on the inputs which produces a logic high (“1”) at the receiver outputs. The differential receivers have a proprietary circuit that detect open or shorted inputs and if so, will produce a logic HIGH (“1”) at the receiver output.

CHARGE PUMP

The charge pump is a **Sipex**-patented design (5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses four-phase voltage shifting technique to attain symmetrical power supplies. The charge pump V_{DD} and V_{SS} outputs are regulated to +5.8V and -5.8V, respectively. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage —During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC} . C_1+ is then switched to ground and the charge in C_1- is transferred to C_2- . Since C_2+ is connected to V_{CC} , the voltage potential across capacitor C_2 is now $2 \times V_{CC}$.

Phase 2

— V_{SS} transfer —Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the negative generated voltage to C_3 . This generated voltage is regulated to -5.8V. Simultaneously, the positive side of the capacitor C_1 is switched to V_{CC} and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage —The third phase of the clock is identical to the first phase—the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1 which is applied to the negative side of the capacitor C_2 . Since C_2+ is at V_{CC} , the voltage potential across C_2 is $2 \times V_{CC}$.

Phase 4

— V_{DD} transfer —The fourth phase of the clock connects the negative terminal of C_2 to ground, and transfers the generated 5.8V across C_2 to C_4 , the V_{DD} storage capacitor. This voltage is regulated to +5.8V. At the regulated voltage, the internal oscillator is disabled and simultaneously with this, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to ground, and the cycle begins again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC} ; in a no-load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 250kHz. The external capacitors can be as low as 1 μ F with a 16V breakdown voltage rating.

TERM_OFF FUNCTION

The SP508 contains a TERM_OFF pin that disables all three receiver input termination networks regardless of mode. This allows the device to be used in monitor mode applications typically found in networking test equipment. The TERM_OFF pin internally contains a pull-down device with an impedance of over 500k Ω , which will default in a “ON” condition during power-up if V.35 receivers are used. The individual receiver enable line and the SHUTDOWN mode from the decoder will disable the termination regardless of TERM_OFF.

LOOPBACK FUNCTION

The SP508 contains a LOOPBACK pin that invokes a loopback path. This loopback path is illustrated in *Figure 46*. LOOPBACK has an internal pull-up resistor that defaults to normal mode during power up or if the pin is left floating. During loopback, the driver output and receiver input characteristics will still adhere to its appropriate specifications.

DECODER AND D_LATCH FUNCTION

The SP508 contains a \bar{D} _LATCH pin that latches the data into the D0, D1, and D2 decoder inputs. If tied to a logic LOW (“0”), the latch is transparent, allowing the data at the decoder inputs to propagate through and program the SP508 accordingly. If tied to a logic HIGH (“1”), the latch locks out the data and prevents the mode from changing until this pin is brought to a logic LOW.

There are internal pull-up devices on D0, D1, and D2, which allow the device to be in SHUTDOWN mode (“111”) upon power up. However, if the device is powered -up with the D_LATCH at a logic HIGH, the decoder state of the SP508 will be undefined.

ESD TOLERANCE

The SP508 device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electrostatic discharges and associated transients.

CTR1/CTR2 EUROPEAN COMPLIANCY

As with all of Sipex’s previous multi-protocol serial transceiver IC’s the drivers and receivers have been designed to meet all the requirements to NET1/NET2 and TBR2 in order to meet CTR1/CTR2 compliancy. The SP508 is also tested in-house at Sipex and adheres to all the NET1/2 physical layer testing and the ITU Series V specifications before shipment. Please note that although the SP508, as with its predecessors, adhere to CTR1/CTR2 compliancy testing, any complex or unusual configuration should be double-checked to ensure CTR1/CTR2 compliance. Consult the factory for details.

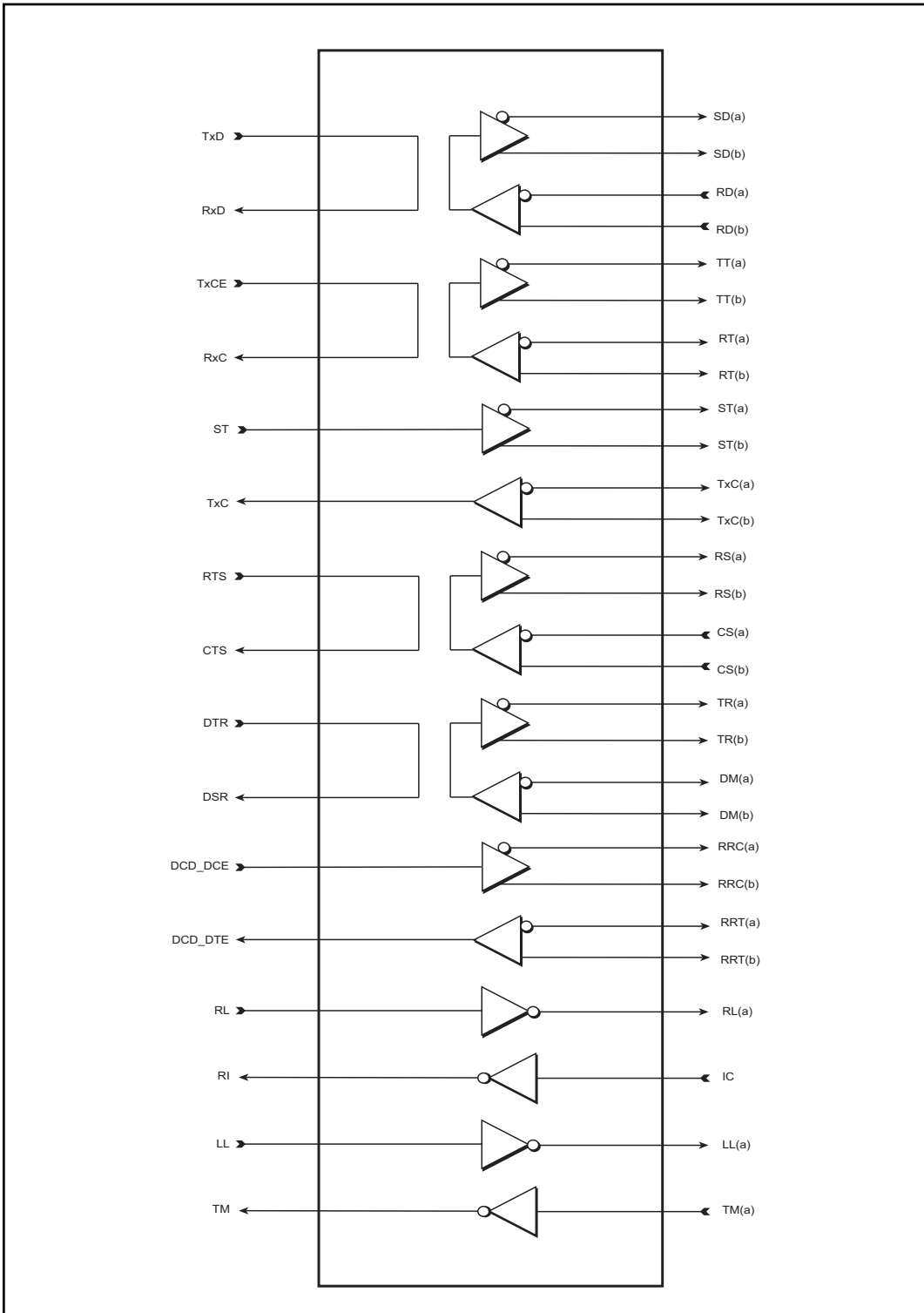
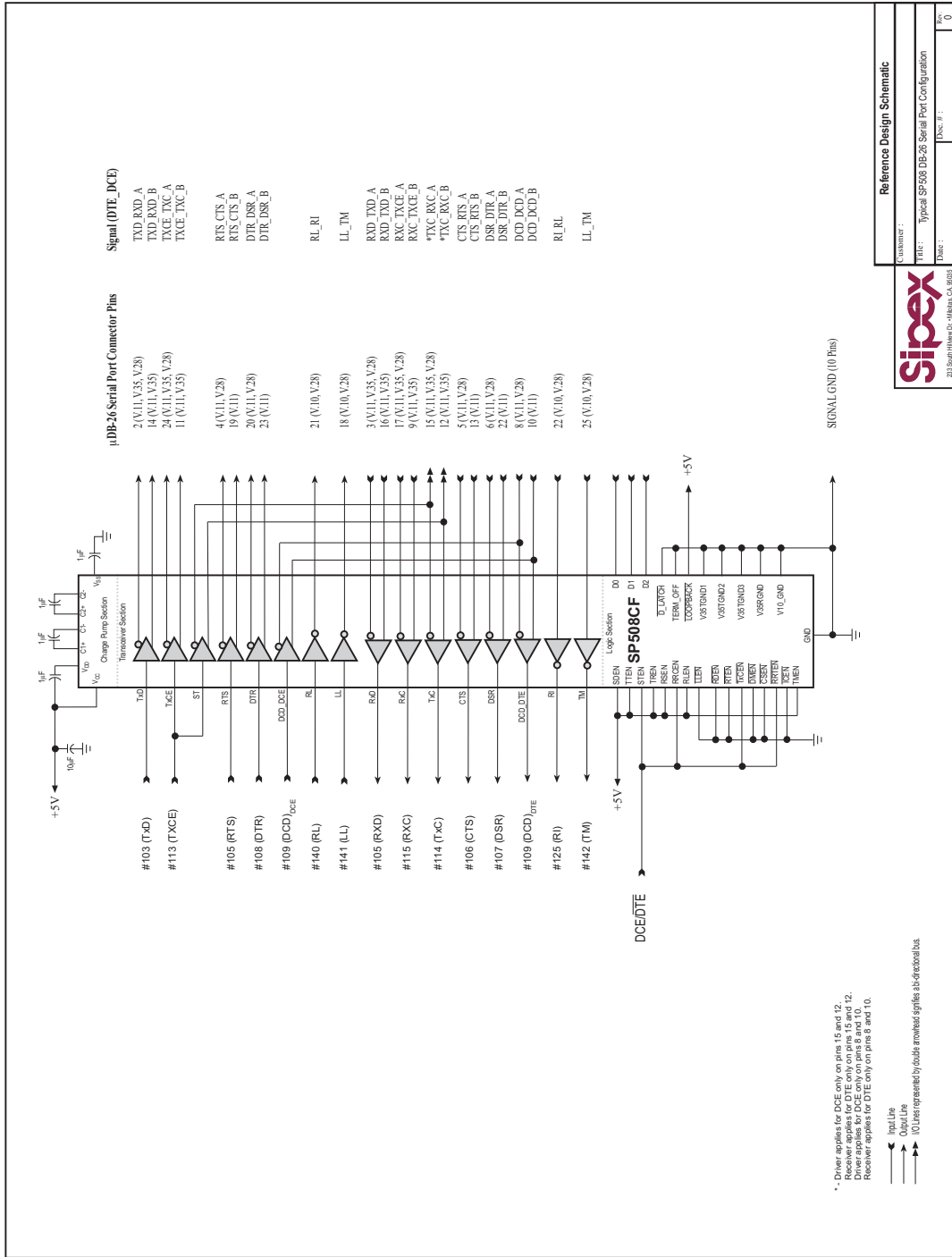


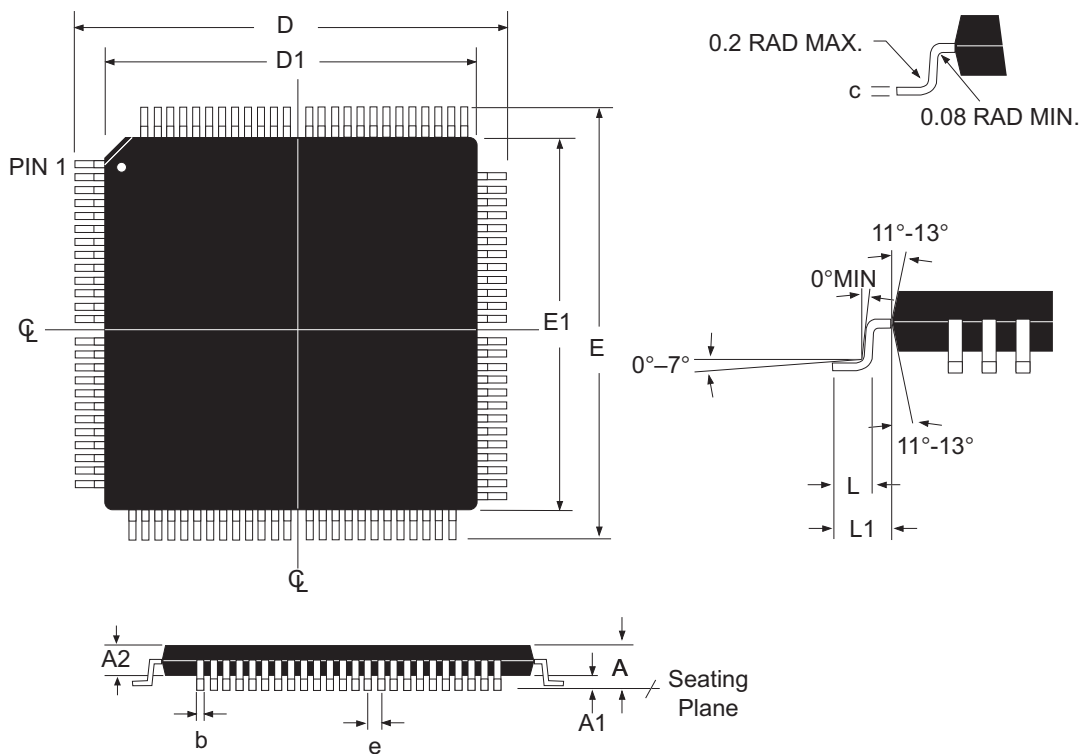
Figure 46. SP508 Loopback Path



Sipex
231 Southline Dr., Milpitas, CA 95031

Customer: **Reference Design Schematic**
Title: **Typical SP508 DB-26 Serial Port Configuration**
Doc #: **0**

Figure 47. SP508 Typical Operating Configuration to Serial Port Connector with DCE/DTE programmability



DIMENSIONS Minimum/Maximum (mm)	100-PIN LQFP JEDEC MS-026 (BED) Variation		
	MIN	NOM	MAX
SYMBOL			
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
N	100		

COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
c	0.09		0.20
L	0.45	0.60	0.75
L1	1.00 REF		

100 PIN LQFP

DCE CONFIGURATION

SP508 Multiprotocol Configured as DCE

Pin Number	Interface to System Logic Pin Mnemonic	Circuit	Interface to Port-Connector	
			Pin Mnemonic	Pin Number
28	TxD	Driver_1	SD(A)	97
3	SDEN	Driver_2	TT(A)	100
29	TxGE	Driver_3	TT(B)	92
4	TTEN	Driver_4	ST(A)	96
30	ST	Driver_5	RS(A)	87
5	STEN	Driver_6	RS(B)	90
31	RTS	Driver_7	TR(A)	83
6	RSEN	Driver_8	TR(B)	85
32	DTR	Driver_9	RRC(A)	75
7	TREN	Driver_10	RRC(B)	78
33	DGD_DCE	Driver_11	RL(A)	81
8	RRCEN	Driver_12	LL(A)	79
34	RL	Driver_13		65
9	RLEN	Driver_14		
35	LL	Driver_15		63
10	LLEN#	Receiver_1		
36	RxD	Receiver_2	RD(A)	48
11	RDEN#	Receiver_3	RD(B)	47
37	RxC	Receiver_4	RT(A)	50
12	RTEN#	Receiver_5	RT(B)	49
38	TxC	Receiver_6	TxC(A)	53
13	TxCEN#	Receiver_7	TxC(B)	51
39	CTS	Receiver_8	CS(A)	55
14	CSEN#	Receiver_9	CS(B)	54
40	DSR	Receiver_10	DM(A)	57
15	DMEN#	Receiver_11	DM(B)	56
41	DGD_DTE	Receiver_12	RRT(A)	60
16	RRTEN#	Receiver_13	RRT(B)	59
42	RI	Receiver_14	IC	61
17	ICEN#	Receiver_15		
43	TM	Receiver_16	TM(A)	62
18	TMEN	Receiver_17		

Spare drivers and receivers may be used for optional signals (Signal Quality, Rate Detect, Standby) or may be disabled using individual enable pins for each driver and receiver.

Recommended Signals and Port Pin Assignments

RS-232 or V.24			EIA-530			RS-449			V.35			X.21		
Signal Type	Mnemonic	Pin(F)	Signal Type	Mnemonic	Pin(F)	Signal Type	Mnemonic	Pin(F)	Signal Type	Mnemonic	Pin(F)	Signal Type	Mnemonic	Pin(F)
V.28	BB	3	V.11	BB(A)	3	V.11	RD(A)	6	V.35	R	4	V.11	R(A)	4
V.28	DD	17	V.11	DD(A)	16	V.11	RD(B)	24	V.35	T	11	V.11	R(B)	11
V.28	DD	17	V.11	DD(B)	17	V.11	RT(A)	8	V.35	T	11	V.11	R(B)	11
V.28	DB	15	V.11	DD(A)	17	V.11	RT(B)	8	V.35	V	115	V.11	B(A)	7**
V.28	DB	15	V.11	DD(B)	9	V.11	RT(A)	26	V.35	X	115	V.11	B(A)	7**
V.28	CB	5	V.11	DB(A)	15	V.11	ST(A)	5	V.35	Y	114	V.11	S(A)	6
V.28	CB	5	V.11	DB(B)	12	V.11	ST(B)	23	V.35	Y	114	V.11	S(A)	6
V.28	CC	6	V.11	CB(A)	5	V.11	CS(A)	9	V.28	AA	114	V.11	S(B)	13
V.28	CC	6	V.11	CB(B)	13	V.11	CS(B)	27	V.28	D	106	V.11	I(A)	5
V.28	CF	8	V.11	CC(A)	6	V.11	DM(A)	11	V.28	E	107	V.11	I(B)	12
V.28	CF	8	V.11	CC(B)	22	V.11	DM(B)	29						
V.28	CE	22	V.11	CF(A)	8	V.11	RR(A)	13	V.28	F	109			
V.28	CE	22	V.11	CF(B)	10	V.11	RR(B)	31	V.28	J	125			
V.28	TM	25	V.10	TM	25	V.10	TM	18	V.28	NN	142			
V.28	BA	2	V.11	BA(A)	2	V.11	SD(A)	4	V.35	P	103	V.11	T(A)	2
V.28	DA	24	V.11	BA(B)	12	V.11	SD(B)	22	V.35	S	103	V.11	T(B)	9
V.28	DA	24	V.11	DA(A)	24	V.11	TT(A)	17	V.35	U	113	V.11	X(A)	7**
V.28	DA	24	V.11	DA(B)	11	V.11	TT(B)	35	V.35	W	113	V.11	X(B)	14**
V.28	CA	4	V.11	CA(A)	4	V.11	RS(A)	7	V.28	C	105	V.11	C(A)	3
V.28	CD	20	V.11	CA(B)	19	V.11	RS(B)	25	V.28	H	108	V.11	C(B)	10
V.28	RL	21	V.10	CD(A)	20	V.11	TR(A)	12						
V.28	LL	18	V.10	CD(B)	23	V.11	TR(B)	30						
V.28	RL	21	V.10	RL	21	V.10	RL	14	V.28	N	140			
V.28	LL	18	V.10	LL	18	V.10	LL	10	V.28	L	141			

Pin assignments and signal functions are subject to national or regional variation and proprietary / non-standard implementations

** X.21 use either B() or X(), not both

DTE CONFIGURATION

SP508 Multiprotocol Configured as DTE

Interface to System Logic		Interface to Port-Connector	
Pin Number	Pin Mnemonic	Circuit	Pin Mnemonic
28	TxD	Driver_1	SD(A)
3	SDEN	Driver_2	SD(B)
29	TxC	Driver_3	TT(A)
4	TLEN	Driver_4	TT(B)
30	ST	Driver_5	ST(A)
5	STEN	Driver_6	ST(B)
31	RIS	Driver_7	RS(A)
6	RSEN	Driver_8	RS(B)
32	DTR	Driver_9	TR(A)
7	TREN	Driver_10	TR(B)
33	DCD DCE	Driver_11	RRC(A)
8	RRGEN	Driver_12	RRC(B)
34	RL	Driver_13	RL(A)
9	RLEN	Driver_14	RL(B)
35	LL	Driver_15	LL(A)
10	LLEN#	Driver_16	LL(B)
36	RxD	Receiver_1	RD(A)
11	RDEEN#	Receiver_2	RD(B)
37	RxC	Receiver_3	RT(A)
12	RTEN#	Receiver_4	RT(B)
38	TxC	Receiver_5	TxC(A)
13	TxCEN#	Receiver_6	TxC(B)
39	CTS	Receiver_7	CS(A)
14	CSEN#	Receiver_8	CS(B)
40	DSR	Receiver_9	DM(A)
15	DMEN#	Receiver_10	DM(B)
41	DCD DTE	Receiver_11	RRT(A)
16	RRTEN#	Receiver_12	RRT(B)
42	RI	Receiver_13	IC
17	ICEN#	Receiver_14	IC
43	TM	Receiver_15	TM(A)
18	TMEN	Receiver_16	TM(B)

Spare drivers and receivers may be used for optional signals (Signal Quality, Rate Detect, Standby) or may be disabled using individual enable pins for each driver and receiver

Recommended Signals and Port Pin Assignments

RS-232 or V.24		EIA-530		RS-449		V.35		X.21		AppleTalk™	
Signal Type	Mnemonic	Pin(M)	Mnemonic	Pin(M)	Mnemonic	Pin(M)	Mnemonic	Pin(M)	Mnemonic	Pin(M)	Mnemonic
V.28	BA	2	V.11 BA(A)	4	SD(A)	4	V.35 103 P	2	V.11 T(A)	2	V.11 TxD -
V.28	DA	24	V.11 DA(A)	14	SD(B)	22	V.35 103 S	9	V.11 T(B)	9	V.11 TxD +
			V.11 DA(B)	24	TT(A)	17	V.35 113 U	7**	V.11 X(A)	7**	
			V.11 DA(B)	11	TT(B)	35	V.35 113 W	14**	V.11 X(B)	14**	
V.28	CA	4	V.11 CA(A)	4	RS(A)	7	V.28 105 C	3	V.11 C(A)	3	
			V.11 CA(B)	19	RS(B)	25		10	V.11 C(B)	10	
V.28	CD	20	V.11/10 CD(A)	20	TR(A)	12	V.28 108 H				HSK0
			V.11/10 CD(B)	23	TR(B)	30					1
V.28	RL	21	V.10 RL	21	RL	14	V.28 140 N				
V.28	LL	18	V.10 LL	18	LL	10	V.28 141 L				
V.28	BB	3	V.11 BB(A)	3	RD(A)	6	V.35 104 R	4	V.11 R(A)	4	RxD-
			V.11 BB(B)	16	RD(B)	24	V.35 104 T	11	V.11 R(B)	11	RxD+
V.28	DD	17	V.11 DD(A)	17	RT(A)	8	V.35 115 V				
			V.11 DD(B)	9	RT(B)	26	V.35 115 X				
V.28	DB	15	V.11 DB(A)	15	ST(A)	5	V.35 114 Y	6	V.11 S(A)	6	
			V.11 DB(B)	12	ST(B)	23	V.35 114 AA	13	V.11 S(B)	13	
V.28	CB	5	V.11 CB(A)	5	CS(A)	9	V.28 106 D	5	V.11 I(A)	5	GND
			V.11 CB(B)	13	CS(B)	27		12	V.11 I(B)	12	HSK1
V.28	CC	6	V.11/10 CC(A)	6	DM(A)	11	V.28 107 E	7**	V.11 B(A)	7**	GPI
			V.11/10 CC(B)	22‡	DM(B)	29		14**	V.11 B(B)	14**	
V.28	CF	8	V.11 CF(A)	8	RR(A)	13	V.28 109 F				
			V.11 CF(B)	10	RR(B)	31					
V.28	CE	22	V.10 RI	22‡			V.28 125 J				
V.28	TM	25	V.10 TM	25	TM	18	V.28 142 NN				

Pin assignments and signal functions are subject to national or regional variation and proprietary / non-standard implementations
 † EIA-530 uses V.11 (differential) for DSR (CC) and DTR (CD) signals; EIA-530-A uses single-ended V.10 for DSR and DTR and adds RI signal on pin 22
 ** X.21 use either B() or X(), not both

ORDERING INFORMATION

Part Number	Top Mark	Temperature Range	Package Types
SP508CF	SP508CFYYWW.....	0°C to +70°C	100 Lead LQFP
SP508EF	SP508EFYYWW.....	-40°C to +85°C	100 Lead LQFP

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP508EF = standard; SP508EF-L = lead free

REVISION HISTORY

DATE	REVISION	DESCRIPTION
3/31/04	A	Implemented tracking revision.
5/6/04	B	Added Top Mark to ordering information.
6/3/04	C	Added Tables to page 28 and 29.
8/19/04	D	Corrected pin description table and figure 49. Updated DCE/DTE tables.
1/19/05	E	Corrected reference to figure 46.



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