

**S1D13742 Mobile Graphics Engine**

# **Interfacing the Sharp LQ043xxx 480x272 TFT Panel**

## NOTICE

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# Chapter 1 Interfacing the Sharp LQ043xxx 480x272 TFT Panel

This document describes the hardware and software environment required to interface the S1D13742 Mobile Graphics Engine and Sharp LQ043xxx 480x272 TFT Panel.

The designs described in this document are presented only as examples of how such interfaces might be implemented.

## 1.1 Overview

The S1D13742 directly supports the Sharp LQ043xxx and requires no additional hardware and minimal programming. The S1D13742 register settings and electrical interface is described below.

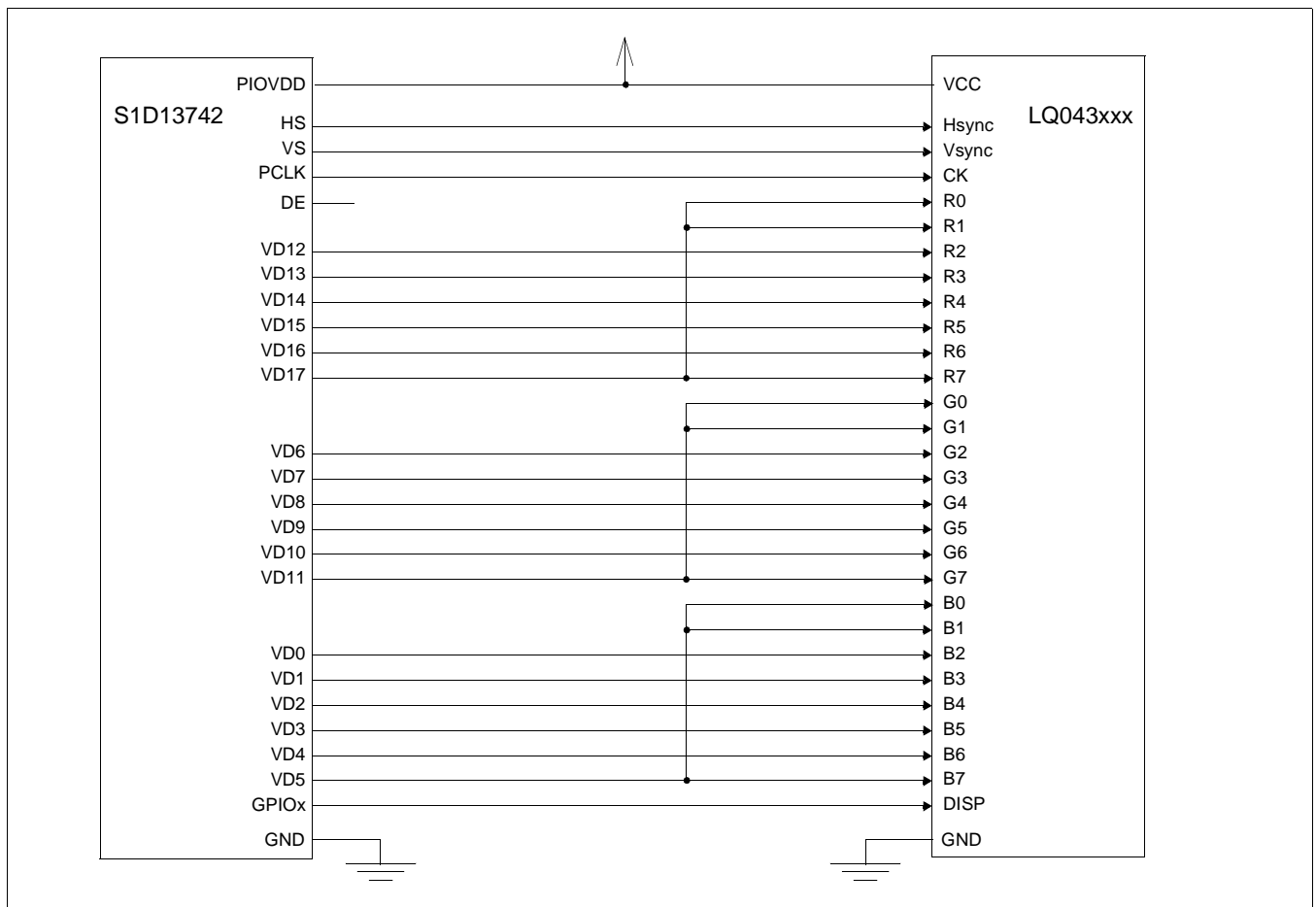


Figure 1-1: S2D13742 to Sharp LQ043xxx Connection Diagram

### 1.1.1 Electrical Interface

*Table 1-1: Pin Mapping*

<b>S1D13742 Pin Name</b>	<b>LQ043xxx Pin Name</b>
HS	Hsync
VS	Vsync
PCLK	CK
DE	-
VD17	R0
VD17	R1
VD12	R2
VD13	R3
VD14	R4
VD15	R5
VD16	R6
VD17	R7
VD11	G0
VD11	G1
VD6	G2
VD7	G3
VD8	G4
VD9	G5
VD10	G6
VD11	G7
VD5	B0
VD5	B1
VD0	B2
VD1	B3
VD2	B4
VD3	B5
VD4	B6
VD5	B7
GPIOx (any of GPIO[7:0] pins)	DISP

The same power must be connected to PIOVDD pins of S1D13742 and to VCC pins of Sharp LQ043xxx panel.

Display ON/OFF signal is provided by one of S1D13742 GPIO pins and it is under application software control. The Vertical Non-Display Period status bit or TE pin, can be used to comply with the Sharp LQ043xxx requirement that DISP signal does not change while Vsync is low.

### 1.1.2 S1D13742 Register Settings for Sharp LQ043xxx, 480x272 TFT Panel

The registers listed below are only those associated with panel specific timing issues. All other registers are not shown here.

When a window is setup for YUV data, the data must always alternate between odd and even lines, starting with an odd line.

*Table 1-2: Example Register Settings for Sharp LQ043xxx 480x272 TFT Panel*

Register	Value	Comment
All	default	Come out of reset - all registers set to default values
REG[56h]	02h	enter sleep mode (or use PWRSVE pin)
REG[04h]	03h	set PLL M-Divider. CLKI = 4MHz, PLL input clock = CLKI/4 = 1MHz.
REG[06h]	F8h	
REG[08h]	80h	
REG[0Ah]	28h	
REG[0Ch]	00h	
REG[0Eh]	3Eh	LL = 63, resulting SYSCLK = LL x PLL input clock = 63MHz
REG[12h]	31h	set PCLK divide, PCLK = 9MHz set SYSCLK source = PLL
REG[14h]	00h	no panel data swap, 18-bit panel
REG[16h]	3Ch	HDP = 480 pixels
REG[18h]	2Dh	HNDP = 45 pixels
REG[1Ah]	10h	VDP = 272 lines
REG[1Ch]	01h	
REG[1Eh]	0Eh	VNDP = 14 lines
REG[20h]	29h	HS Pulse Width = 41 pixels
REG[22h]	02h	HS Start Position = 2 pixels
REG[24h]	0Ah	VS Width = 10 lines
REG[26h]	02h	VS Start Position (VFP) = 2 line
REG[28h]	00h	PCLK Polarity: data output on rising edge
REG[2Ah]	82h	set memory to 18bpp, data mode to RGB 6:6:6 mode 1
REG[56h]	00h	disable sleep mode
REG[04h] bit 7	—	wait for PLL to lock - poll REG[04h] bit 7
REG[38h]	00h	Window X Start Position = 0
REG[3Ah]	00h	
REG[3Ch]	00h	Window Y Start Position = 0
REG[3Eh]	00h	
REG[40h]	DFh	Window X End Position = 479
REG[42h]	01h	
REG[44h]	0Fh	Window Y End Position = 271
REG[46h]	01h	
REG[48h]	Write the image data to the Memory Data Port, REG[48h] and REG[49h]. The image will immediately begin to appear on the LCD.	
REG[49h]		

The above values are intended as examples. This example assumes that CLKI = 4MHz and that the PLL is used to generate SYSCLK. Actual settings can vary and still remain within the LCD panel timing requirements.

## Chapter 2 Change Record

**X63A-A-001-00 Revision 1.0 - Issued: June 11, 2008**

- all changes from the last revision are highlighted in Red
- initial release



### AMERICA

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**EPSON ELECTRONICS AMERICA, INC.****HEADQUARTERS**

2580 Orchard Parkway  
San Jose, CA 95131, USA  
Phone: +1-800-228-3964      FAX: +1-408-922-0238

**SALES OFFICES****Northeast**

301 Edgewater Place, Suite 210  
Wakefield, MA 01880, U.S.A.  
Phone: +1-800-922-7667      FAX: +1-781-246-5443

### EUROPE

---

**EPSON EUROPE ELECTRONICS GmbH****HEADQUARTERS**

Riesstrasse 15  
80992 Munich, GERMANY  
Phone: +49-89-14005-0      FAX: +49-89-14005-110

### ASIA

---

**EPSON (CHINA) CO., LTD.**

23F, Beijing Silver Tower 2# North RD DongSanHuan  
ChaoYang District, Beijing, CHINA  
Phone: +86-10-6410-6655      FAX: +86-10-6410-7320

**SHANGHAI BRANCH**

7F, High-Tech Bldg., 900, Yishan Road,  
Shanghai 200233, CHINA  
Phone: +86-21-5423-5522      FAX: +86-21-5423-5512

**EPSON HONG KONG LTD.**

20/F., Harbour Centre, 25 Harbour Road  
Wanchai, Hong Kong  
Phone: +852-2585-4600      FAX: +852-2827-4346  
Telex: 65542 EPSCO HX

**EPSON Electronic Technology Development (Shenzhen) LTD.**

12/F, Dawning Mansion, Keji South 12th Road,  
Hi-Tech Park, Shenzhen  
Phone: +86-755-2699-3828      FAX: +86-755-2699-3838

**EPSON TAIWAN TECHNOLOGY & TRADING LTD.**

14F, No. 7, Song Ren Road,  
Taipei 110  
Phone: +886-2-8786-6688      FAX: +886-2-8786-6660

**EPSON SINGAPORE PTE., LTD.**

1 HarbourFront Place,  
#03-02 HarbourFront Tower One, Singapore 098633  
Phone: +65-6586-5500      FAX: +65-6271-3182

**SEIKO EPSON CORPORATION****KOREA OFFICE**

50F, KLI 63 Bldg., 60 Yoido-dong  
Youngdeungpo-Ku, Seoul, 150-763, KOREA  
Phone: +82-2-784-6027      FAX: +82-2-767-3677

**GUMI OFFICE**

2F, Grand B/D, 457-4 Songjeong-dong,  
Gumi-City, KOREA  
Phone: +82-54-454-6027      FAX: +82-54-454-6093

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**SEIKO EPSON CORPORATION****SEMICONDUCTOR OPERATIONS DIVISION****IC Sales Dept.****IC International Sales Group**

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN  
Phone: +81-42-587-5814      FAX: +81-42-587-5117