EV1340QI
4A Synchronous Highly Integrated DC-DC DDR2/3/QDR™ Memory Termination and Low VIN Power SoC

Description

The EV1340 is a Power System on a Chip (PowerSoC) DC to DC converter in a 54 pin QFN that is optimized for DDR2, DDR3, and QDR™ VTT applications. In addition, the EV1340 is an excellent solution for low V_{IN} applications where high efficiency is critical. For VTT applications, the EV1340 requires a power supply (AVIN) for the controller and operates from an input supply (VDDQ) voltage range of 1.0V to 1.8V and provides a tightly regulated and very stable output voltage (VTT) which tracks VDDQ while sinking and sourcing up to 4A of output current.

The EV1340 utilizes innovative circuit techniques, high-density circuit integrations and optimized switching frequency along with Enpirion's proprietary inductor technology to deliver high-quality, ultra compact, non-isolated DC-DC conversion.

The complete power converter solution enhances productivity by offering greatly simplified board design, layout and manufacturing requirements.

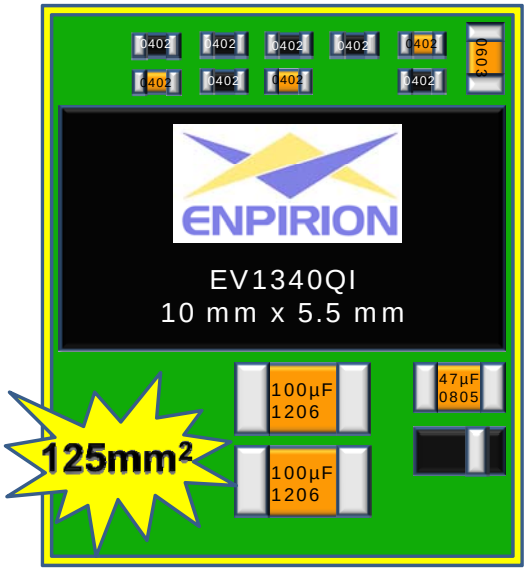


Figure 1: EV1340 Total Solution Size ~ 125mm² (not to scale)

Features

- High efficiency, up to 91%.
- Scaled version of VDDQ applied to VREF
- Output voltage tracks VDDQ +/- 1%.
- Monotonic start-up with pre-bias.
- Programmable soft-start time. Soft shutdown.
- Thermal shutdown, over current, short circuit, and under-voltage protection.
- RoHS compliant, MSL level 3, 260°C reflow.

Application

- Bus Termination: DDR2, DDR3, & QDR™ memory

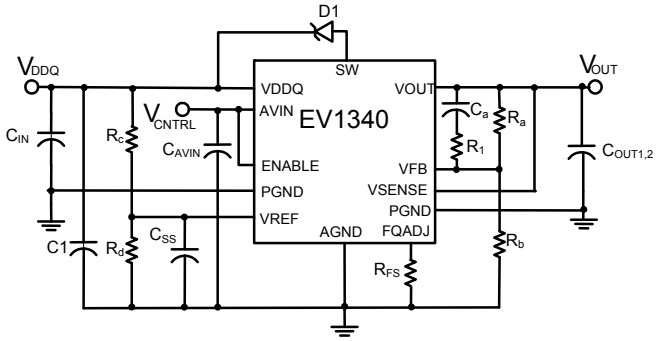


Figure 2: Typical V_{TT} Application Schematic (V_{DDQ} is the memory core voltage; V_{TT} is memory termination voltage that tracks V_{DDQ})

Ordering Information

Part Number	Temp Rating (°C)	Package
EV1340QI	-40 to +85	54-pin QFN T&R
EV1340QI-E	QFN Evaluation Board	

Pin Assignments (Top View)

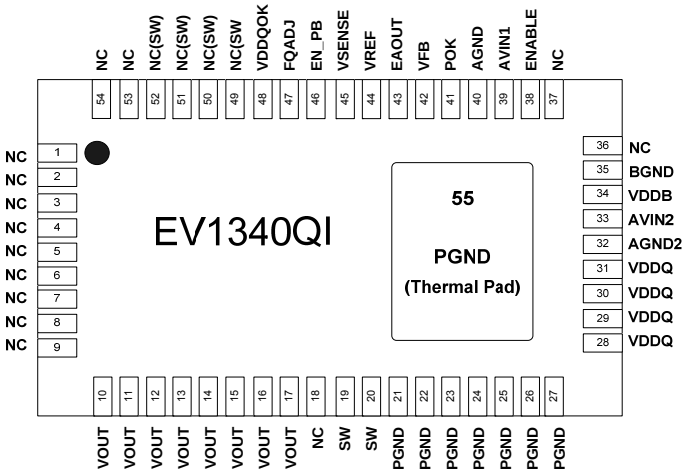


Figure 3: Pin Out Diagram (Top View).
All pins must be soldered to PCB

NOTE: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

Pin Description

PIN	NAME	FUNCTION
1-9, 18, 36, 37, 53, 54	NC	NO CONNECT: These pins must be soldered to PCB but not electrically connected to each other or to any external signal, voltage, or ground. These pins may be connected internally. Failure to follow this guideline may result in device damage.
10 -17	VOUT	Regulated converter output. Decouple with output filter capacitor to PGND. Refer to layout section for specific layout requirements
19, 20,	SW	These pins are internally connected to the common switching node of the internal MOSFETs. The anode of a Schottky diode needs to be connected to these pins. The cathode of the diode needs to be connected to VDDQ.
21-27	PGND	Input and output power ground. Refer to layout section for specific layout requirements.
28-31	VDDQ	In DDR applications the input to this pin is the DDR core voltage. This is the input power supply to the power train which will be divided by two to create an output voltage that tracks with the input voltage applied to this pin. Decouple with input capacitor to PGND. Refer to layout section for specific layout requirements
32	AGND2	Ground for the gate driver supply. Connect to the GND plane with a via next to the pin.
33, 39	AVIN1, AVIN2	Analog input voltage for the controller circuits. Each of these pins needs to be separately connected to the 3.3V input supply. Decouple with a capacitor to AGND.
34	VDDB	Internal regulated voltage used for the internal control circuitry. This pin is reserved for Enpirion testing, and should be left floating.
35	BGND	This pin is reserved for Enpirion testing, and should be left floating.
38	ENABLE	This is the Device Enable pin. Floating this pin or a high level enables the device while a low level disables the device.
40	AGND	This is the quiet ground for the controller. Connect to the GND plane with a via next to the pin.
41	POK	POK is a logical AND of VDDQOK and the internally generated POK of the EV1340. POK is an open drain logic output that requires an external pull-up resistor. POK is logic high when VOUT is within -10% to +10% of VOUT nominal. This pin guarantees a logic low even when the EV1340 is completely un-powered. This pin can sink a maximum 4mA. The pull-up resistor may be connected to a power supply other than AVIN or VDDQ but the voltage should be <3.6Volts.

PIN	NAME	FUNCTION
42	VFB	This is the feedback input pin which is always active. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. (A feed-forward capacitor and a resistor are required across the upper resistor.) The output voltage regulates so as to make the VFB node voltage = 600mV.
43	EAOUT	Optional Error Amplifier Output. Allows for customization of the control loop.
44	VREF	External voltage reference input. A resistor divider connects from VDDQ to AGND. The mid-point of the resistor divider is connected to VREF. The resistor divider has to be chosen to make the voltage applied to this pin 600mV. An optional capacitor (for soft start) may be connected from VREF to AGND.
45	VSENSE	This pin senses the output voltage when the device is in pre-bias (or backfeed) mode. Connect to VOUT if EN_PB is high. Leave this pin floating if EN_PB is pulled to GND.
46	EN_PB	Monotonic start-up with pre-bias is enabled by either pulling this pin high or letting it float. A logical low on this pin will disable pre-bias mode operation.
47	FQADJ	Optimized frequency adjust pin. Connect a 3.57kΩ resistor from this pin to AGND to optimize on switching frequency.
48	VDDQOK	This is an active high input pin that indicates the externally supplied VDDQ input has reached its POK level. This pin should be tied to the VDDQ regulator POK output. It has an internal pull-up, and can be left floating if not needed.
49-52	NC(SW)	No Connect – these pins are internally connected to the common switching node of the internal MOSFETs. They are not to be electrically connected to any external signal, ground, or voltage. Failure to follow these guidelines may result in damage to the device.
55	Thermal Pad (PGND)	Device thermal pad and PGND. Connected to the system ground plane. See Layout Recommendations section.

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage: AVIN1, AVIN2	V_{IN}	-0.5	4.0	V
Voltages on: ENABLE, EN_PB, VDDQOK		-0.5	V_{IN}	V
Voltages on: VFB, VREF, EAOUT, VDDQ, VOUT, VSENSE, FQADJ		-0.5	2.7	V
Voltage on: POK			3.6	V
Voltage on: SW		-0.5	VDDQ+0.5	V
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ Max}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model)			2000	V
ESD Rating (based on CDM)			500	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range: AVIN1, AVIN2		2.9	3.7	V
Input Voltage Range: VDDQ		1.0	1.8	V
Input Voltage Range: VREF	V_{EXTREF}	0.4	0.72	V
EN_PB, VDDQOK, EN		0	AVIN	V
Operating Ambient Temperature	T_A	- 40	+85	°C
Operating Junction Temperature	T_J	- 40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM) (**Note 1**)	θ_{JA}	22	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	2	°C/W
Thermal Shutdown	T_{SD}	150	°C
Thermal Shutdown Hysteresis	T_{SDH}	20	°C

Note 1: Based on a 2 oz. copper board and proper thermal design in line with JEDEC EIJ/JESD 51 Standards.

Electrical Characteristics

NOTE: AVIN1, AVIN2 = 3.3V, over operating temperature range unless otherwise noted. Typical values are at T_A = 25°C.

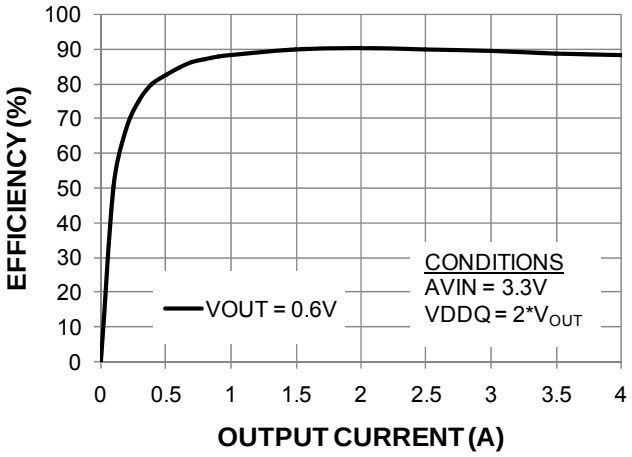
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Power Supply Voltage	VDDQ		1.0		1.8	V
Controller Supply Voltage	AVIN		2.9	3.3	3.7	V
Output Voltage Accuracy – Initial	ΔV_{OUT}	V_{OUT} =1/2 VDDQ (e.g. @ VDDQ = 1.500V), 0.1% input and output resistor dividers)	0.740	0.750	0.760	V
Input Voltage Reference	VREF	With 0.1% resistor values for Rc and Rd. See figure 2.	599	600	601	mV
VFB Pin Voltage	V_{VFB}	2.9V ≤ AVIN ≤ 3.7V, VREF=600mV, 0A ≤ ILOAD ≤ 4A	591	600	609	mV
VFB Pin Input Leakage Current	I_{VFB}	VFB pin input leakage current		20		nA
Shut-Down Supply Current	I_S	Power Supply current with Enable=0		1		mA
Under Voltage Lock-out – AVIN Rising	V_{UVLOR}	Voltage above which UVLO is not asserted		2.3		V
Under Voltage Lock-out – AVIN Falling	V_{UVLOF}	Voltage below which UVLO is asserted		2.1		V
Continuous Output Sourcing Current	$I_{OUT\_Max\_SRC}$	Maximum load current. See Note 1.	0		4	A
Maximum Continuous Output Sinking Current	$I_{OUT\_Max\_SNK}$	Maximum load current. See Note 1.	0		4	A
Over Current Trip Level	I_{OCPH}	Sourcing. VDDQ = 1.35V		14		A
Switching Frequency	F_{SW}	R_{FQADJ} = 3.57kOhms		1.5		MHz
Frequency Adjust Resistor	R_{FQADJ}			3.57		kΩ
Pre-Bias Level	V_{PB}	Allowable pre-bias as a fraction of programmed output voltage for monotonic start up	20		85	%
Non-Monotonicity	V_{PB_NM}	Allowable non-monotonicity under pre-bias start up		50		mV
V_{OUT} Range for P_{OK} = High		Range of output voltage as a fraction of programmed value when P_{OK} is asserted	92		110	%
P_{OK} Deglitch Delay		Falling edge deglitch delay after output crossing 90% level		64		Clock cycles
V_{POK} Logic Low level		With 4mA current sink into P_{OK} pin		0.6		V
V_{POK} Logic high level				AVIN		V
POK Current Sink Capability		2.9V ≤ AVIN ≤ 3.7V		4		mA
VTT Tracking VDDQ	VDDQ – 2*VTT	VDDQ > 400mV, VDDQ Rate of change < 2V/mS	-25		+25	mV
Enable Threshold	V_{ENABLE}	2.9V ≤ AVIN ≤ 3.7 V; Min voltage to ensure the converter is enabled	1.3			V
Disable Threshold	$V_{DISABLE}$	Max voltage to ensure the converter is disabled			0.8	V
Enable Pin Current	I_{EN}	AVIN = 3.6V		50		µA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Binary Pin Logic Low Threshold	V_{B-LOW}	VDDQOK			0.8	V
Binary Pin Logic High Threshold	V_{B-HIGH}	VDDQOK	1.8			V

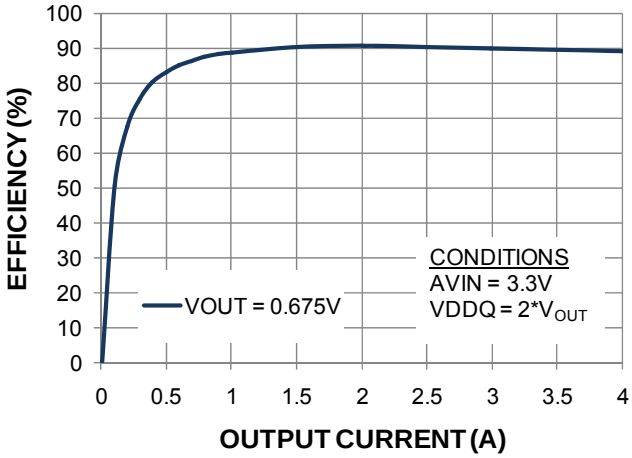
Note 1: Maximum output current may need to be de-rated, based on operating condition, to meet TJ requirements.

Typical Performance Curves

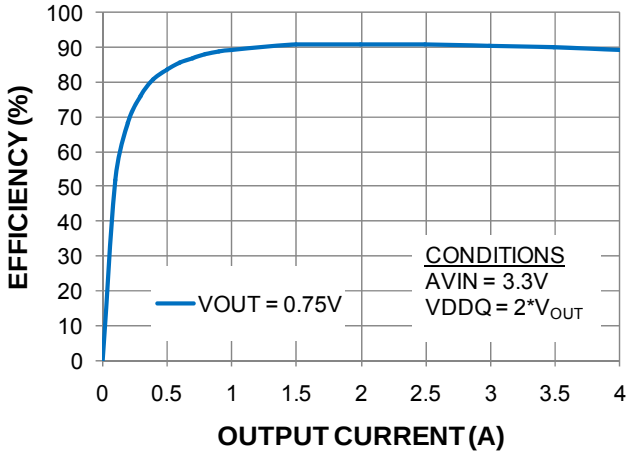
Efficiency vs. Output Current



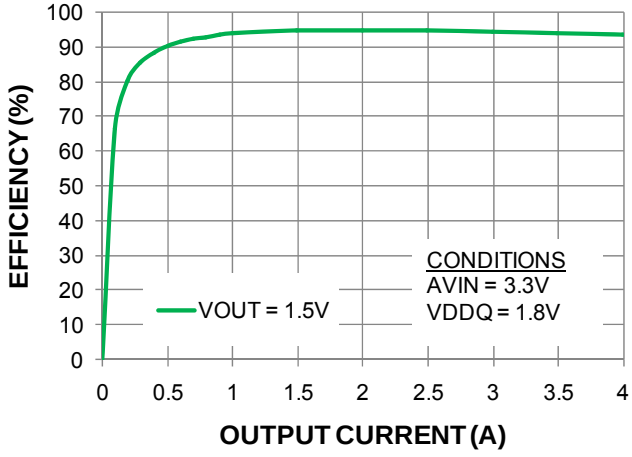
Efficiency vs. Output Current



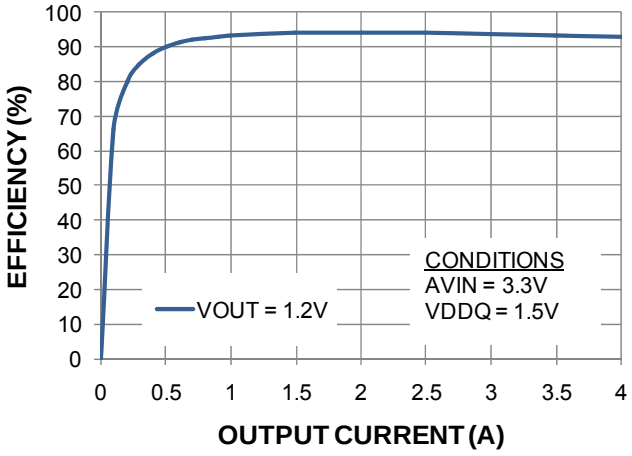
Efficiency vs. Output Current



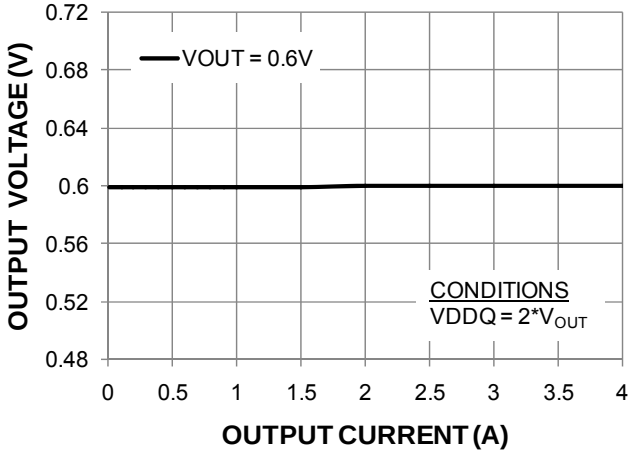
Efficiency vs. Output Current



Efficiency vs. Output Current



V_{OUT} vs. I_{OUT}



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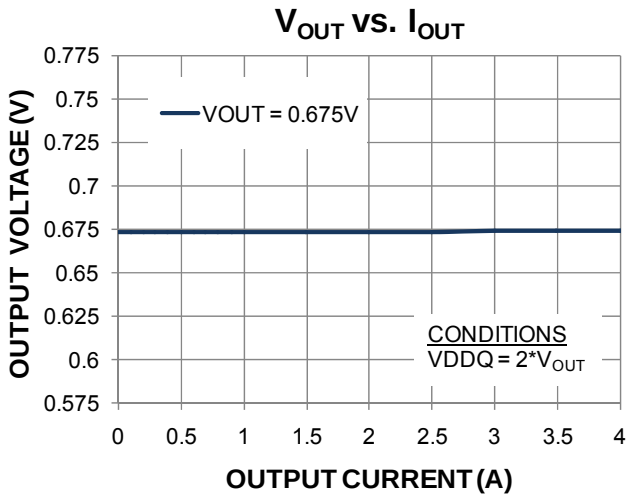
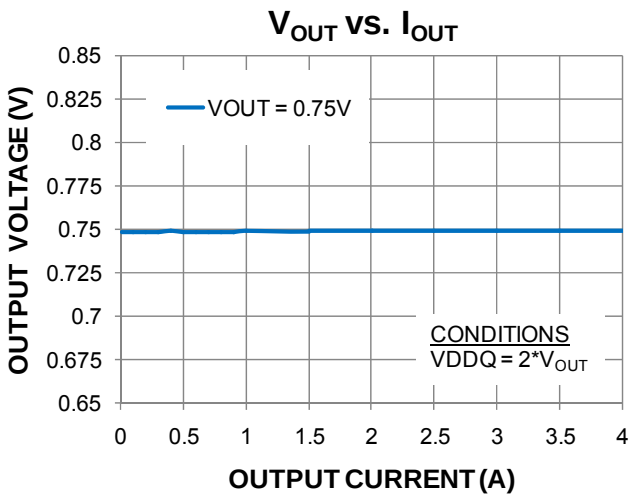
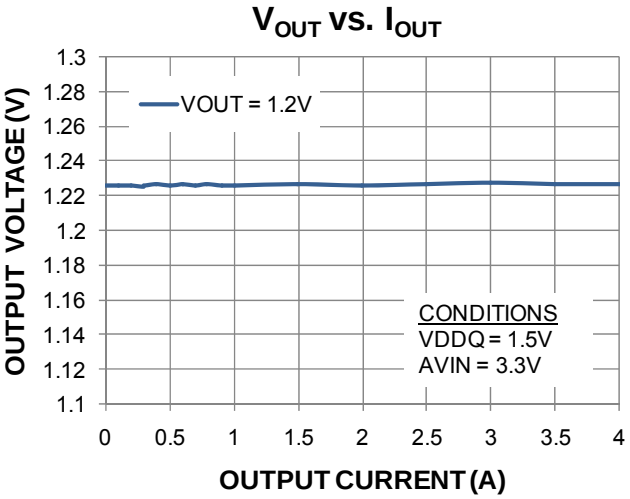
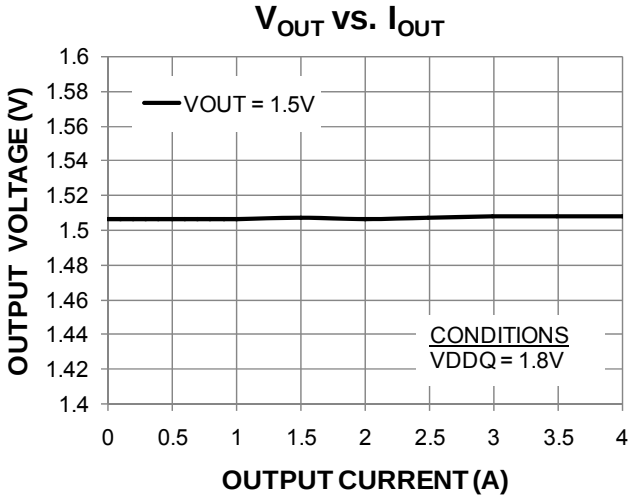
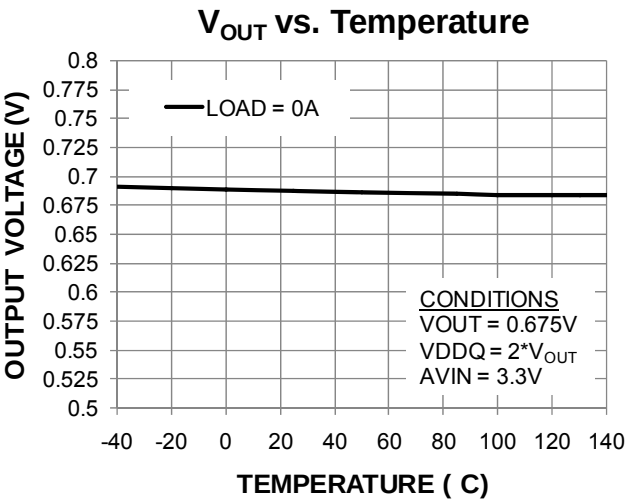
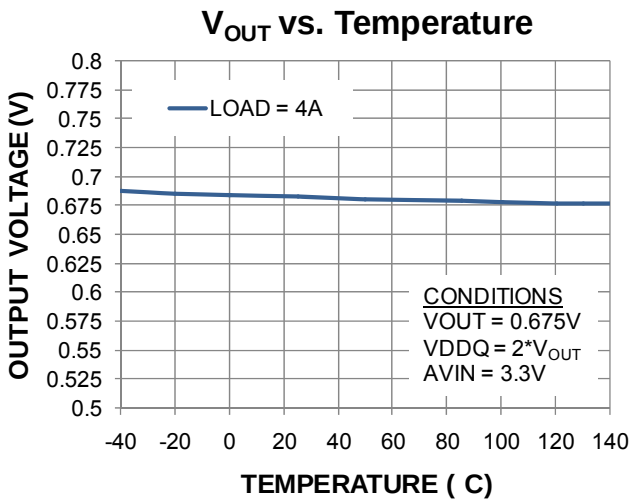






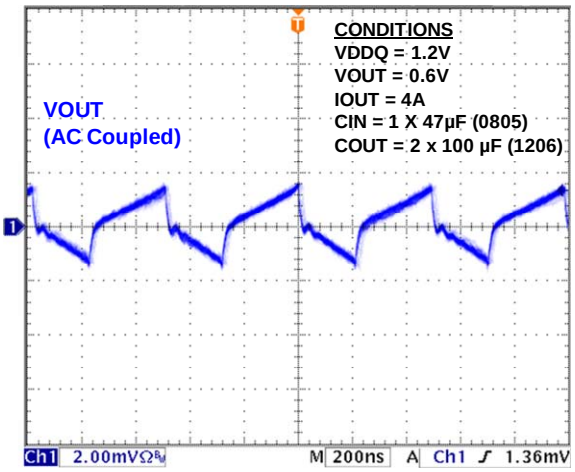




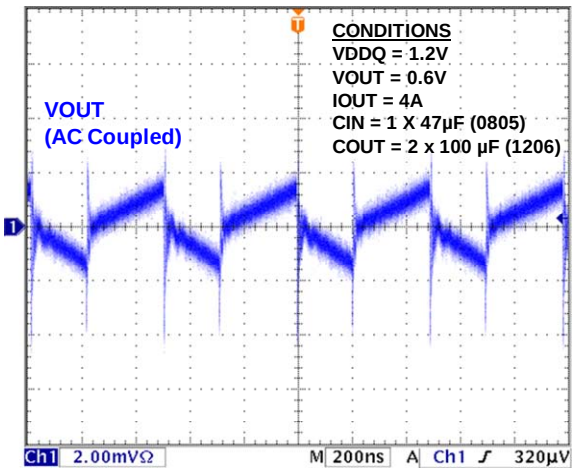


Typical Performance Characteristics

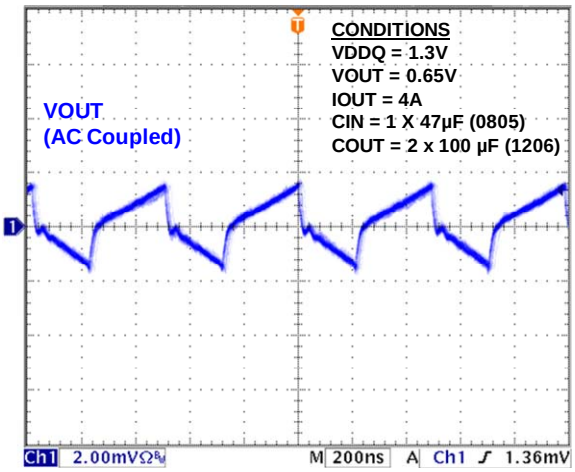
Output Ripple at 20MHz Bandwidth



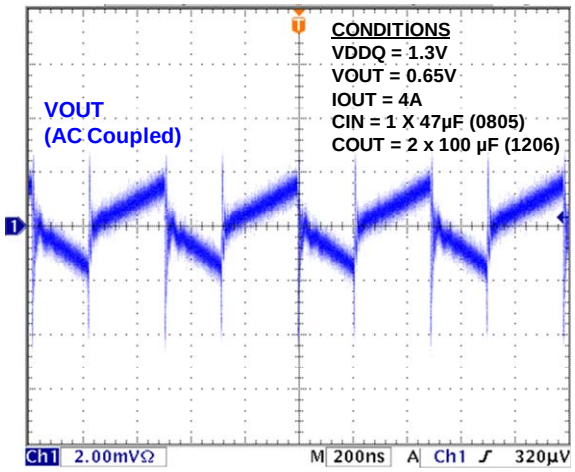
Output Ripple at Full Bandwidth



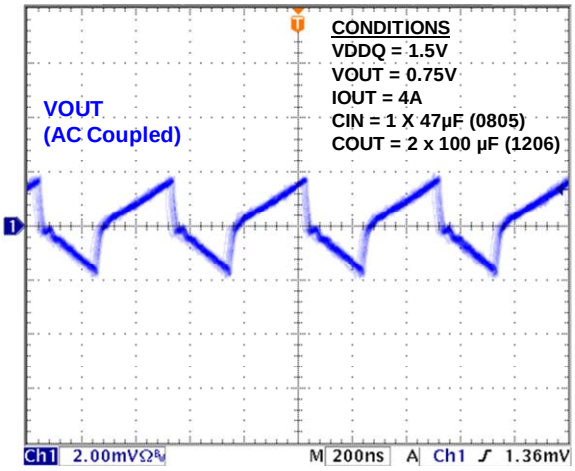
Output Ripple at 20MHz Bandwidth



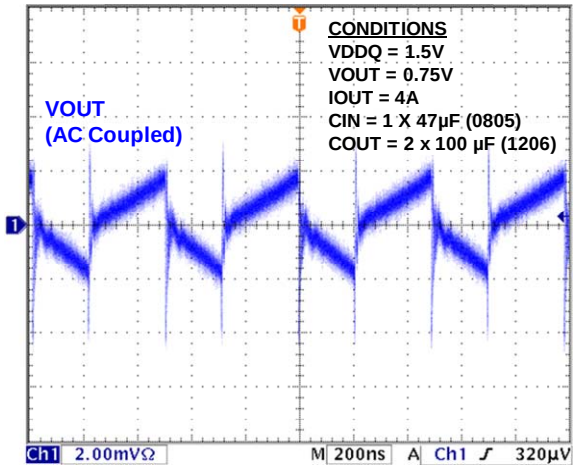
Output Ripple at Full Bandwidth



Output Ripple at 20MHz Bandwidth

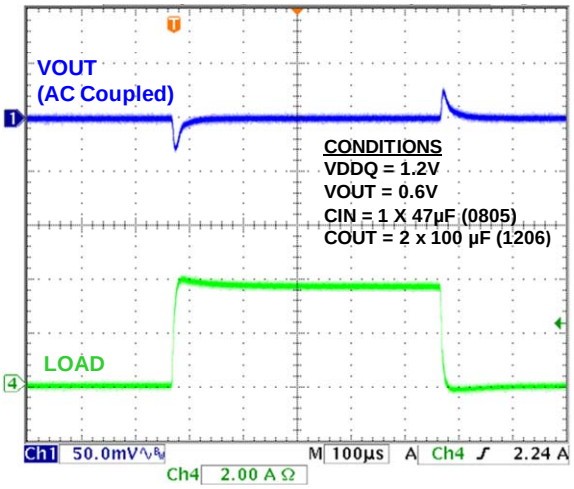


Output Ripple at Full Bandwidth

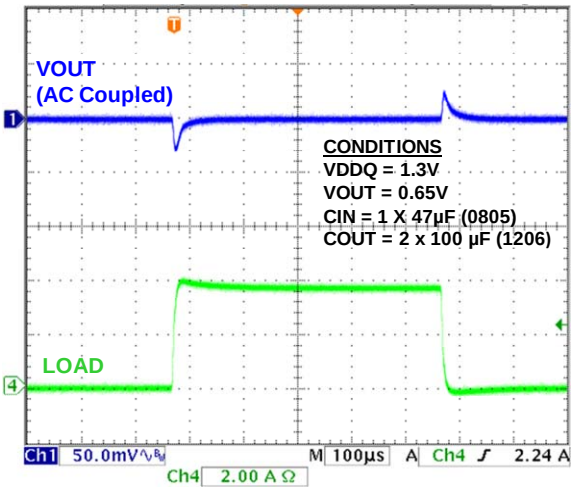


Typical Performance Characteristics (Continued)

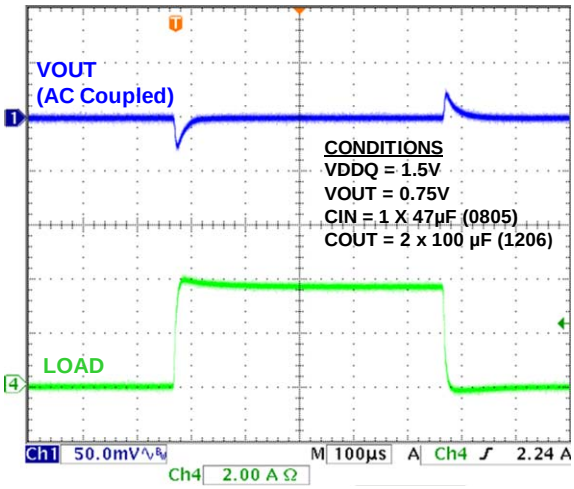
Load Transient from 0 to 4A



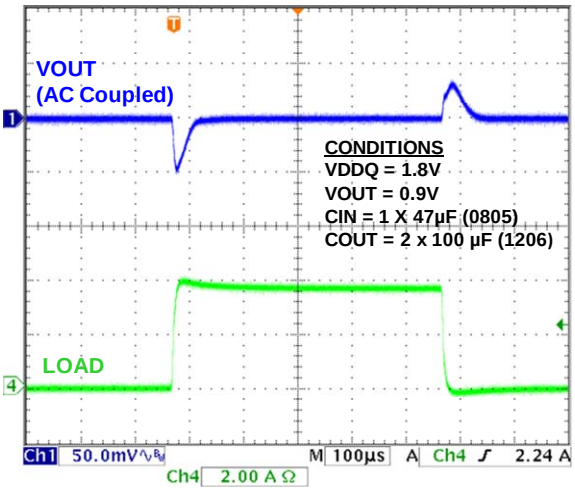
Load Transient from 0 to 4A



Load Transient from 0 to 4A



Load Transient from 0 to 4A



Functional Block Diagram

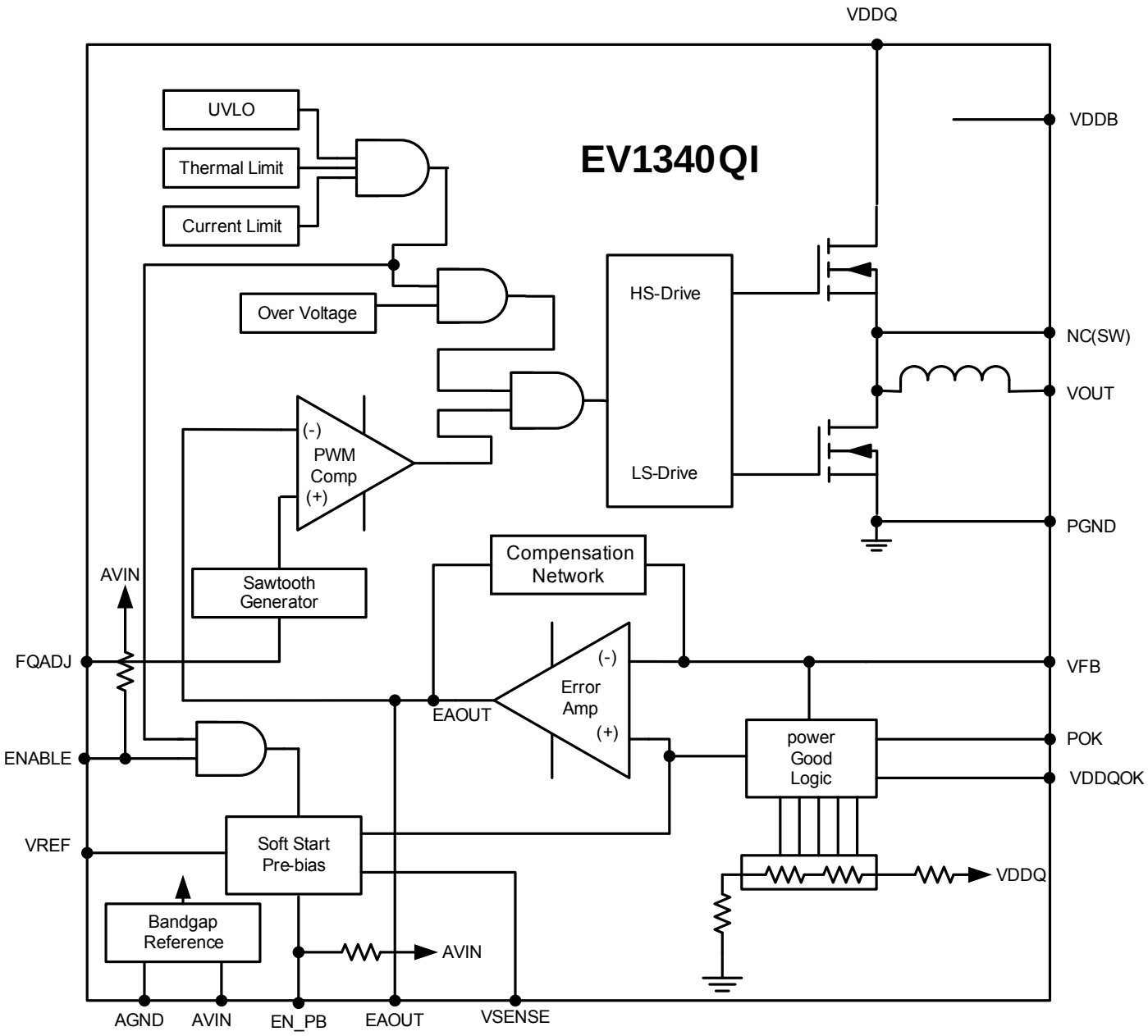


Figure 4: Functional Block Diagram

Functional Description

Synchronous Buck Converter

The EV1340 is a synchronous, programmable buck power supply with integrated power MOSFET switches and integrated inductor. The switching supply uses voltage mode control and a low noise PWM topology. Typically two power sources are required to operate this device; a power supply for the controller (AVIN) with a nominal input voltage range of 2.9-3.7V. The second supply (VDDQ) is the supply that is tracked - the recommended operating range is 1.0 to 1.8V. With the right choice of input and output dividers, the output voltage of the EV1340 will produce an output voltage which tracks to ½ VDDQ. The EV1340 can continuously source or sink currents up to 4A. The 1.5MHz nominal switching frequency enables small-size input and output capacitors.

Soft-Start and Soft-Shutdown

The EV1340 is expected to operate with the controller power supply (AVIN) ON, ENABLE High, and VDDQ ramped up and down at a relatively slow rate (~1V/mS). It is also expected that VDDQ may be dynamically scaled within a small voltage range. If, however, VDDQ should ramp up at a high rate, or if the device is enabled with a stable VDDQ, a capacitor connected between VREF and AGND provides the soft-start function to limit in-rush current. The soft-start time constant is determined by the input voltage divider and the soft-start capacitor. See figure 5.

Pre-Bias Start-up

The EV1340 supports start up into a pre-biased load. A proprietary circuit ensures the output voltage ramps up monotonically from the pre-bias value to the programmed output voltage. Monotonic start-up is guaranteed for pre-bias voltages in the range of >20% to <85% of the programmed output voltage. Outside of this range, the output voltage may not rise monotonically. The Pre-Bias feature is controlled by the EN_PB pin. For the pre-Bias feature to function properly, VDDQ must be stable; Enable must be toggled; and a pre-bias must be present at the output.

POK Operation

The internal POK signal is asserted when VDDQ > 0.3V and 0.45*VDDQ < VOUT < 0.55*VDDQ, indicating VOUT is tracking VDDQ. This assertion range assumes typical VDDQ slew rates associated with VDDQ POL regulators. For typical VDDQ POL regulators, the VDDQ ramp rate will range from 0.5 V/mSec to 2 V/mSec. Within this range of slew rates, the speed of the POK circuit, the loop bandwidth, and the delay caused by the soft-start capacitor on the VREF pin will not significantly affect the measured POK threshold. For much faster VDDQ ramp rates, hot-plug slew rates for example, the speed and latency of the elements will cause the measured VOUT voltage where POK is valid to be higher than the actual threshold.

The internal EV1340 POK is AND'ed with the VDDQOK input. The VDDQOK input is driven by the upstream VDDQ regulator's POK output. Normally the VDDQOK input indicates that VDDQ has settled to the required level. If VDDQ is dynamically switched, VDDQOK is expected to mask the EV1340 POK during the voltage transition. POK is not guaranteed to be valid when VDDQ < 300mV. The POK signal is asserted high when rising VOUT voltage crosses 46% (nominal) of VDDQ. POK is de-asserted low ~64 clock cycles after the falling VOUT voltage crosses 45% (nominal) of VDDQ. POK is also de-asserted if VOUT exceeds 55% (nominal) of VDDQ. For proper POK thresholds, the input voltage divider must generate VREF = 1/3*VDDQ.

Over Current Protection

The current limit function is achieved by sensing the current flowing in the hi-Side FET. When the sensed current exceeds the current limit, both power FETs are turned off for the rest of the switching cycle. If the over-current condition lasts only a few switching cycles,

normal PWM operation is resumed. If the over-current condition persists, the circuit will continue to protect the load by entering a hiccup mode. In the hiccup mode, the output is disabled for approximately 20ms and then it goes through a soft-start. The output will no longer track the input voltage briefly as a result of the fault condition. This cycle can continue indefinitely as long as the over current condition persists.

Thermal Overload Protection

Temperature sensing circuits in the controller will disable operation when the Junction temperature exceeds approximately 150ºC. When the junction temperature drops by approx 20ºC, the converter will re-start with a normal soft-start cycle.

Input Under-Voltage Lock-Out

When the input voltage is below a required voltage level (V_{UVHI}) for normal operation, converter switching is inhibited. The lock-out threshold has hysteresis to prevent chatter. When the device is operating normally, the input voltage must fall below the lower threshold (V_{UVLO}) for the device to stop switching.

Application Information / Layout Recommendation

Soft-start Capacitor Selection

A soft-start capacitor is recommended on the EV1340's VREF pin. The soft start capacitor serves as both a noise filter for noise on VDDQ as well as a slew rate limiter for fast VDDQ input ramps. The soft start time constant is determined by the value of this capacitor and the input divider resistors Rc and Rd. See figure 5. Enpirion recommends a 15nF value capacitor on this node.

Output Voltage Programming and loop Compensation

The output voltage of EV1340QI is determined by the two voltage dividers as shown in the simplified application diagram below:

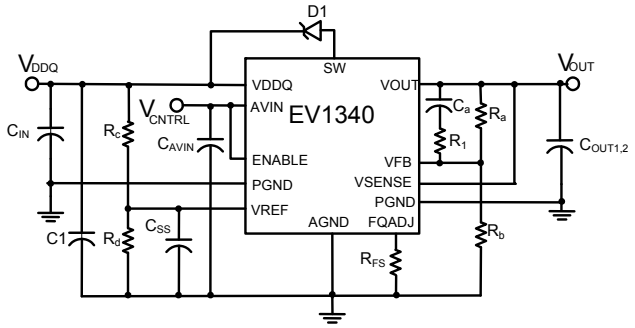


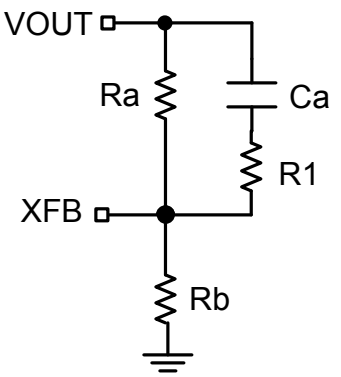
Figure 5: Typical Application Schematic

The input voltage divider consisting of R_c and R_d should be selected to make VREF = 0.4 * VDDQ for proper POK operation. Enpirion recommends R_c = 15kOhms and R_d = 10kOhms. This requirement is essential for proper operation of POK.
In steady state, VREF = VFB, and VOUT = 0.5 *VDDQ.

Although the EV1340 integrates most of the compensation network, a phase lead capacitor and a resistor are required in parallel with the upper resistor R_a of the external feedback network (see Figure 6).

The compensation is optimized for use with 2X100µF, 1206, X5R or X7R ceramic output capacitors.

In exceptional cases, modifications to the compensation might be required. The EV1340's compensation can be modified for specific applications. For more information, contact Enpirion Applications Engineering support.



$R_a = 100 * VDDQ \quad k\Omega$

Where VDDQ in volts

$$C_a = \frac{5 * 10^{-6}}{R_a} \quad F$$

Where R_a in Ohm

$R_1 = 3k\Omega$

$R_b = 4R_a$

Figure 6: External Feedback and Compensation Network

Enable Operation

With the device input power applied, the device automatically starts to operate with a soft-start, provided the AVIN voltage is above the upper UVLO high threshold.

Input Capacitor Selection

The EV1340 requires approximately 50µF of input capacitance for VDDQ. Additional capacitors (C_{AVIN} and C1) of 10µF is recommended for AVIN and the resistor divider network of VREF (Rc, Rd). Low ESR ceramic capacitors are required with X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations must not be used because these dielectrics lose capacitance with frequency, temperature and bias voltage.

In some applications, lower value ceramic capacitors maybe needed in parallel with the larger capacitors in order to provide high frequency decoupling.

Recommended Input Capacitors

Description	MFG	P/N
47µF, 10V, X5R, 1206	Taiyo Yuden	LMK316BJ476ML-T
47µF, 4V, X5R, 0805	Murata	GRM21BR60G476M

Output Capacitor Selection

The EV1340 has been optimized for use with an output capacitance of 200µF. Low ESR ceramic capacitors are required with X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose capacitance with frequency, temperature and bias voltage.

Recommended Output Capacitors

Description	MFG	P/N
47µF, 10V, X5R, 1206	Taiyo Yuden	LMK316BJ476ML-T
47µF, 6.3V, X5R, 1206	Taiyo Yuden Murata	JMK316BJ476ML-T GRM31CR60J476ME19L
100µF, 6.3V, X5R, 1206	Murata	GRM31CR60J107M

Output ripple voltage is primarily determined by the aggregate output capacitor impedance. At the 1.5MHz switching frequency output impedance, denoted as Z, is comprised mainly of effective series resistance, ESR, and effective series inductance, ESL:

Z = ESR + ESL.

Placing multiple capacitors in parallel reduces the impedance and hence will result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + ... + \frac{1}{Z_n}$$

Typical Ripple Voltages

Output Capacitor Configuration	Typical Output Ripple (mVp-p) VDDQ = 1.5V, V_{OUT} = 0.75V
2 x 100 µF	<10mV

Low V_{IN} Applications

The EV1340 is an excellent solution for low V_{IN} applications where highest efficiency is very critical. Reference the low V_{IN} efficiency chart in the Typical Performance Characteristics section for estimated efficiencies at several use cases. In these applications, a precision voltage reference is required for the VREF input of the EV1340. Figure 7 shows a schematic for a typical low V_{IN} application.

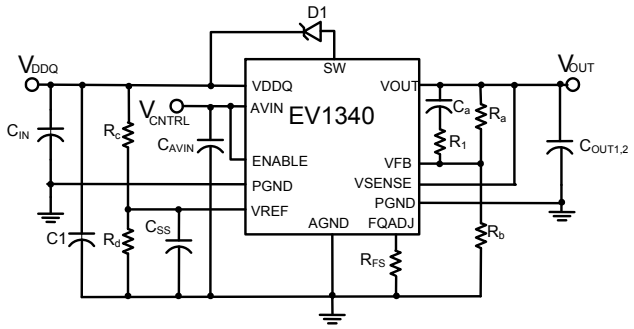


Figure 7: Typical Low V_{IN} Application Schematic

Layout Recommendations

Figure 8 and Figure 9 shows critical components along with top and bottom traces of a recommended minimum footprint of the EV1340QI layout with ENABLE tied to V_{IN}. Alternate ENABLE configurations and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Enpirion website www.enpirion.com for exact dimensions and other layers. Please refer to this Figure while reading the layout recommendations in this section.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EV1340QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EV1340QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: There are a total of seven PGND pins dedicated to the input and output circuits. The input and output ground should be separated until they reach the seven PGND pins to help minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files on the Enpirion website www.enpirion.com.

Recommendation 4: The large thermal pad underneath the component must be connected to the system ground plane through as many vias as possible.

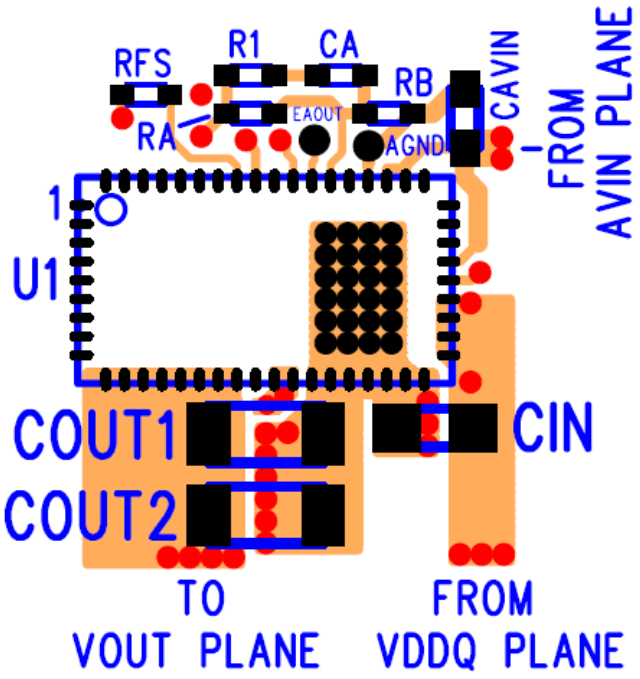


Figure 8: Top PCB Layer with Critical Components and Copper for Minimum Footprint

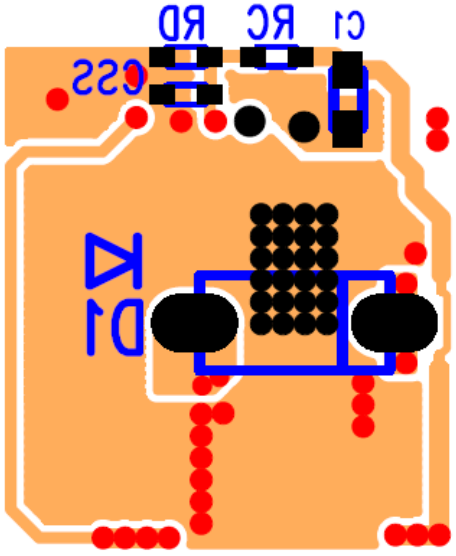


Figure 9: Bottom PCB Layer with Critical Components and Copper for Minimum Footprint

The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter. Please see Figure 8 and Figure 9.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4 should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 8 and Figure 9. These vias connect the input/output filter capacitors to the GND plane and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 6: AVIN1 and AVIN2 is the power supply for the internal small-signal control circuits. AVIN1 and AVIN2 should be powered by an external supply. In Figure 8, the filter capacitor C_{AVIN} is connected closely from the AVIN1 and AVIN2 pins to AGND for proper filtering of the control circuit.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 8. See the section regarding exposed metal on bottom of package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

Recommendation 9: Keep R_A, C_A, R1 and R_B close to the VFB pin (see Figure 8). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND pin instead of going through the GND plane.

Recommendation 10: Connect AGND to the ground plane through a single via as close to the AGND pin as possible. This establishes the connection between AGND and PGND.

Recommendation 11: The VREF sets the reference voltage for VOUT and should be as clean as possible. The connection from VDDQ to VREF should begin from the CIN1 input capacitor to the VREF through a resistor voltage divider (Rc, Rd). A bypass capacitor C1 should be placed close to the Rc resistor for additional filtering. The long trace from VDDQ to C1 will form a low pas filter and help reduce noise coupling to VREF.

Recommendation 12: The Schottky diode (D1) should be connected from the switch node to VDDQ with very low inductance traces. Place D1 directly under the device as shown in Figures 8 and 9 with vias from the SW pins to the bottom layer. Connect D1 to VDDQ through vias from the bottom layer to the top near the VDDQ pins. Contact Enpirion Applications Support for alternate placements for this diode.

Design Considerations

Exposed Metal on Bottom of Package

Package lead frames offer advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. They do, however, require some special considerations.

In the assembly process, lead-frame construction requires-for mechanical support-that some of the lead-frame cantilevers be exposed at the point where wire-bonds or internal passives are attached. Because of this lead frame requirement, several small pads are exposed on the bottom of the package. Only the large thermal pad and the perimeter pads should be mechanically or electrically connected to the PC board. The PCB top layer under the EV1340 should be clear of any metal except for the large thermal pad. The "grayed-out" area in Figure 10 represents the area that should be clear of all metal (traces, vias, or planes) on the top layer of the PCB.

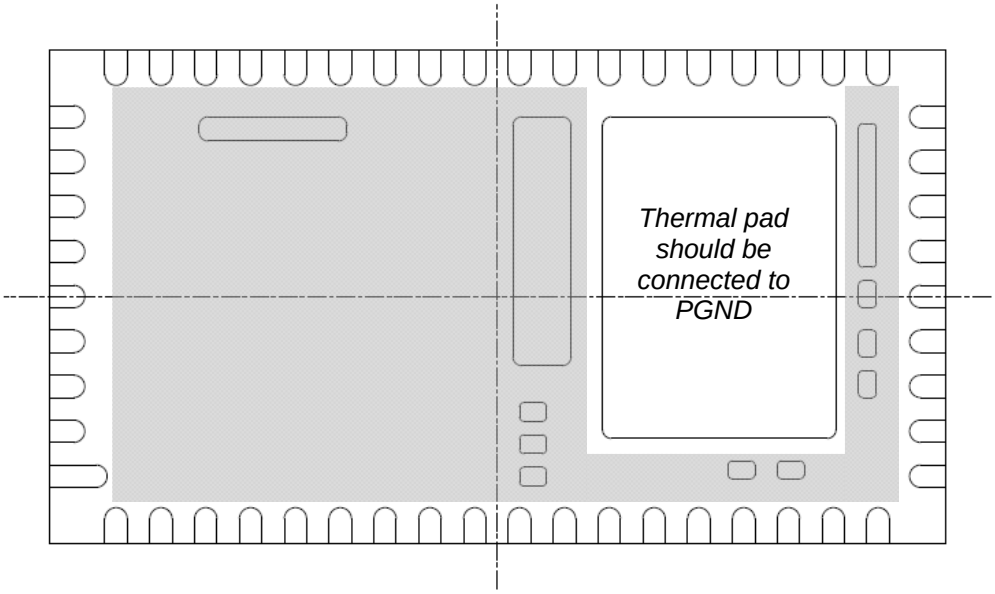


Figure 10: Lead-Frame Exposed Metal. Gray area highlights exposed metal below which there should not be any metal (traces, vias, or planes) on the top layer of the PCB

Recommended PCB Footprint

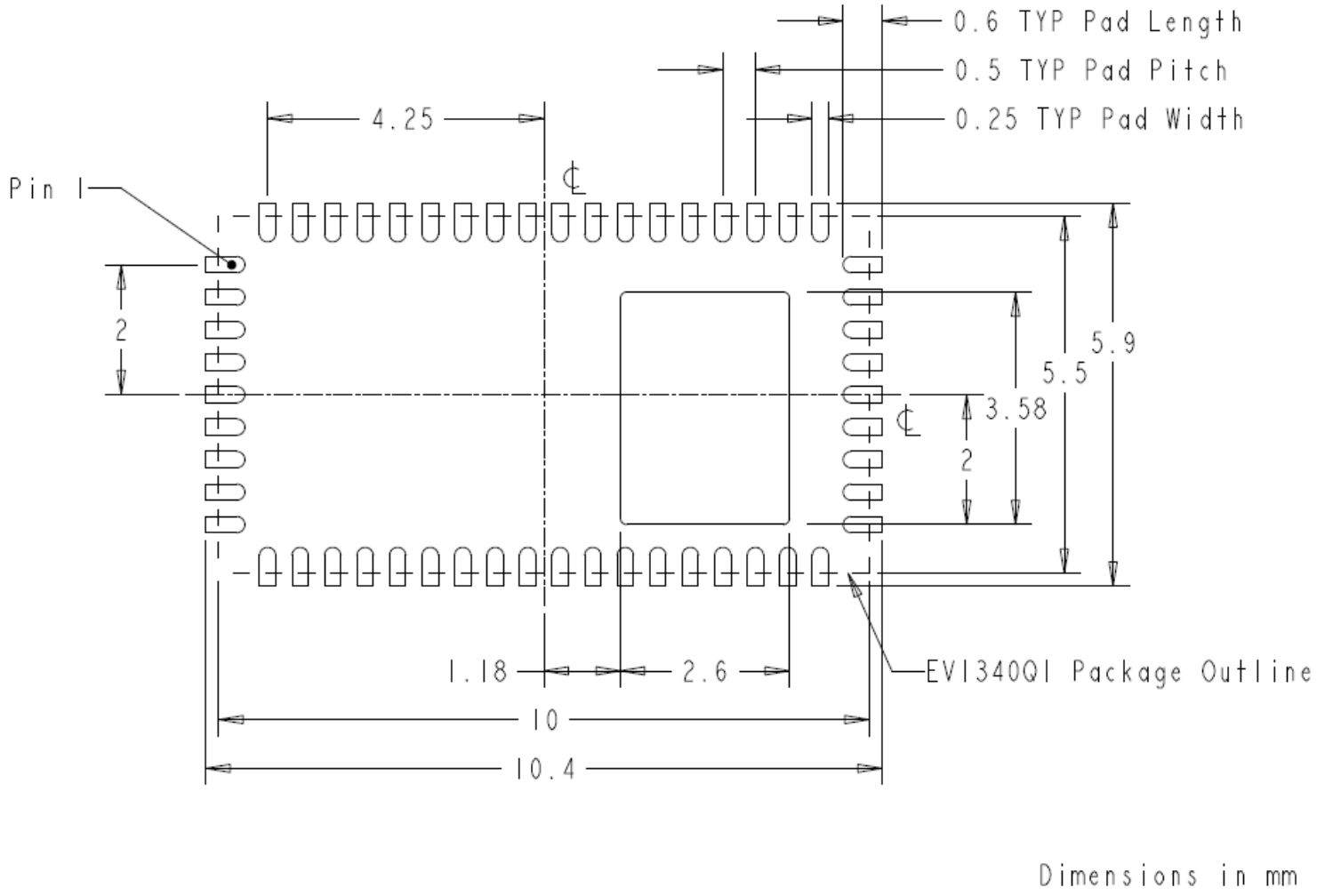


Figure 11: EV1340 Package PCB Footprint

Package and Mechanical

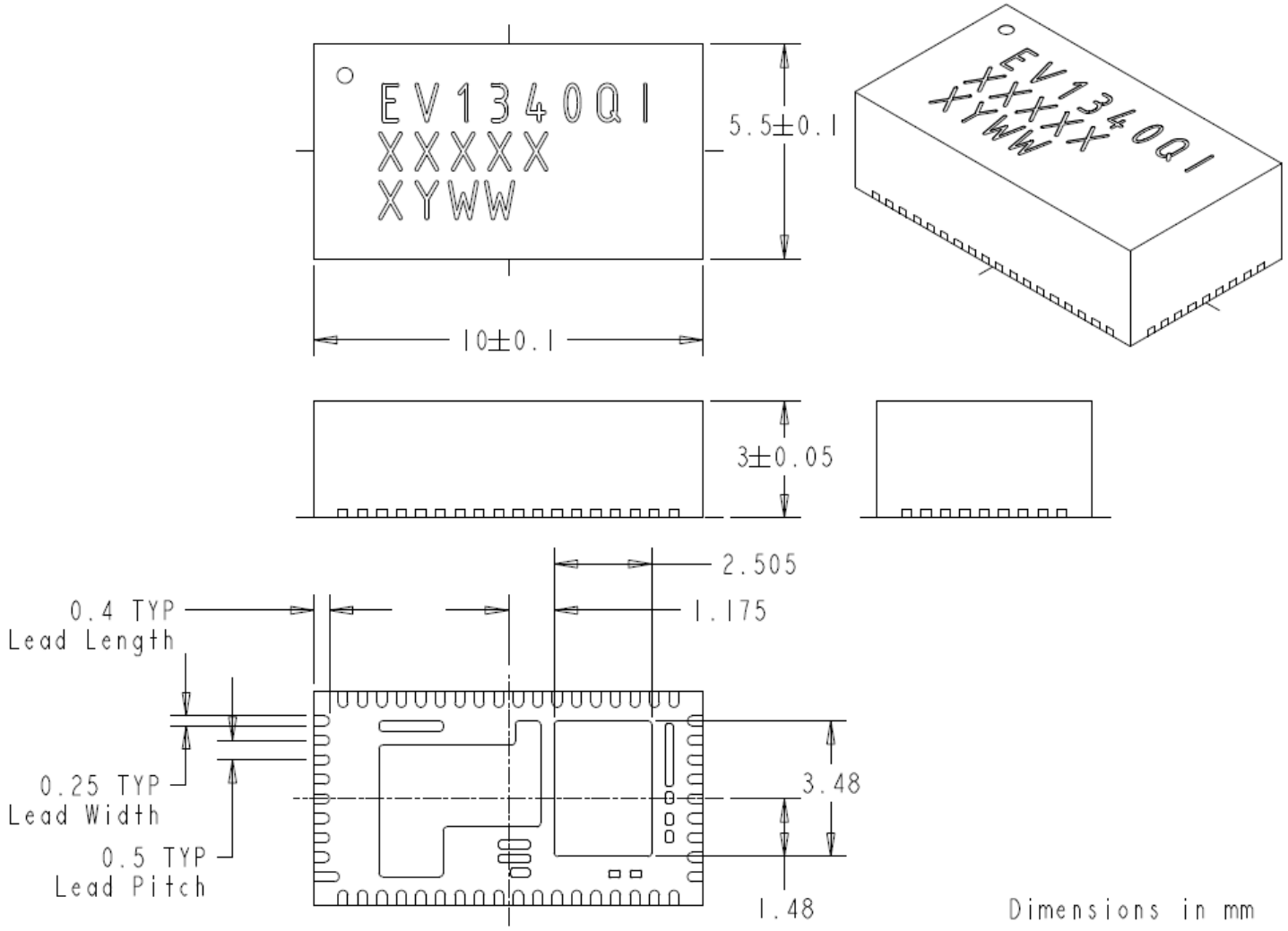


Figure 12: EV1340 Package Dimensions

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