EP53A8LQI/EP53A8HQI

1000mA Synchronous Buck Regulator With Integrated Inductor

3mm x 3mm x 1.1mm Package

November 2008

RoHS Compliant
Halogen Free

Product Overview

The EP53A8xQI (x = L or H) represents a break-through in power density at over 360mW/mm^2. The EP53A8xQI integrates MOSFET switches, control, compensation, and the magnetics in an advanced 3mm x 3mm QFN Package. Integrated magnetics enables a tiny solution footprint, low noise and EMI, low part-count, high reliability, while maintaining high efficiency. The complete solution can be implemented in less than 24mm^2.

Integrated Inductor greatly eases design constraints and speeds time to market

The EP53A8xQI uses a 3-pin VID to easily select the output voltage setting. Output voltage settings are available in 2 optimized ranges providing coverage for typical V_{OUT} settings. EP53A8LQI further has the option to use an external voltage divider.

Product Highlights

Featuring Integrated Inductor Technology

- **3mm x 3mm x 1.1mm QFN package**
- **Total Solution Footprint < 24mm^2**
- Low V_{OUT} ripple for RF compatibility
- High efficiency, up to 93%
- 1000mA continuous output current
- Less than 1 µA standby current
- 5 MHz switching frequency
- 3 pin VID for glitch free DVS
- V_{OUT} Range 0.6V to V_{IN} – 0.5V
- Short circuit and over current protection
- UVLO and thermal protection
- IC level reliability in a total solution

Applications

- Portable Wireless and RF applications
- Wireless broad band data cards
- Solid state storage applications
- Advanced Low Power Processors, DSP, IO, Memory, Video, Multimedia Engines

Typical Application Circuit

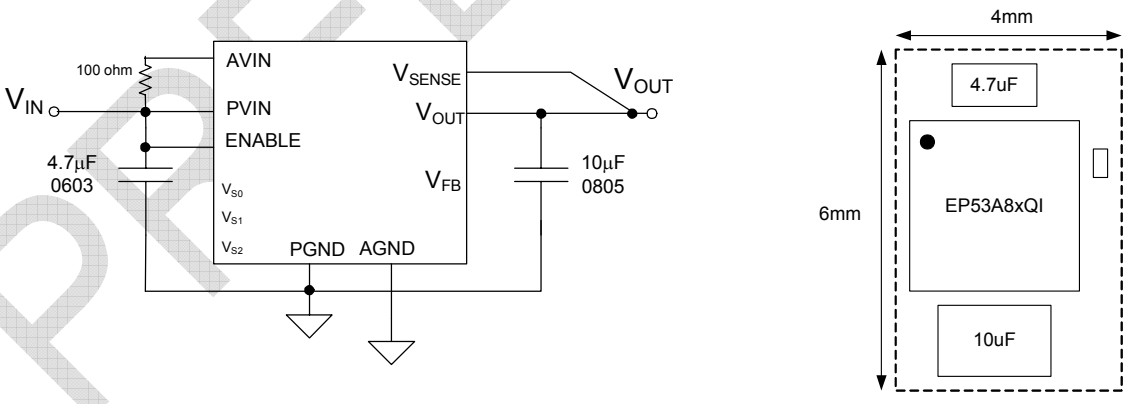


Figure 1. Typical application circuit and layout footprint.

Ordering Information

Part Number	Comment)	Package
EP53A8LQI-T	LOW VID Range	16-pin QFN T&R
EP53A8HQI-T	HIGH VID Range	16-pin QFN T&R
EP53A8LQI-E	EP53A8LQI Evaluation Board	
EP53A8HQI-E	EP53A8HQI Evaluation Board	

Pin Description

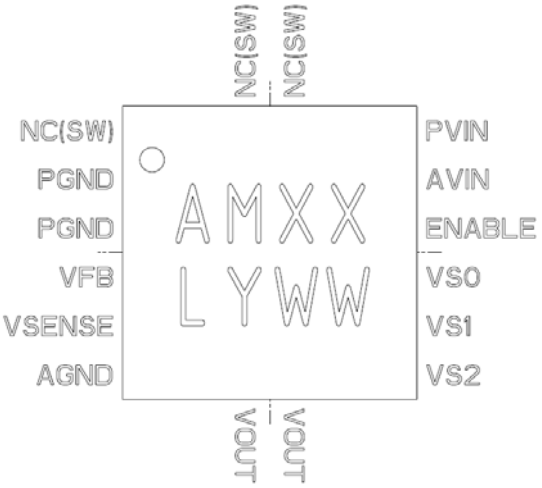


Figure 2A: EP53A8HQI Package Pin-out

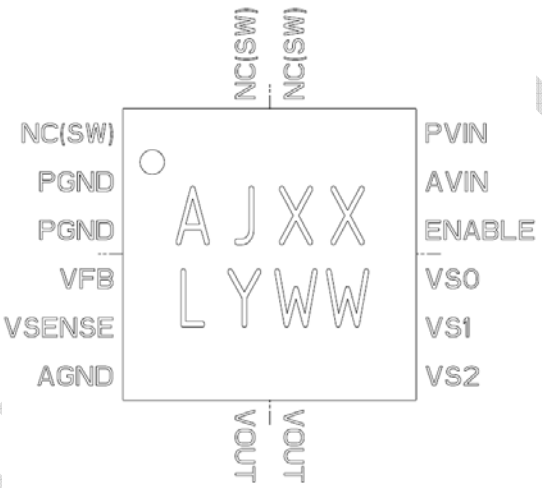


Figure 2B: EP53A8LQI Package Pin-out

PIN	NAME	FUNCTION
1, 15, 16	NC(SW)	No Connect. These pins are internally connected to the common drain output of the internal MOSFETs. NC(SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.
2, 3	PGND	Power Ground
4	VFB	EP53A8LQI: Feed back pin for external divider option. EP53A8HQI: No Connect
5	VSENSE	Sense pin for preset output voltages. Refer to application section for proper configuration
6	AGND	Analog ground. This is the quiet ground for the internal control circuitry. Ground return for external feedback voltage divider.
7,8	VOUT	Regulated Output Voltage. Refer to application section for proper layout and decoupling.
9,10, 11	VS2,VS1,VS0	Output voltage select. VS2=pin9, VS1=pin10 VS0=pin11. Selects one of seven preset output voltages (Eight preset output voltages for EP53A8HQI) or choose external divider by connecting pins to logic high or low. (Refer to section on output voltage select for more details.)
12	ENABLE	Output enable. Enable = logic high, disable = logic low.
13	AVIN	Analog input voltage.
14	PVIN	Input voltage for MOSFET switches.

Functional Block Diagram

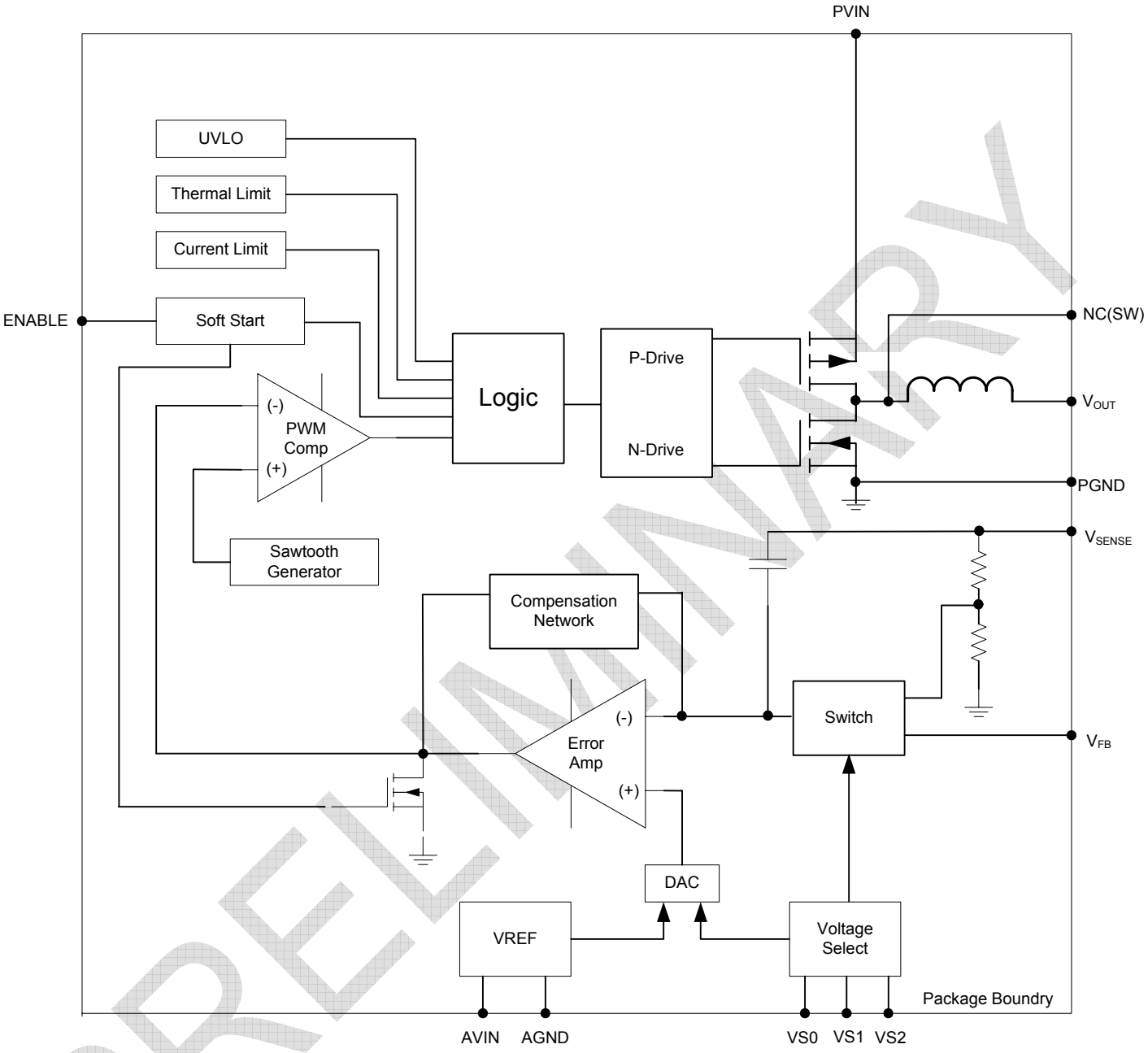


Figure 3. Functional block diagram.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond recommended operating conditions is not implied. Stress beyond absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage	V_{IN}	-0.3	7.0	V
Voltages on: ENABLE, V_{SENSE}, V_{S0}-V_{S2}		-0.3	V_{IN} + 0.3	V
Voltage on: V_{FB} (EP53A8LQI)		-0.3	2.7	V
Storage Temperature Range	T_{STG}	-65	150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020C			260	°C
ESD Rating (based on Human Body Model)			2000	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.4	5.5	V
Operating Ambient Temperature	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM)	θ_{JA}	100	°C/W
Thermal Overload Trip Point	T_{J-TP}	+150	°C
Thermal Overload Trip Point Hysteresis		15	°C

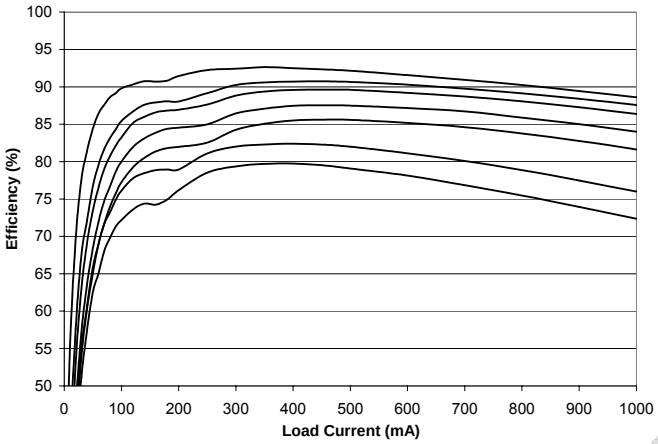
Electrical Characteristics

NOTE: T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, VIN = 3.6V.
C_{IN} =4.7µF 0603 MLCC, C_{OUT}=10uF 0805 MLCC.

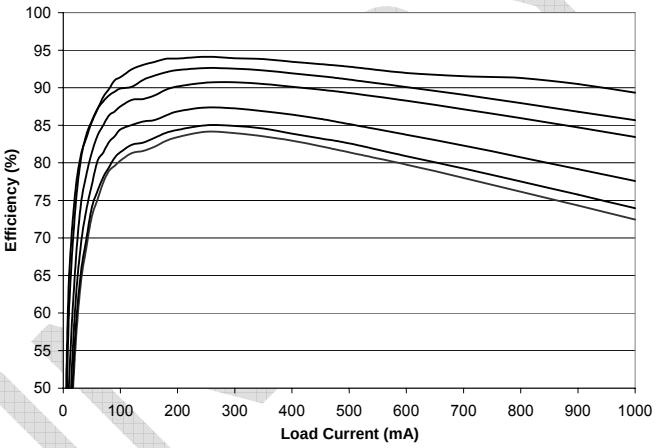
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Range	V_{OUT}	EP53A8LQI EP53A8HQI	0.6 1.8		V_{IN}-0.5 3.3	V
Dynamic Voltage Slew Rate	V_{slew}			4.2		mV/µS
V_{OUT} Initial Accuracy	ΔV_{OUT}	T_A = 25°C, V_{IN} = 3.6V, I_{LOAD} = 100mA;. 0.8V ≤ V_{OUT} ≤ 3.3V	-2		+2	%
Line Regulation	ΔV_{OUT_Line}	2.4V ≤ V_{IN} ≤ 5.5V		0.06		%/V
Load Regulation	ΔV_{OUT_Load}	0A ≤ I_{LOAD} ≤ 1000mA		0.3		%/ A
Temperature Variation	ΔV_{OUT_templ}	-40°C ≤ T_A ≤ +85°C		.00165		%/°C
Output Current	I_{OUT}		1000			mA
Shut-Down Current	I_{SD}	Enable = Low		0.75		µA
OCP Threshold	I_{LIM}	2.4V ≤ V_{IN} ≤ 5.5V; 0.6V ≤ V_{OUT} ≤ 3.3V		1.4		A
Feedback Pin Voltage	V_{FB}			0.6		V
Feedback Pin Input Current	I_{FB}			<100		nA
VS0-VS2, Pin Logic Low	V_{VSLO}		0.0		0.4	V
VS0-VS2, Pin Logic High	V_{VSHI}		1.4		Vin	V
VS0-VS2 Pin Input Current	I_{VSX}			<100		nA
Enable Pin Logic Low	V_{ENLO}				0.4	V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Enable Pin Logic High	V_{ENHi}		1.4			V
Operating Frequency	F_{OSC}	EP53A8LQI		5		MHz
Soft-Start Operation						
SoftStart Slew Rate	ΔV_{SS}			4.2		mV/uS

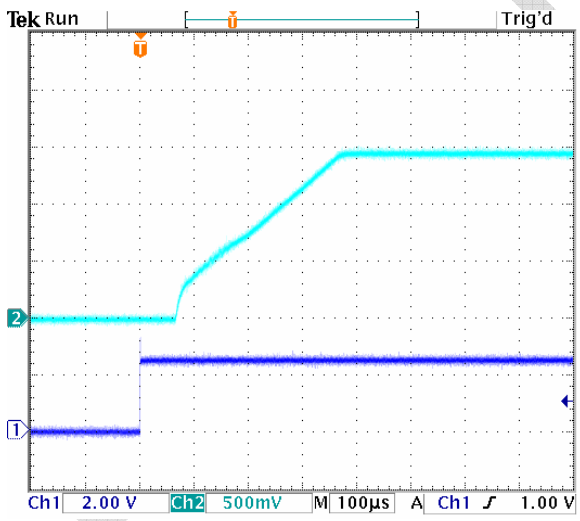
Typical Performance Characteristics



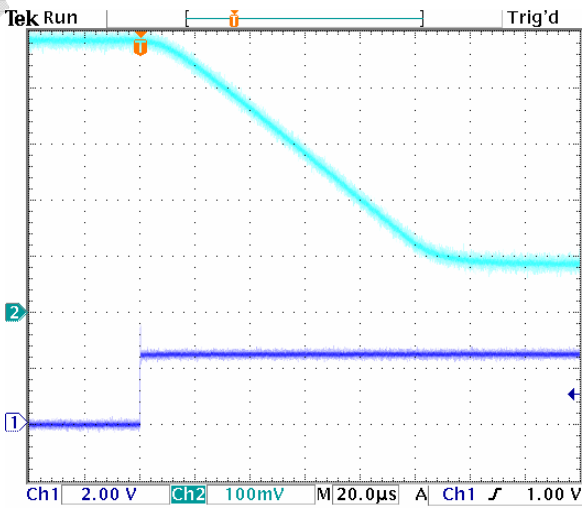
Efficiency vs. Load Current: V_{IN} = 5V, V_{OUT} = 3.7V, 3.3V, 3.0V, 2.5V, 2.1V, 1.5V, 1.2V,from top to bottom..



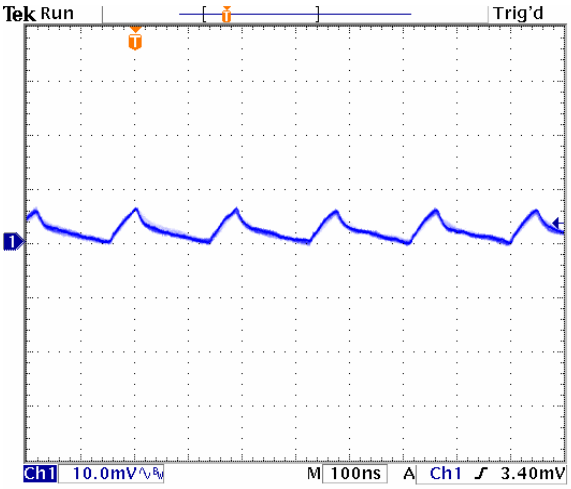
Efficiency vs. Load Current: V_{IN} = 3.3V, V_{OUT} = 3.0V, 2.5V, 2.1V, 1.5V, 1.2V, 1.1V, from top to bottom.



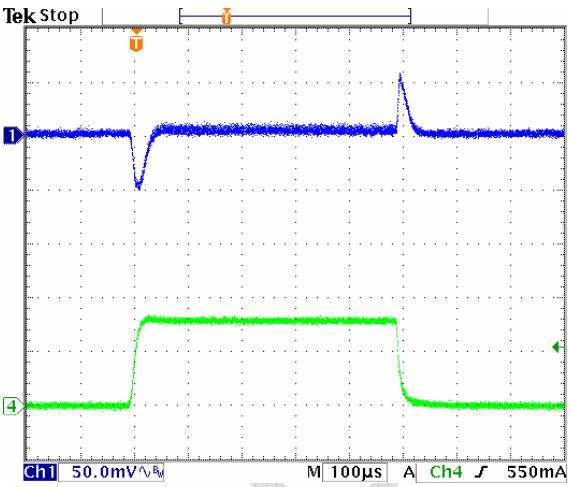
Start-up Waveform. V_{OUT} = 1.45V, Ch.1 Enable, Ch.2 V_{OUT}.



Dynamic Voltage Step. V_{OUT} = 1.5V step to 1.1V; Ch.1: VS2, Ch.2: V_{OUT} (DC Offset = 1.0V).



Output Ripple. V_{IN} = 5.0V, V_{OUT} = 1.2V, Load = 300mA.



Load Transient. V_{IN} = 3.7V, V_{OUT} = 1.2V
Load stepped from 0mA to 800mA.

Detailed Description

Functional Overview

The EP53A8xQI requires only 2 small MLCC capacitors and an 0201 MLC resistor for a complete DC-DC converter solution. The device integrates MOSFET switches, PWM controller, Gate-drive, compensation, and inductor into a tiny 3mm x 3mm x 1.1mm QFN package. Advanced package design, along with the high level of integration, provides very low noise and EMI. The EP53A8xQI uses voltage mode control for high noise immunity and load matching to advanced ≤90nm loads. A 3-pin VID allows the user to choose from one of 8 output voltage settings. The EP53A8xQI comes with two VID output voltage ranges. The EP53A8HQI is optimized for V_{OUT} settings from 1.8V to 3.3V, the EP53A8LQI provides VID settings from 0.8V to 1.5V, and also has an external resistor divider option to program output setting over the 0.6V to V_{IN}-0. 5V range. The EP53A8xQI provides the industry's highest power density of any 1A DCDC converter solution.

The key enabler of this revolutionary integration is Enpirion's proprietary power MOSFET technology. The advanced MOSFET switches are implemented in deep-submicron CMOS to supply very low switching loss at high switching frequencies and to allow a high level of integration. The semiconductor process allows seem-less integration of all switching, control, and compensation circuitry.

The proprietary magnetics design provides high-density/high-value magnetics in a very small footprint. Enpirion magnetics are carefully matched to the control and compensation circuitry yielding an optimal solution with assured performance over the entire operating range.

Protection features include under-voltage lock-out (UVLO), over-current protection (OCP), short circuit protection, and thermal overload protection.

Integrated Inductor: Low-Noise Low-EMI

The EP53A8xQI utilizes a proprietary low loss integrated inductor. The use of an internal inductor localizes the noises associated with the output loop currents. The inherent shielding and compact construction of the integrated inductor reduces the conducted and radiated noise that can couple into the traces of the

printed circuit board. Further, the package layout is optimized to reduce the electrical path length for the high di/dT input AC ripple currents that are a major source of radiated emissions from DC-DC converters. The integrated inductor significantly reduces parasitic effects that can harm loop stability, and makes layout very simple. The integrated inductor provides the optimal solution to ripple, noise, and EMI that plague low power design.

Control Matched to sub 90nm Loads

The EP53A8xQI utilizes an internal type III compensation network. Voltage mode control is inherently impedance matched to the sub 90nm process technology that is used in today's advanced ICs. Voltage mode control also provides a high degree of noise immunity at light load currents so that low ripple and high accuracy are maintained over the entire load range. The very high switching frequency allows for a very wide control loop bandwidth and hence excellent transient performance.

Soft Start

Internal soft start circuits limit in-rush current when the device starts up from a power down condition or when the "ENABLE" pin is asserted "high". Digital control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor.

Over Current/Short Circuit Protection

The current limit function is achieved by sensing the current flowing through a sense P-MOSFET which is compared to a reference current. When this level is exceeded the P-FET is turned off and the N-FET is turned on, pulling V_{OUT} low. This condition is maintained for approximately 1mS and then a normal soft start is initiated. If the over current condition still persists, this cycle will repeat.

Under Voltage Lockout

During initial power up an under voltage lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to insure proper operation. If the voltage drops below the UVLO threshold the lockout circuitry will again disable the switching. Hysteresis is included to prevent chattering between states.

Enable

The ENABLE pin provides a means to shut down the converter or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation.

NOTE: The ENABLE pin must not be left floating.

Thermal Shutdown

When excessive power is dissipated in the chip, the junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases by 15C°, the device will go through the normal startup process.

Application Information

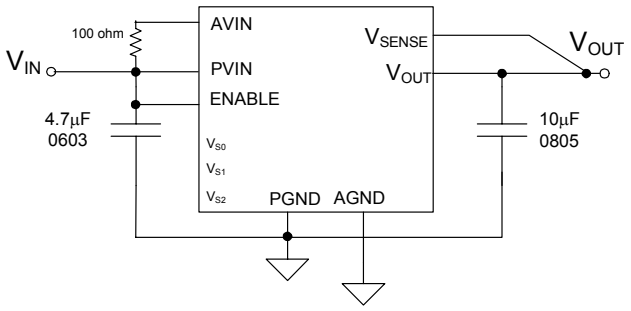


Figure 4. Application Circuit, EP53A8HQI.

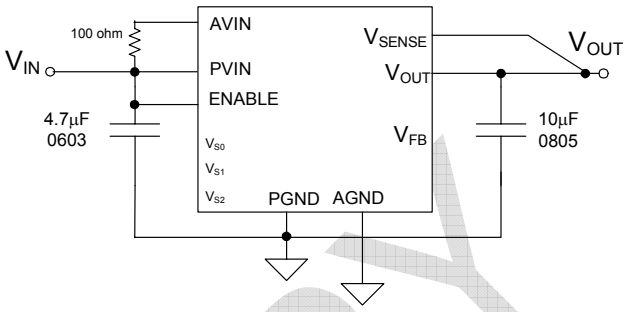


Figure 5. Application Circuit, EP53A8LQI.

Output Voltage Programming

The EP53A8xQI utilizes a 3-pin VID to program the output voltage value. The VID is available in two sets of output VID programming ranges.

The "Low" range is optimized for low voltage applications. It comes with VID steps of 50mV and ranges between 0.80V and 1.5V. This VID set also has an external divider option.

To specify this VID range, order part number EP53A8LQI.

The "High" VID range provides 100mV increments with output voltage settings ranging from 1.8V to 3.3V. This version does not have an external divider option. To specify this VID range, order part number EP53A8HQI.

Internally, the output of the VID multiplexer sets the value for the voltage reference DAC, which in turn is connected to the non-inverting input of the error amplifier. This allows the use of a single feedback divider with constant loop gain and optimum compensation, independent of the output voltage selected.

NOTE: The VID pins must not be left floating.

EP53A8L Low VID Range Programming

The EP53A8LQI is designed to provide a high degree of flexibility in powering applications that require low V_{OUT} settings and dynamic voltage scaling (DVS). The device employs a 3-pin VID architecture that allows the user to choose one of seven (7) preset output voltage settings, or the user can select an external voltage divider option. The VID pin settings can be changed on the fly to implement glitch-free voltage scaling.

Table 1 shows the VS2-VS0 pin logic states for the EP53A8LQI and the associated output voltage levels. A logic "1" indicates a connection to V_{IN} or to a "high" logic voltage level. A logic "0" indicates a connection to ground or to a "low" logic voltage level. These pins can be either hardwired to V_{IN} or GND or alternatively can be driven by standard logic levels. Logic low is defined as $V_{LOW} \leq 0.4V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate.

Table 1. EP53A8LQI VID Voltage Select Settings.

VS2	VS1	VS0	VOUT
0	0	0	1.50
0	0	1	1.45
0	1	0	1.20
0	1	1	1.15
1	0	0	1.10
1	0	1	1.05
1	1	0	0.8
1	1	1	EXT

EP53A8LQI External Voltage Divider

The external divider option is chosen by connecting VID pins VS2-VS0 to V_{IN} or a logic "1" or "high".. The EP53A8LQI uses a separate feedback pin, V_{FB}, when using the external divider. V_{SENSE} must be connected to V_{OUT} as indicated in Figure 5.

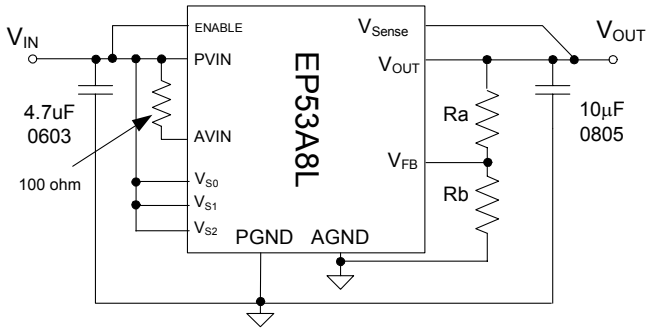


Figure 6. EP53A8LQI using external divider.

The output voltage is selected by the following formula:

$$V_{OUT} = 0.6V\left(1+\frac{Ra}{Rb}\right)$$

R_a must be chosen as 237KΩ to maintain loop gain. Then R_b is given as:

$$R_b = \frac{142.2x10^3}{V_{OUT}-0.6}\Omega$$

V_{OUT} can be programmed over the range of 0.6V to (V_{IN} – 0.5V).

NOTE: DVS is not allowed between internal preset voltages and external divider.

EP53A8HQI High VID Range Programming

The EP53A8HQI V_{OUT} settings are optimized for higher nominal voltages such as those required to power IO, RF, or IC memory. The preset voltages range from 1.8V to 3.3V. There are eight (8) preset output voltage settings. The EP53A8HQI does not have an external divider option. As with the EP53A8LQI, the VID pin settings can be changed while the device is enabled.

.

Table 2 shows the VS0-VS2 pin logic states for the EP53A8HQI and the associated output voltage levels. A logic "1" indicates a connection to V_{IN} or to a "high" logic voltage level. A logic "0" indicates a connection to ground or to a "low" logic voltage level. These pins can be either hardwired to V_{IN} or GND or alternatively can be driven by standard logic levels. Logic low is defined as $V_{LOW} \leq 0.4V$. Logic high is defined as $V_{HIGH} \geq 1.4V$. Any level between these two values is indeterminate. These pins must not be left floating.

Table 2. EP53A8HQI VID Voltage Select Settings.

VS2	VS1	VS0	VOUT
0	0	0	3.3
0	0	1	3.0
0	1	0	2.9
0	1	1	2.6
1	0	0	2.5
1	0	1	2.2
1	1	0	2.1
1	1	1	1.8

Input and Output Capacitors

The **input** capacitance requirement is 4.7uF 0603 low ESR MLCC capacitor. The input capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and with temperature, and are not suitable for switch-mode DC-DC converter input filter applications.

The **output** capacitance requirement is a 10uF. 0805 MLCC capacitor. Ripple performance can be improved by using 2x10uF 0603 MLCC capacitors.

The output capacitor must use a X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and temperature and are not suitable for switch-mode DC-DC converter output filter applications.

PCB Footprint

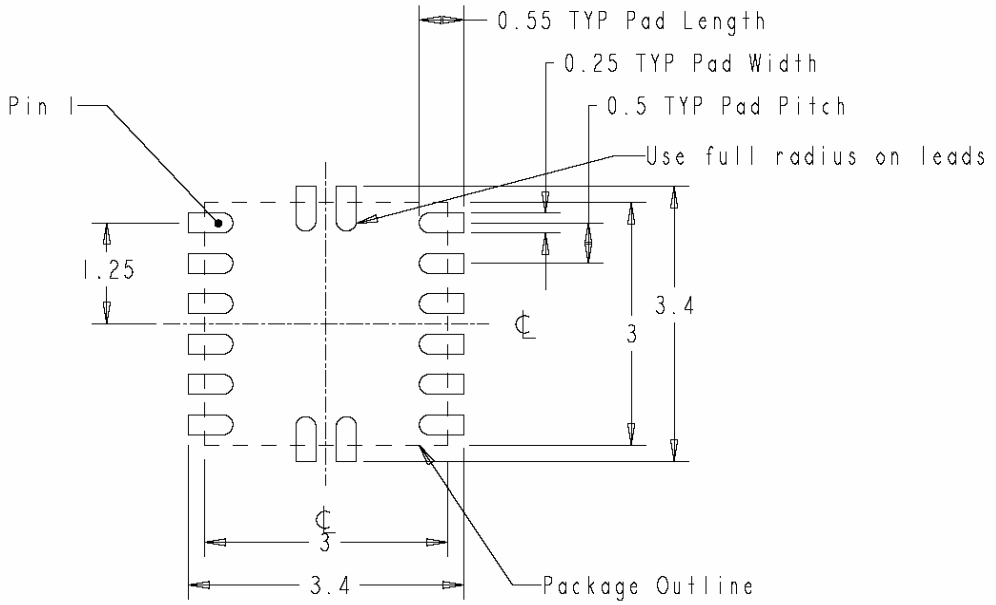


Figure 7. Recommended PCB footprint.

Package Dimensions

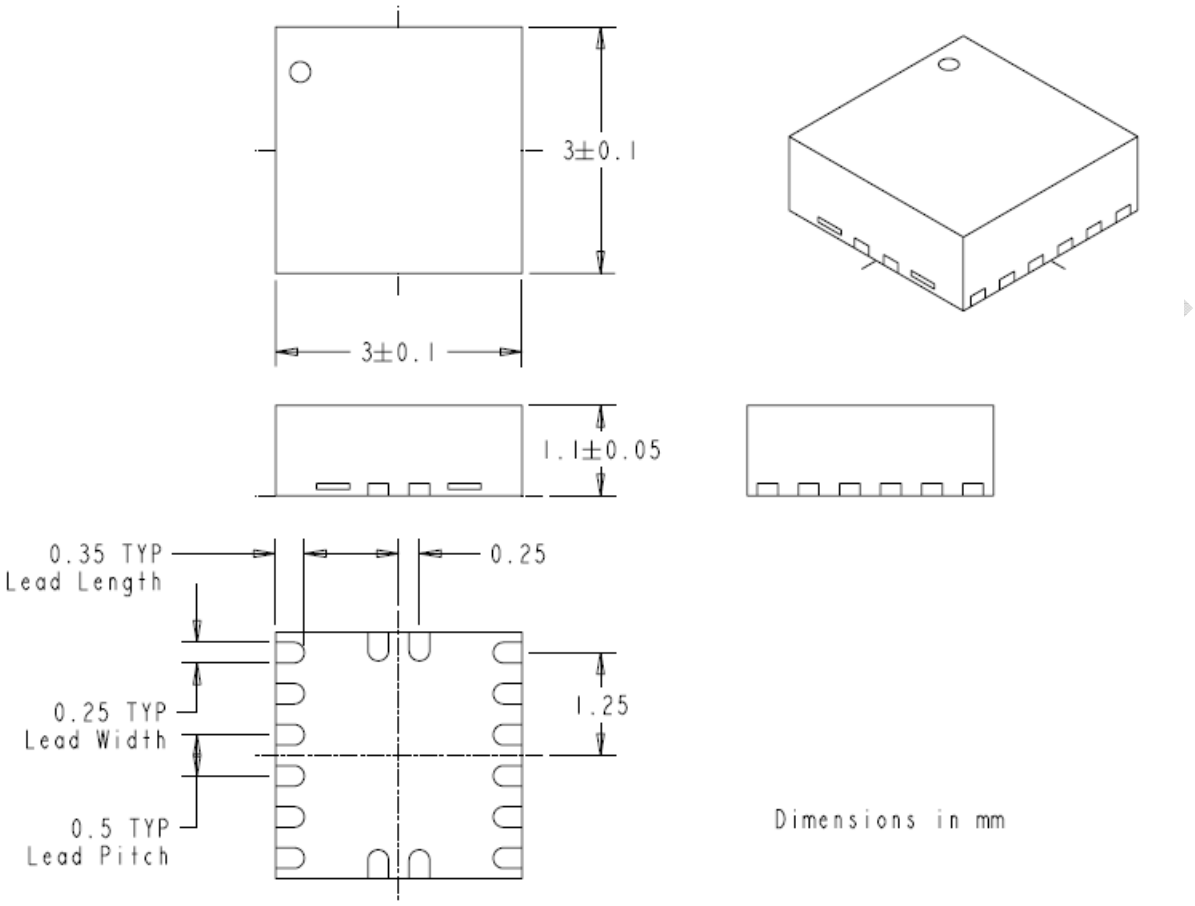


Figure 8. Package Dimensions.

Contact Information

Enpirion, Inc.
685 US Route 202/206 Suite 305
Bridgewater, NJ 08807
Phone: +1 908-575-7550
Fax: +1 908-575-0775