



*Image may not represent actual product

General Specifications

Pin Count	67 pin (M Key)
Form Factor	M.2 (80mm)
Unformatted Capacity	2000GB
Cache	Uncontrolled

Default Format	Unformatted
Voltage	3.3V
Interface	PCIe 4.0 x4, NVMe 1.3
Warranty	1 Year

Endurance/Power/Performance

Max Read Speed*	4950 MB/s
Max Write Speed*	4300 MB/s
Seq. Read Speed**	4950 MB/s
Seq. Write Speed**	4350 MB/s
4k Random Read***	450000 IOPs
4k Random Write***	530000 IOPs
Endurance (TBW)	

Active Power	6900 mW
Idle Power	20 mW
Sleep Power	2 mW
Shock Tolerance	1500G(.5ms duration, half sine wave)
Vibration Tolerance	20G(Peak,80-2000Hz)
MTBF	1,700,000 Hrs

NAND Specifications

NAND Manufacturer	NOT CONTROLLED
NAND Part Number	NOT CONTROLLED
NAND Type	TLC
NAND Geometry	3D

NAND Config.	NOT CONTROLLED
NAND Quantity	NOT CONTROLLED
NAND Package	NOT CONTROLLED
NAND Technology	Dual Plane

*Maximum speeds are determined using ATTO Disk Benchmark

**Maximum Sequential speeds measured using HD Tune Pro 5.75

***Maximum I/O performance is measured using IOMeter 2010, 4K bytes Random

Environment

Operating Temp	Commercial (0 to 70 C)
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Storage Temp	Storage (-40 to +85 C)
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Controller Specifications

Controller Mfg.	Phison
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Controller PN	PS5016-E16
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Wear Level Static	Enabled
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Wear Level Dynamic	Enabled
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Power Loss Protection	No
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RAID Support	Yes
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SMART Support	Yes
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TRIM Support	Yes
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ECC	LDPC Gen4 + RAID
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Data Encryption	AES 256-bit & Pyrite
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Certifications

ROHS	Yes
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Pin Out Diagram

Pin Assignment and Description

Pin No.	PCIe Pin	Description	Pin No.	PCIe Pin	Description
1	GND	CONFIG_3 = GND	30	N/C	No connect
2	3.3V	3.3V source	31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
3	GND	Ground	32	N/C	No connect
4	3.3V	3.3V source	33	GND	Ground
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec	34	N/C	No connect
6	N/C	No connect	35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec	36	N/C	No connect
8	N/C	No connect	37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
9	GND	Ground	38	N/C	No connect
10	LED1#	Open drain, active low signal. These signals are used to allow the addn card to provide status indicators via LED devices that will be provided by the system.	39	GND	Ground
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec	40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pullup on platform
12	3.3V	3.3V source	41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec	42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pullup on platform.
14	3.3V	3.3V source	43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
15	GND	Ground	44	ALERT#(O) (0/1.8V)	Alert notification to master; Open Drain with pullup on platform; Active low.
16	3.3V	3.3V source	45	GND	Ground
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec	46	N/C	No connect
18	3.3V	3.3V source	47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec	48	N/C	No connect
20	N/C	No connect	49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
21	GND	Ground	50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
22	N/C	No connect	51	GND	Ground
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec	52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Substates.
24	N/C	No connect	53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec
25	PERp2	PCIe RX Differential signal defined by the PCIe Express M.2 spec	54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
26	N/C	No connect	55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec
27	GND	Ground	56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only Not used in normal operation. Pins should be left N/C in platform Socket.
28	N/C	No connect	57	GND	Ground
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec			
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.			
59	Module Key M	Module Key			
60	Module Key M				
61	Module Key M				
62	Module Key M				
63	Module Key M				
64	Module Key M				
65	Module Key M				
66	Module Key M				
67	N/C	No connect			
68	SUSCLK(32KHz) (I)(0/3.3V)	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module.			
69	N/C	PEDET (NC-PCIe)			
70	3.3V	3.3V source			
71	GND	Ground			
72	3.3V	3.3V source			
73	GND	Ground			
74	3.3V	3.3V source			
75	GND	Ground			

Physical Dimensions

Physical Product Dimension : 80.00mm (L) x 22mm (W) x 1.20mm (H)

