

Centon OEM SSD Commercial, TLC, PCIe 4.0 x4, NVMe 1.3, M.2-2280, 2000GB



*Image may not represent actual product

General Specifications

Pin Count	67 pin (M Key)	Default Format	Unformatted
Form Factor	M.2 (80mm)	Voltage	3.3V
Unformatted Capacity	2000GB	Interface	PCIe 4.0 x4, NVMe 1.3
Cache	Uncontrolled	Warranty	1 Year

Endurance/Power/Performance

Max Read Speed*	4950 MB/s	Active Power	6900 mW
Max Write Speed*	4300 MB/s	Idle Power	20 mW
Seq. Read Speed**	4950 MB/s	Sleep Power	2 mW
Seq. Write Speed**	4350 MB/s	Shock Tolerance	1500G(.5ms duration, half sine wave)
4k Random Read***	450000 IOPs	Vibration Tolerance	20G(Peak,80-2000Hz)
4k Random Write***	530000 IOPs	MTBF	1,700,000 Hrs
Endurance (TBW)			

NAND Specifications

NAND Manufacturer	NOT CONTROLLED	NAND Config.	NOT CONTROLLED
NAND Part Number	NOT CONTROLLED	NAND Quantity	NOT CONTROLLED
NAND Type	TLC	NAND Package	NOT CONTROLLED
NAND Geometry	3D	NAND Technology	Dual Plane

*Maximum speeds are determined using ATTO Disk Benchmark **Maximum Sequential speeds measured using HD Tune Pro 5.75

***Maximum I/O performance is measured using IOMeter 2010, 4K bytes Random

C3-CT-X44E-2.1A

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Environment				
Operating Temp	Commercial (0 to 70 C)	Storage Temp	Storage (-40 to +85 C)	
Controller Specifications				
Controller Mfg.	Phison	RAID Support	Yes	
Controller PN	PS5016-E16	SMART Support	Yes	
Wear Level Static	Enabled	TRIM Support	Yes	
Wear Level Dynamic	Enabled	ECC	LDPC Gen4 + RAID	
Power Loss Protection	No	Data Encryption	AES 256-bit & Pyrite	

Certifications

ROHS

Yes

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Pin Out Diagram

	Pin Ass	ignment and Description			
Pin No.	PCle Pin	Description	Pin No.	PCIe Pin	Description
1	GND	CONFIG_3 = GND	30	N/C	No connect
2	3.3V	3.3V source	31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
3	GND	Ground	32	N/C	No connect
4	3.3V	3.3V source	33	GND	Ground
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec	34	N/C	No connect
6	N/C	No connect	35	PERn1	PCIe RX Differential signaldefined by the PCI Express M.2 spec
7	РЕТр3	PCIe TX Differential signal defined by the PCI Express M.2 spec	36	N/C	No connect
8	N/C	No connect	37	PERp1	PCIe RX Differential signaldefined by the PCI Express M.2 spec
9	GND	Ground	38	N/C	No connect
		Open drain, active low signal. These signals are used to allow the addin	39	GND	Ground
10	LED1#	card to provide status indicators via LED devices that will be provided by	40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pullup on platform
		the system.	41	PETn0	PCIe TX Differential signaldefined by the PCI Express M.2 spec
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec	42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pullup on platform.
12	3.3V	3.3V source	43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec			Alert notification to master; Open Drain with pullup on platform;
14	3.3V	3.3V source	44	ALERT#(O) (0/1.8V)	Active low.
15	GND	Ground	45	GND	Ground
16	3.3V	3.3V source	46	N/C	No connect
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec	47	PERnO	PCIe RX Differential signaldefined by the PCI Express M2 spec
18	3.3V	3.3V source	48	N/C	No connect
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec	49	PERp0	PCIe RX Differential signaldefined by the PCI Express M.2 spec
20	N/C	No connect			PE-Reset is a functional reset to the cardas defined by the PCIe Min
21	GND	Ground	50	PERST#(I)(0/3.3V)	CEM specification.
22	N/C	No connect	51	GND	Ground
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec			Clock Request is a reference clock request signal as defined by the PC
24	N/C	No connect	52	CLKREQ#(I/O)(0/3.3V)	Mini CEM specification; Also used by L1 PM Substates.
25	PERp2	PCIe RX Differential signal defined by the PCExpress M.2 spec			PCIe Reference Clock signals (100 MHz)
26	N/C	No connect	53	REFCLKn	defined by the PCI Express M.2 spec.
27	GND	Ground			PCIe PME Wake.
28	N/C	No connect	54	PEWAKE#(I/O)(0/3.3V)	Open Drain with pull up on platform;Active Low.
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec			PCIe Reference Clock signals (100 MHz)
25	FEINI	FCIE TA Differencial signal defined by the FCI LAPIESS W.2 spec	55	REFCLKp	defined by the PCI Express M.2 spec.
		Manufacturing Clock line. Used for SSD manufacturing only.			Manufacturing Data line. Used for SSD manufacturing only
58	Reserved for MFG CLOCK	Not used in normal operation.	56	Reserved for MFG DATA	Not used in normal operation.
		Pins should be left N/C in platform Socket.			Pins should be left N/C in platform Socket.
59	Module Key M		57	GND	Ground
60	Module Key M				
61	Module Key M				
62	Module Key M	Module Key			
63	Module Key M	Module Key			
64	Module Key M				
65	Module Key M				
66	Module Key M				
67	N/C	No connect			
68	SUSCLK(32KHz)	32.768 kHz clock supply input that is provided by the platform			
00	(I)(0/3.3V)	chipset to reduce power and cost for the module.			
69	N/C	PEDET (NC-PCIe)			
70	3.3V	3.3V source			
71	GND	Ground			
72	3.3V	3.3V source			
73	GND	Ground			
	3.3V	3.3V source			
74	3.3V	5.5V Source			

C3-CT-X44E-2.1A

75

GND

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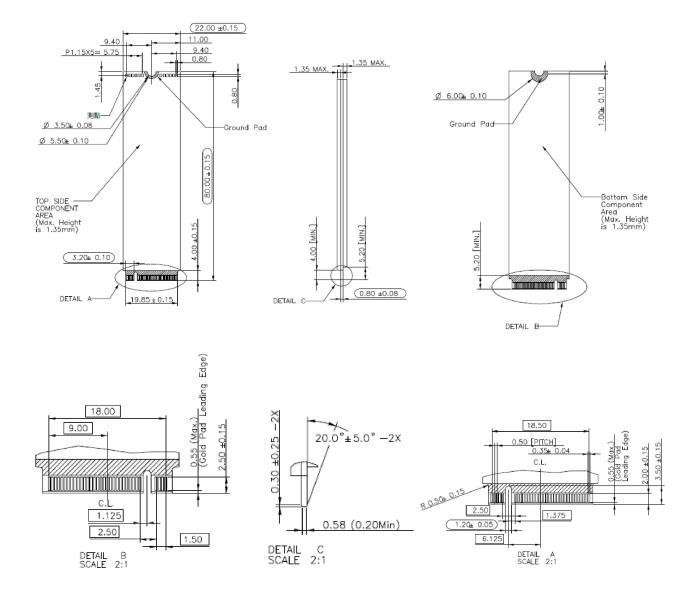
Ground



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Physical Dimensions

Physical Product Dimension : 80.00mm (L) x 22mm (W) x 1.20mm (H)



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