

C3-CT-X44E-1.1A

Centon OEM SSD Commercial, TLC, PCIe 4.0 x4, NVMe 1.3, M.2-2280, 1000GB



*Image may not represent actual product

General Specifications

Pin Count	67 pin (M Key)
Form Factor	M.2 (80mm)
Unformatted Capacity	1000GB
Cache	Uncontrolled

Default Format	Unformatted
Voltage	3.3V
Interface	PCIe 4.0 x4, NVMe 1.3
Warranty	1 Year

Endurance/Power/Performance

Max Read Speed*	4950 MB/s
Max Write Speed*	4300 MB/s
Seq. Read Speed**	4950 MB/s
Seq. Write Speed**	4350 MB/s
4k Random Read***	600000 IOPs
4k Random Write***	550000 IOPs
Endurance (TBW)	

Active Power	6300 mW
Idle Power	20 mW
Sleep Power	2 mW
Shock Tolerance	1500G(.5ms duration, half sine wave)
Vibration Tolerance	20G(Peak,80-2000Hz)
MTBF	1,700,000 Hrs

NAND Specifications

NAND Manufacturer	NOT CONTROLLED
NAND Part Number	NOT CONTROLLED
NAND Type	TLC
NAND Geometry	3D

NAND Config.	NOT CONTROLLED
NAND Quantity	NOT CONTROLLED
NAND Package	NOT CONTROLLED
NAND Technology	Dual Plane

*Maximum speeds are determined using ATTO Disk Benchmark
**Maximum Sequential speeds measured using HD Tune Pro 5.75
***Maximum I/O performance is measured using IOMeter 2010, 4K bytes Random

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For more information visit centon.com, email RFQ@centon.com or call toll-free: 800-234-9292

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Environment

Operating Temp	Commercial (0 to 70 C)	Storage Temp	Storage (-40 to +85 C)
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Controller Specifications

Controller Mfg.	Phison
Controller PN	PS5016-E16
Wear Level Static	Enabled
Wear Level Dynamic	Enabled
Power Loss Protection	No

RAID Support	Yes
SMART Support	Yes
TRIM Support	Yes
ECC	LDPC Gen4 + RAID
Data Encryption	AES 256-bit & Pyrite

Certifications

ROHS	Yes
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Pin Out Diagram

	Pin Ass	ignment and Description			
Pin No.	PCle Pin	Description	Pin No.	PCle Pin	Description
1	GND	CONFIG_3 = GND	30	N/C	No connect
2	3.3V	3.3V source	31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
3	GND	Ground	32	N/C	No connect
4	3.3V	3.3V source	33	GND	Ground
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec	34	N/C	No connect
6	N/C	No connect	35	PERn1	PCIe RX Differential signaldefined by the PCI Express M.2 spec
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec	36	N/C	No connect
8	N/C	No connect	37	PERp1	PCIe RX Differential signaldefined by the PCI Express M.2 spec
9	GND	Ground	38	N/C	No connect
		Open drain, active low signal. These signals are used to allow the addn	39	GND	Ground
10	LED1#	card to provide status indicators via LED devices that will be provided by	40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pullup on platform
		the system.	41	PETn0	PCIe TX Differential signaldefined by the PCI Express M.2 spec
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec	42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pullup on platform.
12	3.3V	3.3V source	43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec		respo	Alert notification to master; Open Drain with pullup on platform;
14	3.3V	3.3V source	44	ALERT#(O) (0/1.8V)	Active low.
15	GND	Ground	45	GND	Ground
16	3.3V	3.3V source	45	N/C	No connect
17	PETn2		47	PERn0	
		PCIe TX Differential signal defined by the PCI Express M.2 spec			PCIe RX Differential signaldefined by the PCI Express M.2 spec
18	3.3V	3.3V source	48	N/C	No connect
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec	49	PERp0	PCIe RX Differential signaldefined by the PCI Express M.2 spec
20	N/C	No connect	50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the cardas defined by the PCIe Min
21	GND	Ground			CEM specification.
22	N/C	No connect	51	GND	Ground
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec	52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the F
24	N/C	No connect			Mini CEM specification; Also used by L1 PM Substates.
25	PERp2	PCIe RX Differential signal defined by the PCExpress M.2 spec	53	REFCLKn	PCIe Reference Clock signals (100 MHz)
26	N/C	No connect			defined by the PCI Express M.2 spec.
27	GND	Ground	54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake.
28	N/C	No connect			Open Drain with pull up on platform;Active Low.
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec	55	REFCLKp	PCIe Reference Clock signals (100 MHz)
		Manufacturing Clock line. Used for SSD manufacturing only.			defined by the PCI Express M.2 spec.
58	Reserved for MFG CLOCK	Not used in normal operation.		Reserved for	Manufacturing Data line. Used for SSD manufacturing only
		Pins should be left N/C in platform Socket.	56 MFG DA	MFG DATA	Not used in normal operation.
59	Module Key M				Pins should be left N/C in platform Socket.
60	Module Key M		57	GND	Ground
61	Module Key M				
62	Module Key M				
63	Module Key M	Module Key			
64	Module Key M	-			
65	Module Key M				
66	Module Key M				
67	N/C	No connect			
07					
68	SUSCLK(32KHz) (I)(0/3.3V)	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module.			
69	N/C	PEDET (NC-PCIe)			
70	3.3V	3.3V source			
71	GND	Ground			

72

73

74

75

3.3V

GND

GND

3.3V source

3.3V source

Ground

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Physical Dimensions

Physical Product Dimension: 80.00mm (L) x 22mm (W) x 1.20mm (H)

