# CY2HH8110

# 1.5V 1:10 HSTL Fanout Buffer

## Features

- **DC to 150-MHz operation**
- **1.5V power supply**
- **One single-ended HSTL input**
- **Ten single-ended Class II HSTL outputs**
- **Less than 1.9% Duty Cycle distortion**
- **Balanced 16-mA output drive**
- **Output Enable/Disable**
- **Low output-output skew**
- **Operating temperature range: 0°C to +85°C**
- **32-pin TQFP package**

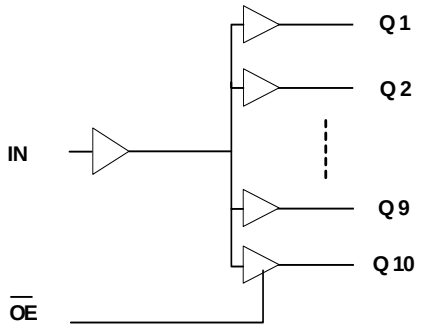
## Description

The CY2HH8110 is a low-voltage HSTL fanout buffer designed for data communications, clock management, and specialty memory applications.

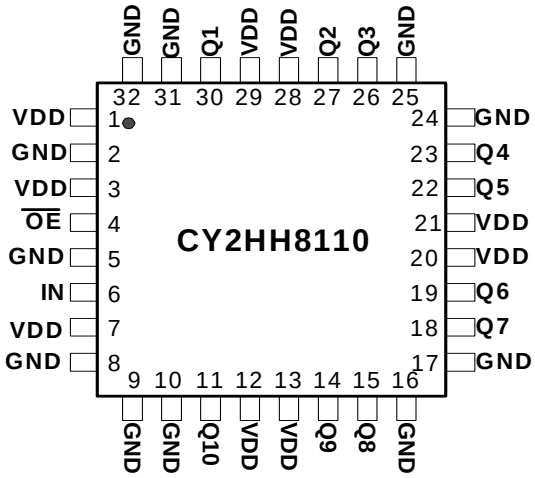
The class II HSTL outputs are balanced Push-Pull in design capable of delivering 16 mA into 10 pF load. This class allows both source series termination and symmetrically double parallel termination.

The CY2HH8110 low-output duty cycle distortion makes it suitable for Double Data Rate (DDR) applications.

**Block Diagram**




**Pin Configuration**



## Pin Description[1]

| Pin | Name | I/O | Type | Description |
|---|---|---|---|---|
| 6 | IN | I | HSTL | **HSTL reference clock input** |
| 30, 27, 26, 23, 22, 19, 18, 15, 14, 11 | Q(1:10) | O | HSTL | **HSTL clock outputs** |
| 4 | OE | I, PD | LVCMOS | **Output enable/disable input**. When held LOW, outputs are enabled. When set HIGH, all outputs are disabled LOW. |
| 1, 3, 7, 12, 13, 20, 21, 28, 29 | VDD | Supply | VDD | **1.5V power supply**[2] |
| 2, 5, 8, 9, 10, 16, 17, 24, 25, 31, 32 | GND | Supply | Ground | **Common ground** |

**Notes:**

1. PD = Internal pull down.
2. A 0.1-uF bypass capacitor should be placed as close as possible to each positive power pin (< 0.2”). If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance of the trace.

## Absolute Maximum Conditions

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | | –0.5 | 2.5 | V |
| $V_{DD}$ | DC Operating Voltage | Functional | 1.35 | 1.65 | V |
| $V_{IN}$ | DC Input Voltage | Relative to $V_{SS}$, with or $V_{DD}$ applied | -0.5 | $V_{DD}$ + 0.5 | V |
| $V_{OUT}$ | DC Output Voltage | Relative to $V_{SS}$ | –0.5 | $V_{DD}$ + 0.5 | V |
| $V_{TT}$ | Output termination Voltage | | | $V_{DD} \div 2$ | V |
| LU | Latch Up Immunity | Functional | 200 | | mA |
| $R_{PS}$ | Power Supply Ripple | Ripple Frequency < 100 kHz | | 150 | mVp-p |
| $T_S$ | Temperature, Storage | Non-functional | –65 | +150 | °C |
| $T_A$ | Temperature, Operating Ambient | Functional | 0 | +85 | °C |
| $T_J$ | Temperature, Junction | Functional | | +150 | °C |
| $Ø_{JC}$ | Dissipation, Junction to Case | Functional | | 42 | °C/W |
| $Ø_{JA}$ | Dissipation, Junction to Ambient | Functional | | 105 | °C/W |
| $ESD_H$ | ESD Protection (Human Body Model) | | 1600 | | V |
| FIT | Failure in Time | Manufacturing test | 10 | | ppm |

**Multiple Supplies**: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

## DC Electrical Specifications ($V_{DD}$ = 1.5V ± 8%, $T_A$ = 0°C to +85°C)

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Voltage, Low | HSTL input, $V_{REF}$ = 0.75V | –0.30 | – | 0.65 | V |
| $V_{IH}$ | Input Voltage, High | | 0.85 | – | 1.80 | V |
| $V_{IL}$ | Input Voltage, Low | OE# input | -0.30 | – | 0.3 * $V_{DD}$ | V |
| $V_{IH}$ | Input Voltage, High | | 0.7 * $V_{DD}$ | – | $V_{DD}$ + 0.3 | V |
| $V_{OL}$ | Output Voltage, Low[3] | $I_{OL}$ = 16 mA | -0.3 | – | 0.4 | V |
| $V_{OH}$ | Output Voltage, High[3] | $I_{OH}$ = –16 mA | 1.0 | – | $V_{DD}$ + 0.3 | V |
| $I_{IL}$ | Input Current, Low[4] | $V_{IL}$ = $V_{SS}$ | – | – | –10 | µA |
| $I_{IH}$ | Input Current, High[4] | $V_{IH}$ = $V_{DD}$ | – | – | 100 | µA |
| $I_{DDQ}$ | Quiescent Supply Current | $V_{IN}$ = 0V, outputs disabled | – | – | 1 | mA |
| $I_{DD}$ | Dynamic Supply Current | Outputs loaded @ 62.5 MHz | – | 215 | 250 | mA |
| $C_{IN}$ | Input Pin Capacitance | | – | – | 6 | pF |
| $C_{OUT}$ | Output Pin Capacitance | | – | 4.5 | 6 | pF |
| $Z_{OUT}$ | Output Impedance | | – | 25 | – | Ω |

## AC Electrical Specifications ($V_{DD}$ = 1.5V ± 8%, $T_A$ = 0°C to +85°C) [5]

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{in}$ | Input Frequency | | – | – | 150 | MHz |
| $V_{IL}$(AC) | AC Input HIGH Voltage | $V_{REF}$ =$V_{DD}$/2, Internal Voltage Reference | 0.95 | – | | V |
| $V_{IH}$(AC) | AC Input LOW Voltage | | – | – | 0.55 | V |
| $t_r$ , $t_f$ | Output rise/fall time[6] | 20% to 80% | 0.3 | – | 1.5 | ns |
| DC | Output duty cycle | Fout < 100 MHz | 48 | – | 52 | % |
| | | Fout > 100 MHz | 45 | – | 55 | |

**Notes:**

3. Driving 50Ω series terminated or symmetrically double parallel terminated transmission line to a termination voltage of $V_{TT}$.
4. Inputs have pull-down resistors that affect the input current.
5. AC characteristics apply for series or parallel output termination to $V_{TT}$. Parameters are guaranteed by characterization and are not 100% tested.
6. tr/tf times are faster with parallel terminated loads.

## AC Electrical Specifications ($V_{DD}$ = 1.5V ± 8%, $T_A$ = 0°C to +85°C) (continued)[5]

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| tjit_DCD | Output Duty Cycle Distortion | Measure Jitter delay between input and output at $V_{DD}/2$ @ $f_{REF}$ = 62.5 MHz | – | – | \|300\| | ps |
| | | DCD @ $f_{REF}$ = 62.5 MHz | – | – | \|1.9\| | % |
| $t_{sk(O)}$ | Output-to-Output Skew | | – | – | 200 | ps |
| tsk(pp) | Part-to-Part Skew | | – | – | 2 | ns |
| $t_{PLH}$ | Propagation Delay, Low to High | | – | – | 7 | ns |
| $t_{PHL}$ | Propagation Delay, High to Low | | – | – | 7 | ns |
| $t_{Qoff}$ | Output Disable Time | | – | – | 7 | ns |
| $t_{Qon}$ | Output Enable Time | | – | – | 7 | ns |
| $t_{JIT(CC)}$ | Cycle-to-Cycle Jitter, Deterministic jitter | | – | 10 | 50 | ps |

## Parameter Measurement Information

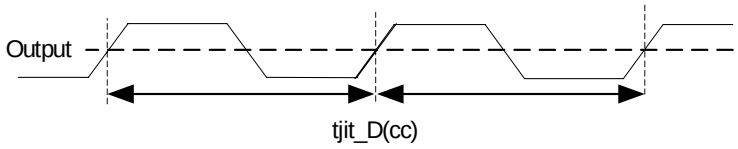



**Figure 1. Cycle-to-Cycle Jitter**

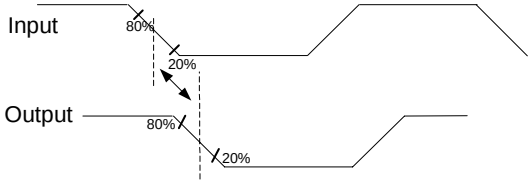



**Figure 2. Propagation Delay from Input Reference to Output *n***

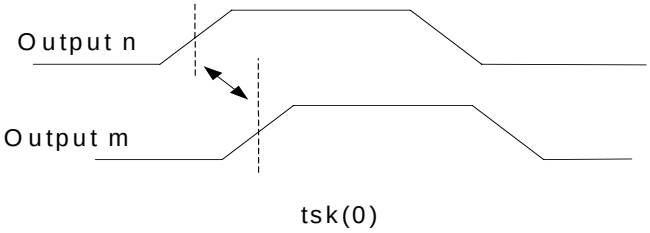



**Figure 3. Output to Output Skew**

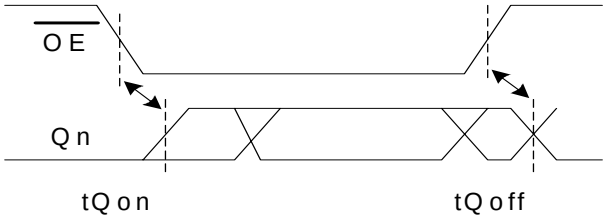



**Figure 4. Output Enable/Disable Time**

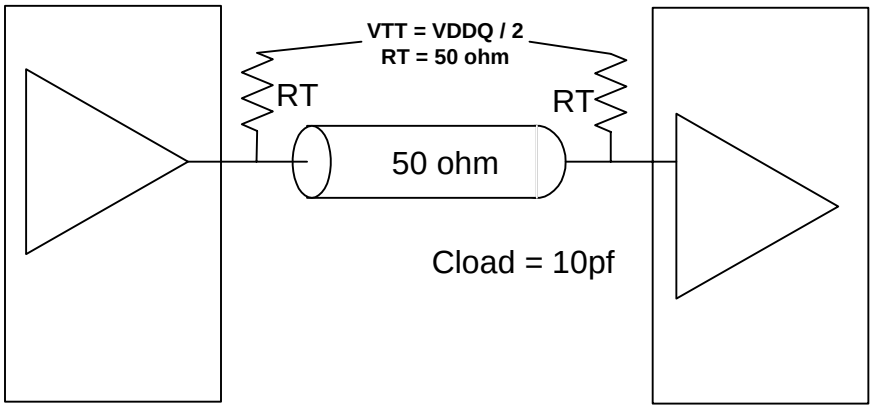



**Figure 5. An Example HSTL Symmetrically Double Parallel Terminated Output Load | and CLASS II HSTL AC Test Load** [7,8]

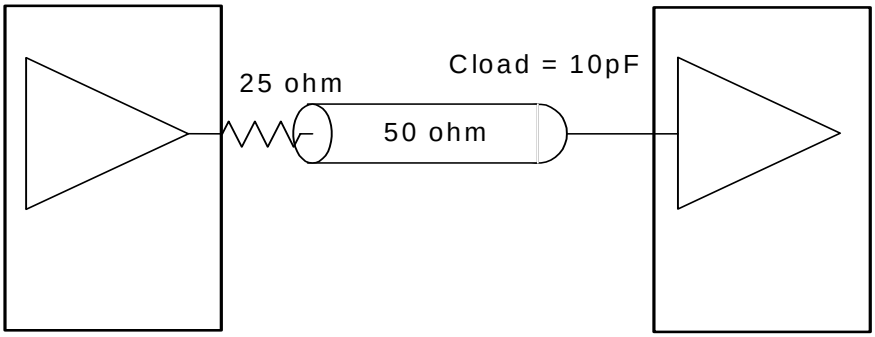



**Figure 6. An Example HSTL Source Series Terminated Output Load**[7,8]

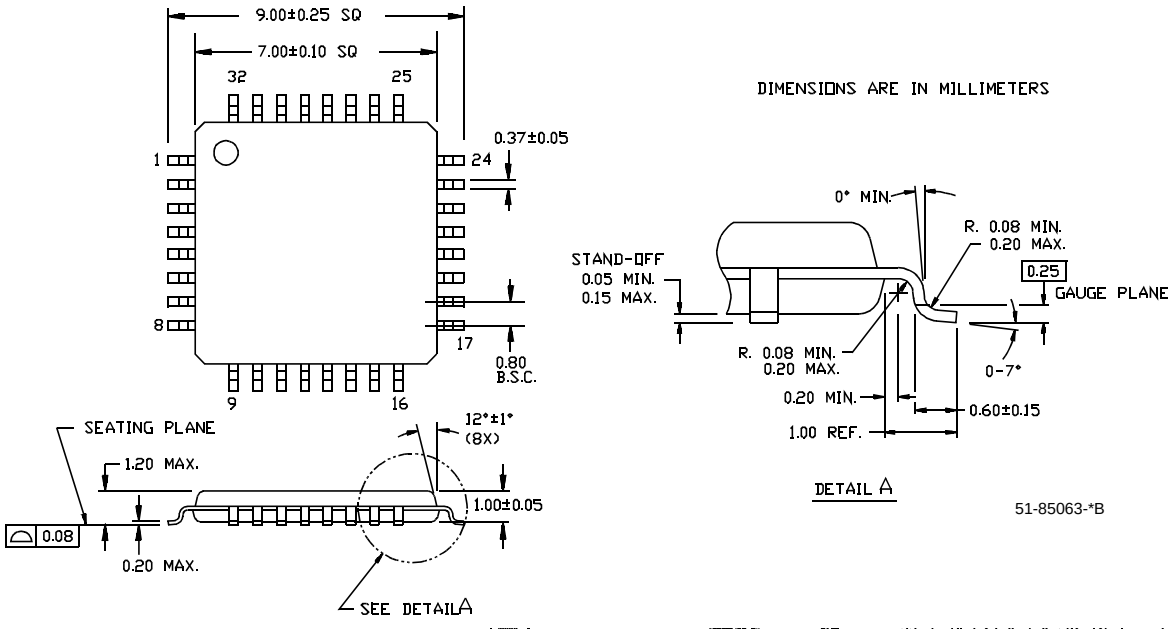
## Ordering Information

| Part Number | Package Type | Product Flow |
|---|---|---|
| CY2HH8110AC | 32-pin TQFP | Commercial, 0°C to +85°C |
| CY2HH8110ACT | 32-pin TQFP – Tape and Reel | |

**Notes:**
7. HSTL to HSTL input.
8. Cload includes probe and test board capacitance.

## Package Drawing and Dimensions

**32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.0mm A32**



## Document History Page

| Document Title:CY2HH8110 1.5V 1:10 HSTL Fanout Buffer<br>Document Number: 38-07556 | | | | |
|---|---|---|---|---|
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| ** | 128398 | 08/04/03 | RGL | New Data Sheet |