OvationONS™ II
Wired Laser Navigation System on Chip

Features

■ Programmable Blocks
  ❏ Highly integrated mouse-on-a-chip with PSoC® microcontroller unit (MCU)
  ❏ 16K Byte Flash memory
  ❏ 2K Byte SRAM memory
  ❏ Internal 24, 12, or 6 MHz main oscillator
  ❏ Internal 32 kHz low speed oscillator
  ❏ 16 bit data report enables high speed and high resolution

■ Tracking Performance
  ❏ Selectable resolution of 400, 800, or 1600 cpi, independent of speed
  ❏ High speed with high accuracy tracking
  ❏ Tracking speed 30 in/s
  ❏ Acceleration up to 20G

■ Peripheral Interface
  ❏ Integrated full speed USB for wired applications
  ❏ SPI master for interface to external functions
  ❏ Up to 28 general purpose I/O pins
  ❏ I²C

■ Power
  ❏ Internal power system enables operation from 5V USB or 2.7 to 3.6V external supply
  ❏ Self-adjusting power saving modes

■ On-Chip Laser
  ❏ Vertical Cavity Surface Emitting Laser (VCSEL) integrated within the sensor package
  ❏ No calibration or alignment needed
  ❏ ESD immunity: 2000V (human body model)
  ❏ Wavelength: 850 nm typical (840 nm minimum, 870 nm maximum)
  ❏ IEC 60825-1 Class 1 Safety: built-in eye-safe fault tolerant laser drive circuitry

■ Snap On Lens
  ❏ Molded Optic: Self aligning snap on molded lens
  ❏ 6 mm distance between the PCB and tracking surface

Description

The CYONS2000 is a member of Cypress Semiconductor's second generation laser navigation SoC family of products. Powered by the high speed and high precision OptiCheck™ technology, along with the world leading PSoC technology, this family integrates the sensor, USB, and MCU functions into one chip. Bundled with the Vertical Cavity Surface Emitting Laser (VCSEL) into one package, the combination forms the market's first true Mouse-on-a-Chip solution.
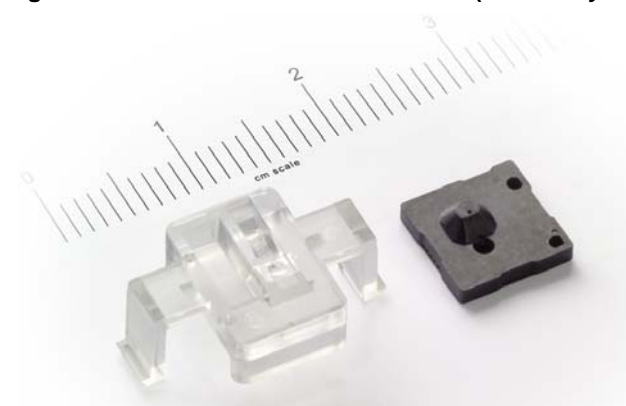
The CYONS2000 is the version that is designed for general purpose wired mouse applications. Enabled by the Cypress 0.13 micron mixed signal process technology, the device integrates the OptiCheck sensor with full speed USB into a single silicon chip that enables seamless communication between sensor and MCU/Full Speed USB. The sensor provides the best translation of precise hand motion into cursor motion on the PC.

This highly integrated solution is programmable. It provides mouse suppliers the ease of use to design a single PCB system and customize their product. With the VCSEL integrated in the same package, designers do not need to calibrate the laser power during the manufacturing process. This greatly increases production throughput and reduces manufacturing costs.

The innovative technology of OvationONS™ II provides high precision, high speed motion tracking, and low power consumption. Designers can select from a family of integration options, ranging from low power to high performance, to target different types of wired and wireless design applications.

The CYONS2000 solutions have a small form factor. Along with the lens, each package forms a complete and compact laser tracking system. This data sheet describes the detailed technology capabilities of the CYONS2000.

Figure 1. CYONS2000/CYONSLENS2000 (2-Piece System)

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OvationONS II Family Performance Table

Parameter	CYONS2000	CYONS2001	CYONS2100	CYONS2101	CYONS2110	Unit
Variable resolution	400, 800, 1600	400, 800, 1600	400–3200	400–3200	400–3200	cpi
Maximum speed	30	30	75	75	75	in/s
Maximum acceleration	20	20	30	30	30	G
Integrated MCU	Yes	Yes	Yes	Yes	Yes	
CapSense	No	No	No	No	26 inputs	
Flash	16K	16K	32K	32K	32K	Byte
SRAM	2K	2K	2K	2K	2K	Byte
Interfaces	Full speed USB 4 wire SPI up to 28 GPIOs	4 wire SPI up to 28 GPIOs	Full speed USB 4 wire SPI up to 28 GPIO	4 wire SPI up to 28 GPIOs	Full speed USB 4 wire SPI up to 28 GPIOs	
Battery supply voltage	NA	0.8 - 3.6	NA	0.8 to 3.6	0.8 to 3.6	V
USB supply voltage	4.25 to 5.25	NA	4.25 to 5.25	NA	4.25 to 5.25	V
External supply voltage	2.7 - 3.6	2.7 - 3.6	2.7 - 3.6	2.7 - 3.6	2.7 - 3.6	V
Zero motion	1	1	1	1	1	count

OvationONS II Family Applications

- Wired and wireless laser mice
  - Gaming, graphic design, desktop, and mobile mice
- Optical trackballs
- Battery powered devices
- Motion sensing applications

OvationONS II Family Functional Description

The OvationONS™ II family is a two-piece laser navigation system on chip (SoC) kit containing the integrated IC package and the molded lens.

The 2 kV ESD rated IC package integrates the VCSEL and laser sensor SoC. Depending on the product selected, the SoC includes a micro controller unit (MCU), Flash, SRAM, internal oscillator, CapSense system, battery boost regulator, power regulator, and full speed USB.

The molded lens collimates the VCSEL beam and images the light scattered from the tracking surface onto the sensor portion of the laser detector. The lens has features for registration to the package and easily snaps onto the PC board.

At the heart of the system is the OptiCheck laser navigation engine. It supports all functions required for tracking, including laser power control, resolution control, and self-adjusting power reduction, which reduces power consumption when motion stops. The laser output power is pre-calibrated to meet the eye safety requirements of IEC 60825 Class 1.

The navigation engine is accessed and controlled by an integrated PSoC-based MCU. The interface between the two blocks is through a system bus and a collection of navigation engine interrupts. Full details are available in the Technical Reference Manual.

In addition to controlling the navigation engine, the PSoC MCU also serves as the main application processor. Based on Cypress's M8C architecture, the PSoC supports a rich instruction set, multiple processor speeds, and flexible general purpose I/Os (GPIOs). Its internal oscillator requires no external crystal. On-chip Flash and RAM enable entire navigation systems to be implemented with the single SoC.

The OvationONS II Family supports a wide range of powering options. Internal regulators minimize the need for external circuitry. Depending on the product selected, the device can be powered from USB's 5V supply, from a single battery, from dual batteries, or from an external supply. The integrated PSoC controls the configuration and use of the power blocks.

Wired sensors include integrated full speed USB. As with the navigation engine and power system, the USB block is controlled by the integrated PSoC.

All sensors support a 4-wire SPI interface. A typical use of the SPI interface is to provide access to a radio for wireless applications.

The CYONS2110 device also supports CapSense functions, enabling additional features and differentiation in end products.

All features of the OvationONS™ II family are configured using Cypress's PSoC Designer software, enabling fast application development and time to market.

The OvationONS™ II family block diagram is shown in Figure 2. It shows a true System-on-a-Chip solution that enables design cycle reductions along with savings on manufacturing, PCB area, and component inventory management. The packaged solution delivers a fully integrated system that demonstrates tracking performance with efficient power consumption.

Figure 2. Block Diagram
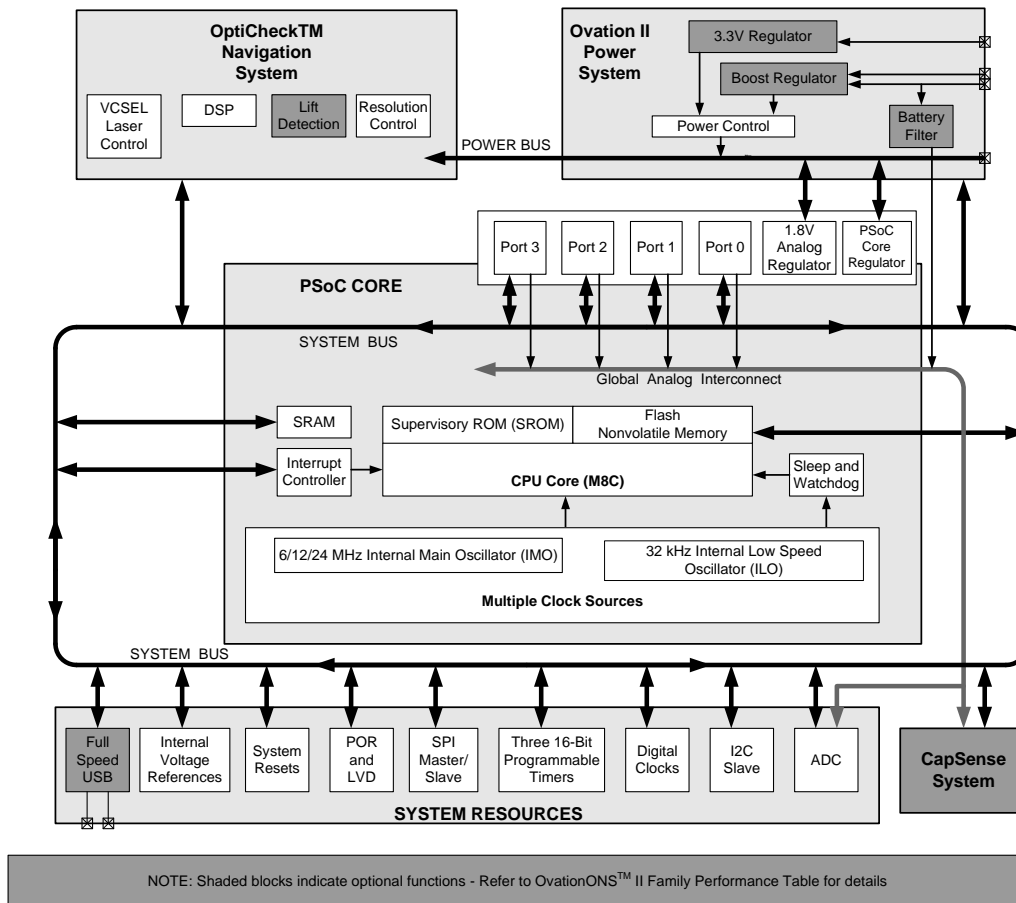
Pin Description

This section describes, lists, and illustrates the CYONS2000 device pins and pinout configurations. The CYONS2000 is available in a 42-pin QFN package.

Table 1. CYONS2000 Pin Description

Pin[1]	Name	Digital	Analog	Description
1	XRES	I		Active high external reset with internal pull down
2	DVSS	Power	Power	Digital ground
3	DNU			Do not use
4	DVSS	Power	Power	Digital ground
5	DVDD	Power	Power	Digital supply voltage and regulated output (see Power Supply Connections on page 11)
6	VREGD	Power	Power	Digital VREG
7	AVDD	Power	Power	Analog supply voltage
8	VREGA	Power	Power	Analog VREG
9	P2[7]	I/O	I	GPIO
10	P1[5]	IOHR	I	SPI MISO, I2C_SDA, GPIO
11	P1[3]	IOHR	I	SPI CLK, GPIO
12	P2[3]	I/O	I	GPIO

[+] Feedback

Table 1. CYONS2000 Pin Description (continued)

Pin[1]	Name	Digital	Analog	Description
13	P2[5]	I/O	I	GPIO
14	P1[7]	IOHR	I	SPI SS, I2C_SCL, GPIO
15	P1[1]	IOHR	I	SPI MOSI, ISSP CLK[1], I2C_SCL, GPIO
16	P3[3]	IOHR	I	HCLK (OCD high speed clock output), GPIO
17	P1[0]	I/O	I	ISSP DATA[1], I2C_SDA, GPIO
18	P3[5]	I/O	I	CCLK (OCD CPU clock output), GPIO
19	P1[6]	IOHR	I	GPIO
20	P1[2]	IOHR	I	GPIO
21	P2[2]	I/O	I	GPIO
22	P3[7]	I/O	I	OCDOE (OCD mode direction pin), GPIO
23	P3[1]	I/O	I	OCDO (OCD odd data output), GPIO
24	OCDE	OCD	OCD	OCDE (OCD even data output)
25	AVSS	Power	Power	Analog ground
26	P2[1]	I/O	I	GPIO
27	P2[0]	I/O	I	GPIO
28	P1[4]	IOHR	I	EXT CLK, GPIO
29	P2[4]	I/O	I	GPIO
30	DVSS	Power	Power	Digital ground
31	P2[6]	I/O	I	GPIO
32	P0[0]	I/O	I	GPIO
33	P0[2]	I/O	I	GPIO
34	P0[4]	I/O	I	GPIO
35	P0[6]	I/O	I	GPIO
36	P0[1]	I/O	I	GPIO
37	P0[3]	I/O	I	GPIO
38	P0[5]	I/O	I	GPIO
39	P0[7]	I/O	I	GPIO
40	D-	I/O		USB data
41	D+	I/O		USB data
42	VDD5V	Power	Power	5V power
CP	DVSS	Power	Power	Center pad must be connected to digital ground
Legend: I=Input; O=Output; H=5 mA High Output Drive, R=Regulated Output, OCD = On-Chip-Debug				

Note
1. These are the ISSP pins, which are not High Z at POR (Power On Reset)

Figure 3. Pin Diagram

Pin diagram: CYONS2000 QFN (Top View)

Top pins:
- 42 VDD5V
- 41 D+
- 40 D-
- 39 AI, P0[7]
- 38 AI, P0[5]
- 37 AI, P0[3]
- 36 AI, P0[1]
- 35 AI, P0[6]

Left pins:
- 1 XRES
- 2 DVSS
- 3 DNU
- 4 DVSS
- 5 DVDD
- 6 VREGD
- 7 AVDD
- 8 VREGA
- 9 AI, P2[7]

Right pins:
- 34 AI, P0[4]
- 33 AI, P0[2]
- 32 AI, P0[0]
- 31 AI, P2[6]
- 30 DVSS
- 29 AI, P2[4]
- 28 AI, EXT CLK, P1[4]
- 27 AI, P2[0]
- 26 AI, P2[1]
- 25 AVSS
- 24 OCDE
- 23 AI, OCDO, P3[1]

Bottom pins:
- 10 AI, SPI MISO, P1[5]
- 11 AI, SPI CLK, P1[3]
- 12 AI, P2[3]
- 13 AI, P2[5]
- 14 AI, SPI SS, P1[7]
- 15 AI, SPI MOSI, ISSP CLK, P1[1]
- 16 AI, HCLK, P3[3]
- 17 AI, ISSP DATA, P1[0]
- 18 AI, CCLK, P3[5]
- 19 AI, P1[6]
- 20 AI, P1[2]
- 21 AI, P2[2]
- 22 AI, OCDOE, P3[7]

Microcontroller System

Features

- Powerful Harvard Architecture processor
  - ❒ M8C processor speed up to 24 MHz
  - ❒ Low power at high speed
  - ❒ Interrupt controller
  - ❒ Operating temperature range: +5°C to +45°C

- Flexible on-chip memory
  - ❒ 16k Flash program storage
    50,000 erase and write cycles
  - ❒ 2K bytes SRAM data storage
  - ❒ Partial Flash updates
  - ❒ Flexible protection modes
  - ❒ In-System Serial Programming (ISSP)

- Full speed USB (12 Mbps)
  - ❒ Eight unidirectional endpoints
  - ❒ One bidirectional control endpoint
  - ❒ USB 2.0 compliant
  - ❒ Dedicated 512 byte buffer
  - ❒ Internal 3.3V output regulator

- Complete development tools
  - ❒ Free development tool (PSoC Designer™)
  - ❒ Full featured In-Circuit Emulator and programmer
  - ❒ Full speed emulation
  - ❒ Complex breakpoint structure
  - ❒ 128K trace memory

- Precision programmable clocking
  - ❒ Internal ±5.0% 6, 12, or 24 MHz main oscillator
  - ❒ Internal low speed oscillator at 32 kHz for watchdog and sleep
  - ❒ Support for optional external 32 kHz crystal
  - ❒ 0.25% accuracy for USB with no external crystal

- Programmable pin configurations
  - ❒ 25 mA sink current on all GPIO
  - ❒ Pull Up, High-Z, Open Drain drive modes on all GPIO
  - ❒ CMOS drive mode on ports 0 and 1
  - ❒ Up to 28 analog inputs on GPIO
  - ❒ Configurable inputs on all GPIO
  - ❒ Selectable, regulated Digital I/O on port 1
  - ❒ 3.0V, 20 mA total port 1 source current
  - ❒ 5 mA source current mode on ports 0 and 1
  - ❒ Hot swap capable

- Versatile analog mux
  - ❒ Common internal analog bus
  - ❒ Simultaneous connection of I/O combinations
  - ❒ High PSRR comparator
  - ❒ Low dropout voltage regulator for the analog array

- Additional system resources
  - ❒ SPI Master and SPI Slave
    - • Configurable between 46.9 kHz and 3 MHz
  - ❒ Three 16-bit timers
  - ❒ Watchdog and Sleep timers
  - ❒ Internal voltage reference
  - ❒ Integrated supervisory circuit
  - ❒ Analog to digital converter
  - ❒ I^2C Slave

PSoC Functional Overview

Cypress's PSoC On-Chip Controllers combine dynamic, configurable analog and digital blocks and an 8-bit MCU on a single chip, replacing multiple discrete components while delivering advanced flexibility and functionality. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture enables the creation of customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as illustrated in Figure 2 on page 4, contains: the core, the navigation sensor, the power system, and the system resources (including a full speed USB port). A common, versatile bus enables connection between I/O and the analog system. General purpose I/O (GPIO) is also included. The GPIO provides access to the MCU and analog mux.

The PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. The PSoC core encompasses SRAM for data storage, an interrupt controller, Sleep and Watchdog timers, an IMO (Internal Main Oscillator), and an ILO (Internal Low Speed Oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4 MIPS, 8-bit Harvard architecture microprocessor.

System resources provide additional capability, such as configurable USB and SPI master-slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

The Analog Multiplexer System

The analog mux bus connects to every GPIO pin. Pins are connected to the bus individually or in any combination. Analog signals may be routed to an internal analog-to-digital converter.

Other multiplexer applications include:

■ Chip-wide mux that enables analog input from any I/O pin

■ Crosspoint connection between any I/O pin combinations

Additional System Resources

System resources, some previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource follow:

■ The SPI master/slave module
  ❑ Provides communication over three or four wires
  ❑ Runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).

■ An I^2C slave module

■ Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.

■ An internal reference provides an absolute reference for capacitive sensing.

Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual* for the PSoC device.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at http://www.cypress.com.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs and are available at http://www.cypress.com.

Development Kits

PSoC Development Kits are available online from Cypress at http://www.cypress.com and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at http://www.cypress.com. The training covers a wide variety of topics and skill levels to assist you in your designs.

Cypros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com and refer to CYPros Consultants.

Solutions Library

Visit our growing library of solution focused designs at http://www.cypress.com. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at http://www.cypress.com. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

PSoC Designer Software Subsystems

System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC On-Chip Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called "drivers" and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I^2C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view, the components are called "user modules". User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in the PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer's output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the "Generate Application" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer's Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

Table 2 lists the acronyms used in this document.

Units of Measure

A units of measure table in Table 3 lists the abbreviations used to measure the devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or '0x' are decimal.

Table 2. Acronyms

Acronym	Description	Acronym	Description
AC	Alternating Current	I/O	Input/output
API	Application Programming Interface	LSb	Least-significant Bit
CPU	Central Processing Unit	LVD	Low Voltage Detect
DC	Direct Current	MSb	Most-significant Bit
GPIO	General Purpose I/O	POR	Power On Reset
GUI	Graphical User Interface	PPOR	Precision Power On Reset
ICE	In-circuit Emulator	PSoC	Programmable System-on-chip
ILO	Internal Low Speed Oscillator	SLIMO	Slow IMO
IMO	Internal Main Oscillator	SRAM	Static Random Access Memory

Table 3. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	μW	microwatt
dB	decibel	mA	milliampere
fF	femtofarad	ms	millisecond
Hz	hertz	mV	millivolt
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolt
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
μA	microampere	pp	peak-to-peak
μF	microfarad	ppm	parts per million
μH	microhenry	ps	picosecond
μs	microsecond	sps	samples per second
μV	microvolts	σ	sigma: one standard deviation
μVrms	microvolts root-mean-square	V	volt

Power Supply Connections

Figure 4. Power Connections Block Diagram
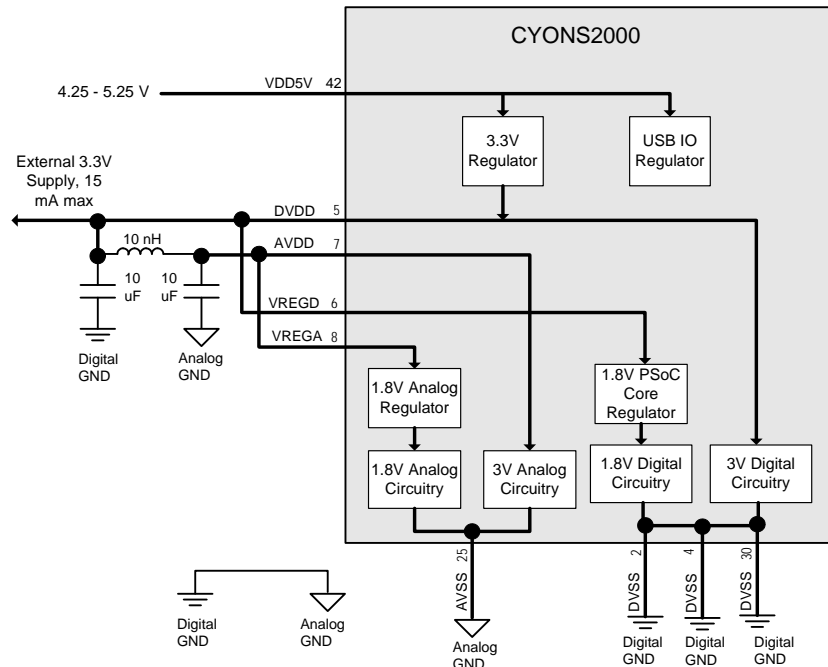
Overview

The CYONS2000 incorporates a powerful and flexible powering system. It can be powered from one of two sources: a 5V supply (typically from the USB VBUS line) or an external 3.3V supply. Additionally, the CYONS2000's internal regulators can supply current to external devices. This section describes the capabilities and usage of the power system. Refer to Figure 4 for a block diagram of the CYONS2000's power system.

Understanding DVDD

DVDD is a unique pin because it serves as either an input or an output. When the device is powered from USB (using the 3.3V Regulator), DVDD acts as an output, providing a 3.3V voltage that can be used to power AVDD, VREGD, VREGA, and external parts. When the device is powered from an external 3.3V supply, DVDD acts as an input only.

AVDD, VREGA, and VREGD

As with DVDD, these signals power the internal circuitry of the device. Unlike DVDD, these are always inputs. They should be connected as shown in Figure 4.

Using USB Power

For most USB applications, the device is powered from the USB VBUS signal. In this case, the 5V VBUS signal should be connected directly to the CYONS2000's VDD5V pin.

Using External Power

The CYONS2000 can also be powered from an external source. In this case, the external 3.3V source should connect to DVDD, and the VDD5V pin should be left unconnected.

Filtering and Grounding

For all designs, it is important to provide proper grounding, and proper isolation between the analog and digital power supplies. The analog and digital grounds should be isolated, except for a single connection point that is placed as close as possible to the device. On the supply side, an L-C filter should be placed between AVDD and DVDD, as shown in Figure 4.

Wired Mouse Application Example

Figure 5 shows an implementation of a wired mouse. For complete details, refer to the CY4631 Reference Design Kit.

Figure 5. Wired Mouse
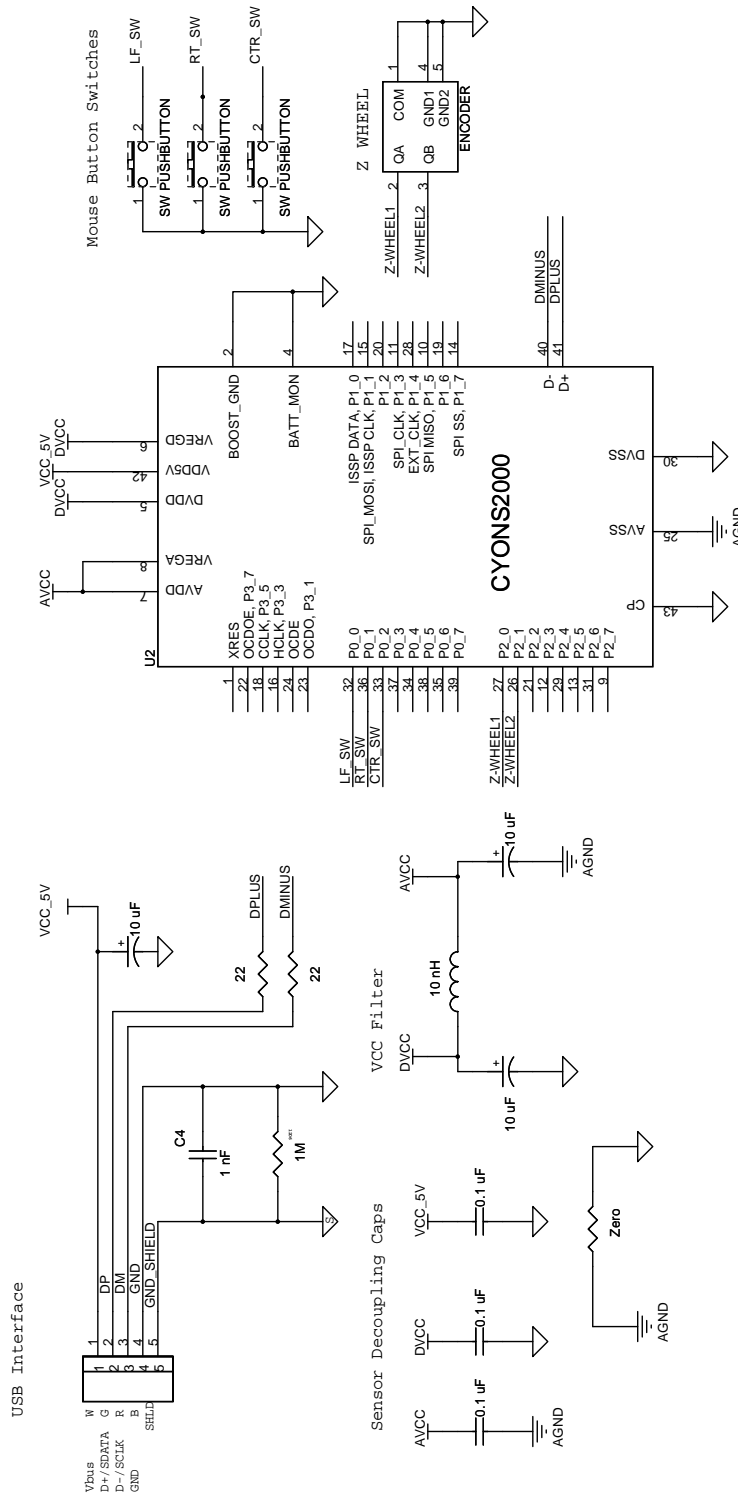
Electrical Specifications

This section presents the DC and AC electrical specifications of the CYONS2000 device. For the most up-to-date electrical specifications, confirm that you have the most recent data sheet by visiting http://www.cypress.com.

Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit	Conditions
Storage Temperature[2]	−40	25	65	°C	Case temperature
Operating Temperature	−15		55	°C	Case temperature
Lead Solder Temperature			260	°C	10 seconds
Supply Voltage, DVDD, AVDD, VREGA, and VREGD relative to DVSS)			3.6	V	
Supply Voltage, VDD5V relative to DVSS			5.5	V	
ESD (Electric Static Discharge)			2	kV	All pins, HBM MIL 883 method 3015
I/O Voltage relative to DVSS	−0.5		DVDD + 0.5	V	GPIO ports 0, 2, and 3
I/O Voltage relative to DVSS			5.5	V	GPIO port 1
Latchup Current			100	mA	
Maximum Current into any GPIO Pin	−25		+50	mA	

Operating Conditions

Parameter	Min	Typ	Max	Unit	Conditions
Operating Temperature	5		45	°C	
Power Supply Voltage VDD5V DVDD, AVDD, VREGD VREGA	 4.35 2.7 1.71		 5.25 3.6 3.6	V	
Power Supply Rise Time	100			µs	
Supply Noise—AVDD (sinusoidal)			25	mV p-p	10 kHz–50 MHz
Supply Noise—VDD, DVDD (sinusoidal)			100	mV p-p	10 kHz–50 MHz
Distance from PCB to Tracking Surface	5.80	6	6.20	mm	See Figure 15 on page 26
PCB Thickness	1.54		1.79	mm	See Figure 15 on page 26

Note
2. High storage temperature reduces flash data retention time. Recommended storage temperature is 25± 25°C. Extended duration above 65°C can degrade reliability.

[+] Feedback

Power Consumption

Introduction

As described earlier, the CYONS2000 has a highly advanced power system, which can be used to develop very low power applications. This section describes and specifies the power consumption performance of the device.

Enabling Low Power Modes

In some cases, designers may want to develop "always-on" applications, with no power-saving modes and consequently no wakeup latency in performance. In other applications, conserving power is crucial, and power saving modes are a firm requirement. The CYONS2000 enables low power modes to be enabled or disabled in firmware, either through register writes or through the application programming interface in Cypress's PSoC Designer development software. The remainder of this section applies to applications requiring power saving modes.

Operating Modes

From a power consumption standpoint, consider these three operating modes:

■ Tracking mode: In this mode, the device is actively tracking on a surface. It is the highest power mode of the device. The current consumption has a slight dependence on speed and surface. The current, however, is independent of resolution.

■ Inactive mode: In this mode, the device is in its lowest power state. In inactive mode, the device cannot sense motion, but a timer is running. This timer can generate an interrupt that can wake the rest of the device and start tracking motion.

■ Sleep modes: In sleep modes, the device self-transitions between tracking mode and inactive mode. The typical use of sleep modes is when the device is at rest, but might still be moved. In Sleep modes, the CYONS2000 stays in inactive mode for a fixed time, then wakes up and checks for motion. If motion is detected, the device fully wakes up and begins tracking. If no motion is detected, the device can go back to Sleep mode.

Power Management Through Sleep Mode Control

Power management for the CYONS2000 consists of setting the parameters that define the sleep modes. The device is equipped with four sets of sleep mode settings, enabling four levels of sleep. By controlling the parameters of these four sleep modes, the designer can tailor the solution to make appropriate tradeoffs between power consumption and wakeup latency.

The transition between sleep modes is under the control of the CYONS2000's DSP - no firmware needs to be written to manage the transition between modes.

Each of the four available sleep modes is defined by three parameters. These parameters are defined as registers that can be controlled by firmware, either through direct register writes or by using the NAV User Module in PSoC Designer.

■ Sleep time: This is the amount of time that the device is in its low power inactive state.

■ Motion threshold: This is the amount of motion that is required to bring the device out of sleep.

■ Sleep mode time: This is the amount of time that the device stays in a particular sleep mode before transitioning to the next lowest sleep mode. Longer sleep times save power but have higher wakeup latency.

Figure 6 on page 14 shows the flowchart for a particular sleep mode, showing how the three parameters affect behavior.

Calculating Power for Sleep Mode

The power consumption in sleep mode can be found by using a duty cycle calculation. The sleep mode current is determined by the tracking mode current, the inactive current, the time required to check for motion (typically 2.9 ms), and the time between check-for-motion events. The expected current consumption is given by the formula

$$I_{SLEEP} = \frac{I_{TRACK} \times 2.9 + I_{INACT} \times T_{SLEEP}}{2.9 + T_{SLEEP}}$$

where I_{SLEEP} is the sleep current, I_{TRACK} is the tracking current, I_{INACT} is the inactive current, and T_{SLEEP} is the time (in ms) in the low power state. As an example, if the tracking current is 8.5 mA, the inactive current is 7.5 µA and the sleep time is 100 ms, then the expected sleep current is 0.25 mA.

Figure 6. Sleep Mode Flowchart

[+] Feedback
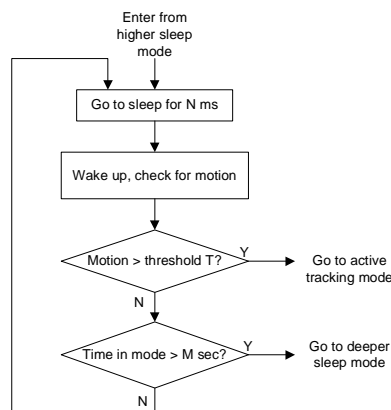
Power Specifications

There are two ways to power the CYONS2000 - external powering and USB powering. Table 4 provides the current consumption values for each mode.

With external powering, a 3V supply is connected to DVDD, AVDD, VREGD, and VREGA, and the internal regulator is turned off. In this case, the current consumption during tracking is I_{TRACK_EXT}, and the consumption during sleep is I_{SLEEP}.

With USB powering, the 5V USB supply is connected to VDD5V, and DVDD, AVDD, VREGD, and VREGA are driven by the internal regulator. Tracking current in this case is specified by I_{TRACK_USB}. Sleep current must include the current consumption of the regulator itself, and is specified by the sum of I_{SLEEP} and I_{REG5V}. Sleep current is achieved by activating "Navigation Sleep Modes" in Cypress' PSoC Designer development environment. Doing so enables the sleep mode progressions described earlier. If sleep modes are not activated, the device current stays at tracking levels, even when the device is not sensing motion.

I_{SB_EXT} is the current in the lowest-power mode of the device. In this mode, the CPU is halted and operation can only be restarted with an external reset at the XRES pin.

For designs using the CYONS2000, low power operation is often only needed to support USB Suspend. Reference code for this is available in the CY4631 Wired Mouse Reference Design Kit.

Table 4. Power Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{TRACK_EXT}	Tracking current into DVDD, AVDD, VREGD, VREGA	3.0V, 25°C, 5 inch/second, 24 MHz IMO, 6 MHz CPU clock, white surface, nominal tracking height		9	12.5	mA
I_{TRACK_USB}	Tracking current into VDD5V	5.25V, 25°C, 5 inch/second, 24 MHz IMO, 6 MHz CPU clock, white surface, nominal tracking height, DVDD, AVDD, VREGD, and VREGA powered by internal regulator		12.5	16	mA
I_{INACT}	Inactive current into DVDD, AVDD, VREGD, VREGA	3.0V, 25°C, CPU in sleep state		7	14	µA
I_{SLEEP}	Sleep current into DVDD, AVDD, VREGD, VREGA	3.0V, 25°C	See previous section for equation			
I_{REG5V}	5V-to-3V regulator current consumption	VDD5V = 5.25V, regulator active		250		µA
I_{SB_EXT}	Shutdown current into DVDD, AVDD, VREGD, VREGA, all blocks off	3.0V, 25°C, 5V supply not present		4	11	µA
I_{SB_USB}	Shutdown current, all blocks off, into VDD5V	5.25V, 25°C, DVDD, AVDD, VREGA, VREGD powered by internal 5V-to-3V regulator in standby mode		80		µA

DC General Purpose I/O Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage range of 2.7V to 3.6V at the DVDD pin, and over the temperature range 5°C ≤ T_A ≤ 45°C. Typical parameters apply to 3.3V at 25°C and are for design guidance only.

Table 5. 2.7V to 3.6V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull up Resistor		4	5.6	8	kΩ
V_{OH1}	High Output Voltage Port 2 or 3 Pins	I_{OH} ≤ 10 μA, maximum of 10 mA source current in all I/Os.	DVDD - 0.2	–	–	V
V_{OH2}	High Output Voltage Port 2 or 3 Pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os.	DVDD - 0.9	–	–	V
V_{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I_{OH} < 10 μA, maximum of 10 mA source current in all I/Os.	DVDD - 0.2	–	–	V
V_{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os.	DVDD - 0.9	–	–	V
V_{OH5}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	I_{OH} < 10 μA, DVDD > 3.1V, maximum of 4 I/Os all sourcing 5 mA.	2.85	3.00	3.30	V
V_{OH6}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	I_{OH} = 5 mA, DVDD > 3.1V, maximum of 20 mA source current in all I/Os.	2.20	–	–	V
V_{OH7}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	I_{OH} < 10 μA, DVDD > 2.7V, maximum of 20 mA source current in all I/Os.	2.35	2.50	2.75	V
V_{OH8}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	I_{OH} = 2 mA, DVDD > 2.7V, maximum of 20 mA source current in all I/Os.	1.90	–	–	V
V_{OH9}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	I_{OH} < 10 μA, DVDD > 2.7V, maximum of 20 mA source current in all I/Os.	1.60	1.80	2.10	V
V_{OH10}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	I_{OH} = 1 mA, DVDD > 2.7V, maximum of 20 mA source current in all I/Os.	1.20	–	–	V
V_{OL}	Low Output Voltage	I_{OL} = 25 mA, DVDD > 3.3V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).	–	–	0.75	V
V_{IL}	Input Low Voltage		–	–	0.80	V
V_{IH}	Input High Voltage		2.00	–		V
V_H	Input Hysteresis Voltage		–	80	–	mV
I_{IL}	Input Leakage (Absolute Value)	Gross tested to 1 μA.	–	0.5	1	μA
C_{PIN}	Pin Capacitance	Temp = 25°C.	0.5	1.7	8	pF

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 6.   DC Analog Mux Bus Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{SW}	Switch Resistance to Common Analog Bus	Pin voltage < 1.8V	–	–	800	Ω
R_{VDD}	Resistance of Initialization Switch to DVSS	Pin voltage < 1.8V	–	–	800	Ω

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 7.   DC Comparator Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{LPC}	Low Power Comparator (LPC) common mode	Maximum voltage limited to DVDD.	0.0	–	1.8	V
I_{LPC}	LPC supply current		–	10	40	μA
V_{OSLPC}	LPC voltage offset		–	2.5	30	mV

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 8.   DC POR and LVD Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{PPOR0} V_{PPOR1} V_{PPOR2} V_{PPOR3}	DVDD Value for PPOR Trip PORLEV[1:0] = 00b, HPOR = 0 PORLEV[1:0] = 00b, HPOR = 1 PORLEV[1:0] = 01b, HPOR = 1 PORLEV[1:0] = 10b, HPOR = 1	DVDD must be greater than or equal to 1.71V during startup, reset from the XRES pin, or reset from watchdog.	1.61 – 	1.66 2.36 2.60 2.82	1.71 2.40 2.65 2.95	V V V V
V_{LVD0} V_{LVD1} V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6}	Vdd Value for LVD Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b		2.40[3] 2.64[4] 2.85[5] 2.95 3.06 1.84 1.75[6]	2.45 2.71 2.92 3.02 3.13 1.90 1.80	2.51 2.78 2.99 3.09 3.20 2.32 1.84	V V V V V V V

Notes
3. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
4. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
5. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
6. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

The CYONS2000 must be properly powered for Flash programming, with DVDD, AVDD, VREGD, and VREGA all held within the specified range. A suitable option for in-circuit programming USB designs is to apply 5V to the VDD5V pin, and use the internal regulator to drive DVDD, AVDD, VREGD, and VREGA. This enables direct connection to Cypress's CY3210-Miniprog. For in-circuit programming of externally-powered designs, the designer must include provisions for supplying DVDD, AVDD, VREGD, and VREGA externally.

Table 9. DC Programming Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IW}	Supply Voltage for Flash Write Operations	V_{IW} applied to DVDD, AVDD, VREGD, and VREGA	2.7	–	3.6	V
I_{DDP}	Supply Current During Programming or Verify		–	5	25	mA
V_{ILP}	Input Low Voltage During Programming or Verify	See DC General Purpose I/O Specifications on page 16.	–	–	V_{IL}	V
V_{IHP}	Input High Voltage During Programming or Verify	See DC General Purpose I/O Specifications on page 16.	V_{IH}	–	–	V
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	Driving internal pull down resistor.	–	–	0.2	mA
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	Driving internal pull down resistor.	–	–	1.5	mA
V_{OLP}	Output Low Voltage During Programming or Verify		–	–	Vss + 0.75	V
V_{OHP}	Output High Voltage During Programming or Verify	DC General Purpose I/O Specifications on page 16. For DVDD > 3V use the value with I_{OH} = 5 mA.	V_{OH}	–	Vdd	V
Flash$_{ENPB}$	Flash Write Endurance	Erase/write cycles by block.	50,000	–	–	Cycles
Flash$_{DR}$	Flash Data Retention	Following maximum flash write cycles at ambient temp of 45°C	5	10	–	Years

DC Characteristics - USB Interface

Table 10. DC USB Characteristics

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ Pull up Resistance	With idle bus	0.900	TBD	1.575	kΩ
Rusba	USB D+ Pull up Resistance	While receiving traffic	1.425	TBD	3.090	kΩ
Vohusb	Static Output High		2.8	TBD	3.6	V
Volusb	Static Output Low			TBD	0.3	V
Vdi	Differential Input Sensitivity		0.2	TBD		V
Vcm	Differential Input Common Mode Range		TBD	TBD	TBD	V
Vse	Single Ended Receiver Threshold		0.8	TBD	2.0	V
Cin	Transceiver Capacitance			TBD	50	pF
Iio	Hi-Z State Data Line Leakage	On D+ or D- line	TBD	TBD	TBD	uA
Rps2	PS/2 Pull up Resistance		3	TBD	7	kΩ
Rext	External USB Series Resistor	In series with each USB pin	21.78	22	22.22	Ω

AC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 11. AC Chip Level Specifications

Parameter	Description	Min	Typ	Max	Unit
F_{MAX}	Maximum Operating Frequency[7]	24			MHz
F_{CPU}	Maximum Processing Frequency[8]	13			MHz
F_{32K1}	Internal Low Speed Oscillator Frequency	19	32	50	kHz
F_{IMO24}	Internal Main Oscillator Stability for 24 MHz ± 5%[9]	22.8	24	25.2	MHz
F_{IMO12}	Internal Main Oscillator Stability for 12 MHz[9]	11.4	12	12.6	MHz
F_{IMO6}	Internal Main Oscillator Stability for 6 MHz[9]	5.7	6.0	6.3	MHz
DC_{IMO}	Duty Cycle of IMO	40	50	60	%
T_{RAMP}	Supply Ramp Time	0	–	–	µs
TXRST	External Reset Pulse Width at Power Up	1			ms
TXRST2	External Reset Pulse Width after Power Up	10			µs
TMOT	Motion Delay from Reset to Valid Tracking Data			30	ms

AC General Purpose I/OI/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges

Table 12. AC GPIO Specs

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO Operating Freq	Strong Mode, Port 1	0	–	12	MHz
T_{RISE_01}	Rise time, ports 0 -1	Strong mode, C_{LOAD} = 50 pF, DVDD = 3.0 - 3.6	10		50	ns
$T_{RISE\_01\_L}$	Rise time, ports 0 -1, low supply	Strong mode, C_{LOAD} = 50 pF, DVDD = 2.7 - 3.0			70	ns
$T_{RISE\_LDO\_3}$	Rise time, port 1, 3V LDO enabled	Strong mode, C_{LOAD} = 50 pF, DVDD > 3.1V			50	ns
$T_{RISE\_LDO\_2.5}$	Rise time, port 1, 2.5 LDO enabled	Strong mode, C_{LOAD} = 50 pF, DVDD > 2.7V	10		70	ns
$T_{RISE\_LDO\_1.8}$	Rise time, port 1, 1.8 LDO enabled	Strong mode, C_{LOAD} = 50 pF, DVDD > 2.7V			100	ns
T_{RISE_23}	Rise time, ports 2 - 3	Strong mode, C_{LOAD} = 50 pF, DVDD = 2.7 - 3.6	15		80	ns
T_{FALL}	Fall time, all ports	Strong mode, C_{LOAD} = 50 pF, DVDD = 3.0 - 3.6	10		50	ns
T_{FALL_L}	Fall time, all ports, low supply	Strong mode, C_{LOAD} = 50 pF, DVDD = 2.7 - 3.0	10		70	ns
$T_{FALL\_LDO\_3}$	Fall time, port 1, 3V LDO enabled	Strong mode, C_{LOAD} = 50 pF, DVDD > 3.1V			50	ns
$T_{FALL\_LDO\_2.5}$	Fall time, port 1, 2.5 LDO enabled	Strong mode, C_{LOAD} = 50 pF, DVDD > 2.7V			70	ns
$T_{FALL\_LDO\_1.8}$	Fall time, port 1, 1.8 LDO enabled	Strong mode, C_{LOAD} = 50 pF, DVDD > 2.7V			80	ns

Notes
7. Vdd = 3.0V and T_J = 85°C, digital clocking functions.
8. Vdd = 3.0V and T_J = 85°C, CPU speed.
9. Trimmed for 3.3V operation using factory trim values.

[+] Feedback

AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 13.   AC External Clock Specifications

Parameter	Description	Min	Typ	Max	Unit
F_{OSCEXT}	Frequency	0.750	–	25.2	MHz
–	High Period	20.6	–	5300	ns
–	Low Period	20.6	–	–	ns
–	Power Up IMO to Switch	150	–	–	μs

AC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14.   AC Analog Mux Bus Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{SW}	Switch Rate	Pin voltage < 1.8V	–	–	6.3	MHz

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 15. AC Programming Specifications

| Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise Time of SCLK		1	–	20	ns
T_{FSCLK}	Fall Time of SCLK		1	–	20	ns
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK		40	–	–	ns
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash Erase Time (Block)		–	–	18	ms
T_{WRITE}	Flash Block Write Time		–	–	25	ms
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	$3.0 \leq DVDD \leq 3.6$	–	–	85	ns

AC SPI Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 16.   AC SPI Master Specifications

Parameter	Description	Min	Typ	Max	Unit
f_{SCLK}	SCK Frequency[10]	–	–	$F_{IMO}/2$	MHz
t_{SETUP}	MISO to SCK Setup Time			150	ns
t_{HOLD}	SCLK to MISO Hold Time	-100			ns
t_{OUT_SU}	MOSI to SCK Setup Time			200	ns
t_{OUT_H}	SCK to MOSI Hold Time	-100			ns

Table 17.   AC SPI Slave Specifications

Parameter	Description	Min	Typ	Max	Unit
f_{SCLK}	SCK Frequency[10]			12	MHz
t_{LOW}	Minimum SCK Low Width			50	ns
t_{HIGH}	Minimum SCK High Width			50	ns
t_{SETUP}	MOSI to SCK Setup Time			25	ns
t_{HOLD}	SCK to MOSI Hold Time			25	ns
t_{OUT_H}	SCK to MISO Hold Time	35			ns
t_{SS_MISO}	SPI_SS to MISO Valid			100	ns
t_{SCLK_MISO}	SCK to MISO Valid			140	ns
t_{SS_HIGH}	Minimum SPI_SS High Width			35	ns
t_{SS_CLK}	Time from SPI_SS Low to First SCK			20	ns
t_{CLK_SS}	Time from Last SCK to SPI_SS High			25	ns

Note
10. Clock frequency is half of clock input to SPI block.

[+] Feedback

Figure 7. SPI Master Timing Diagram, Modes 0 and 2

SPI Master, modes 0 & 2
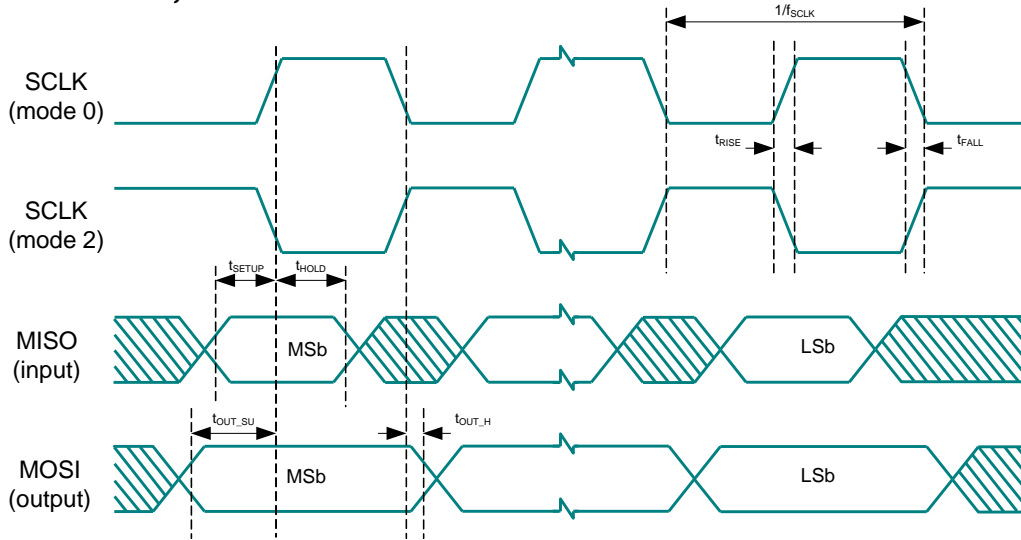
Figure 8. SPI Master Timing Diagram, Modes 1 and 3

SPI Master, modes 1 & 3

[+] Feedback
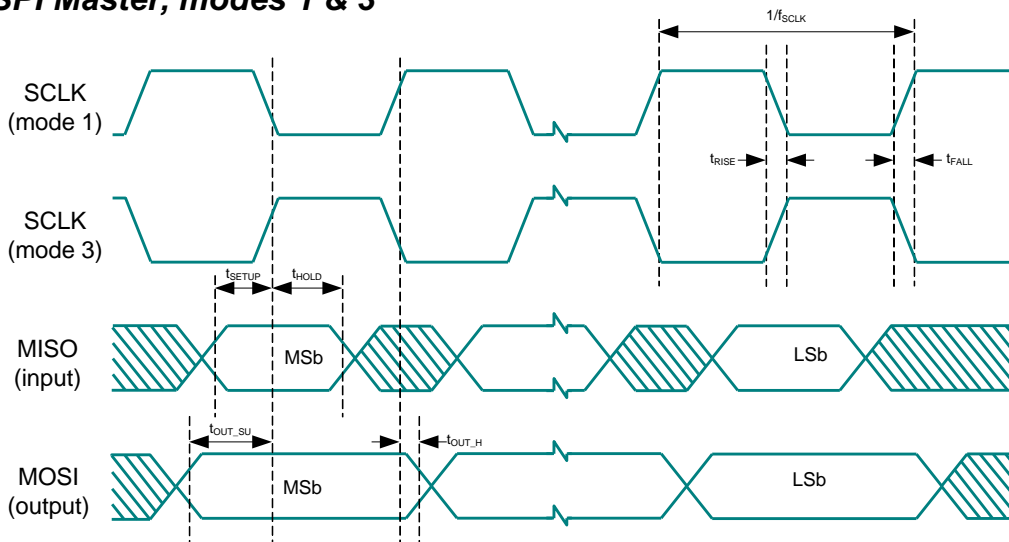
Figure 9. SPI Slave Timing Diagram, Modes 0 and 2

SPI Slave, modes 0 & 2
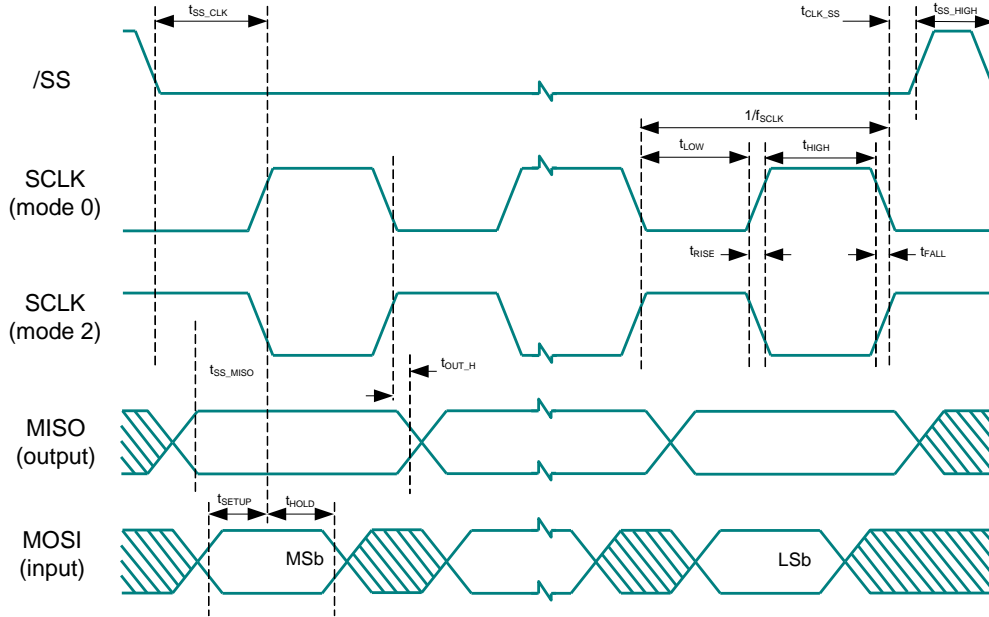
Figure 10. SPI Slave Timing Diagram, Modes 1 and 3

SPI Slave, modes 1 & 3

[+] Feedback
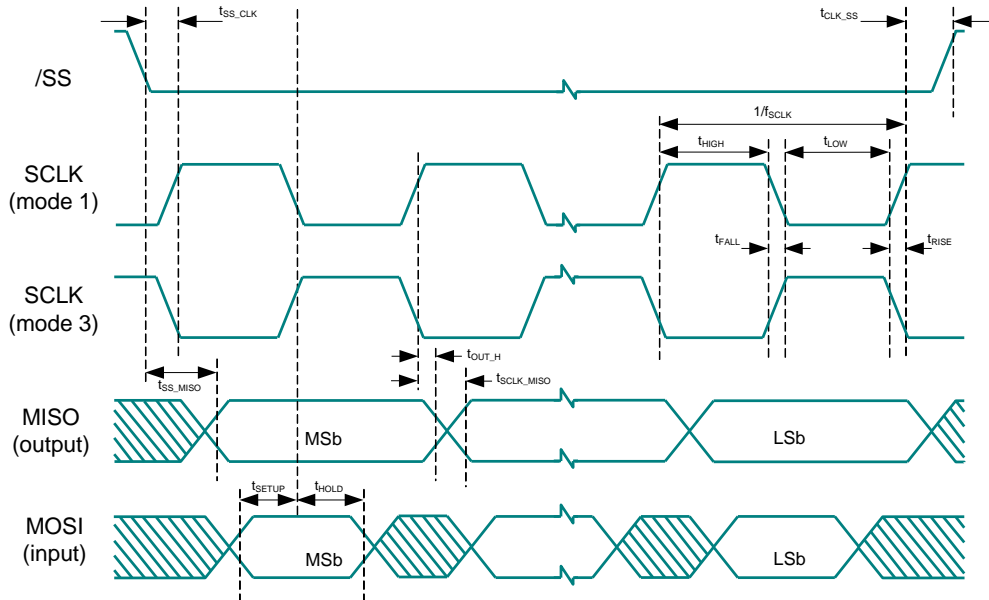
AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{LPC}	Comparator Response Time, 50 mV Overdrive	50 mV overdrive does not include offset voltage			100	ns

AC I^{2}C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. AC Characteristics of the I^{2}C SDA and SCL Pins

Symbol	Description	Conditions	Standard Mode		Fast Mode		Units
			Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency		0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.		4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock		4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock		4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition		4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time		0	–	0	–	µs
$T_{SUDATI2C}$	Data Setup Time		250	–	100[11]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition		4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition		4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.		–	–	0	50	ns

Figure 11. Timing for Fast/Standard Mode on the I^{2}C Bus
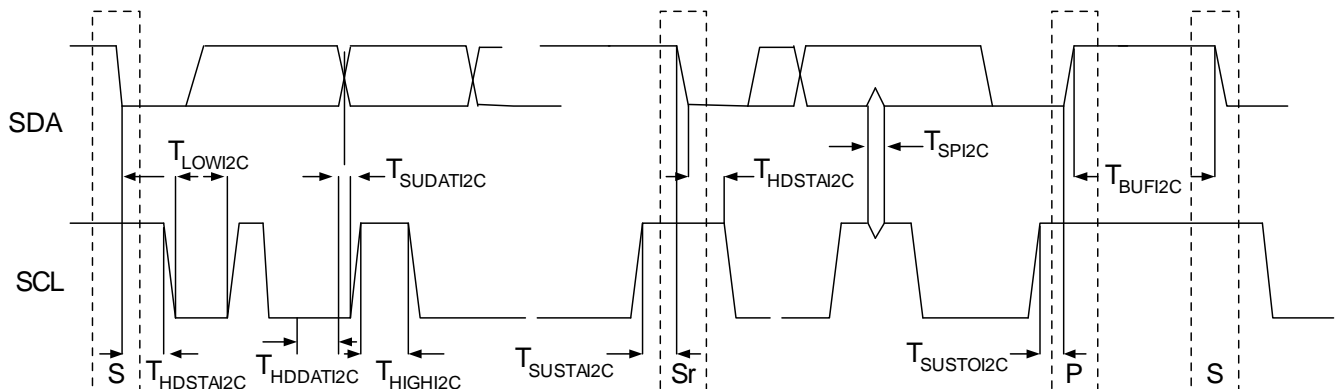
Note
11. A Fast-Mode I2C-bus device can be used in a Standard Mode I2C-bus system, but the requirement $t_{SUDATI2C} \geq 250$ ns must then be met. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

[+] Feedback

AC USB Specifications

Table 20. AC Characteristics – USB Data Timing Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full speed data rate	Average bit rate	12–0.25%	12	12 + 0.25	MHz
Tdjr1	Receiver data jitter tolerance	To next transition	-8	TBD	8	ns
Tdjr2	Receiver data jitter tolerance	To pair transition	-5	TBD	5	ns
Tudj1	Driver differential jitter	To next transition	-3.5	TBD	3.5	ns
Tudj2	Driver differential jitter	To pair transition	-4.0	TBD	4.0	ns
Tfdeop	Source jitter for differential transition	To SE0 transition	-2	TBD	5	ns
Tfeopt	Source SE0 interval of EOP		160	TBD	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	TBD		ns
Tfst	Width of SE0 interval during differential transition			TBD	14	ns

Table 21. AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time	50 pF	4	TBD	20	ns
Tf	Transition fall time	50 pF	4	TBD	20	ns
TR	Rise/fall time matching	0.8V - 2.5V	90.00	TBD	111.11	%
Vcrs	Output signal crossover voltage		1.3	TBD	2.0	V

[+] Feedback

PCB Land Pads and Mechanical Dimensions

Figure 12. Land Pad Architecture and Spacing according to JEDEC MO-220 (52 Pin)
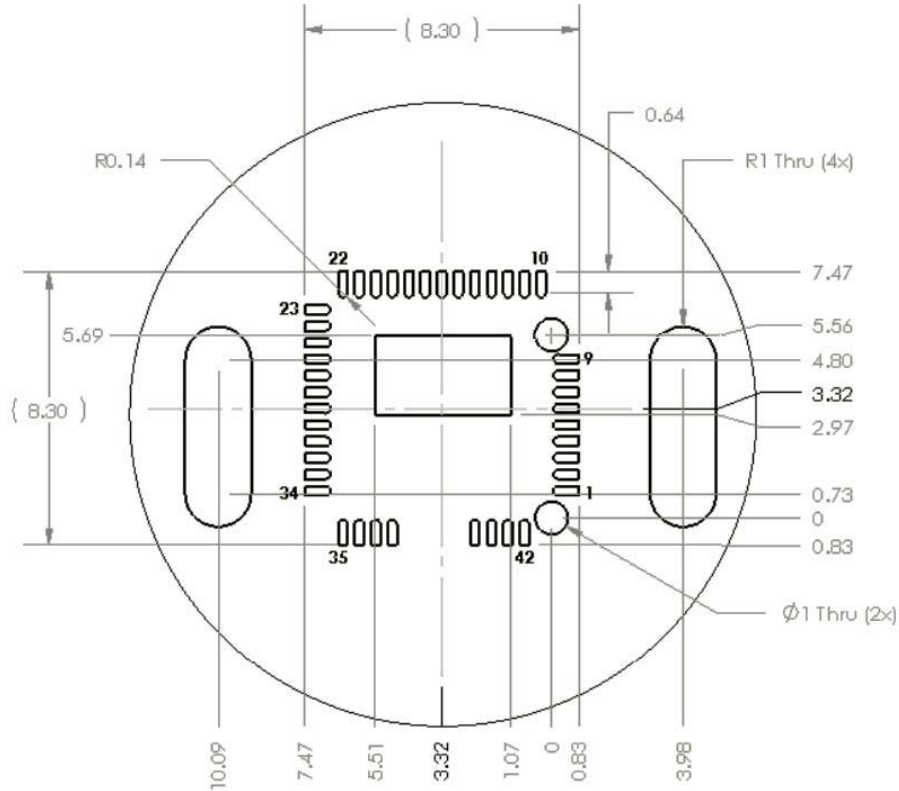
Figure 13. PCB Keep Out Zones
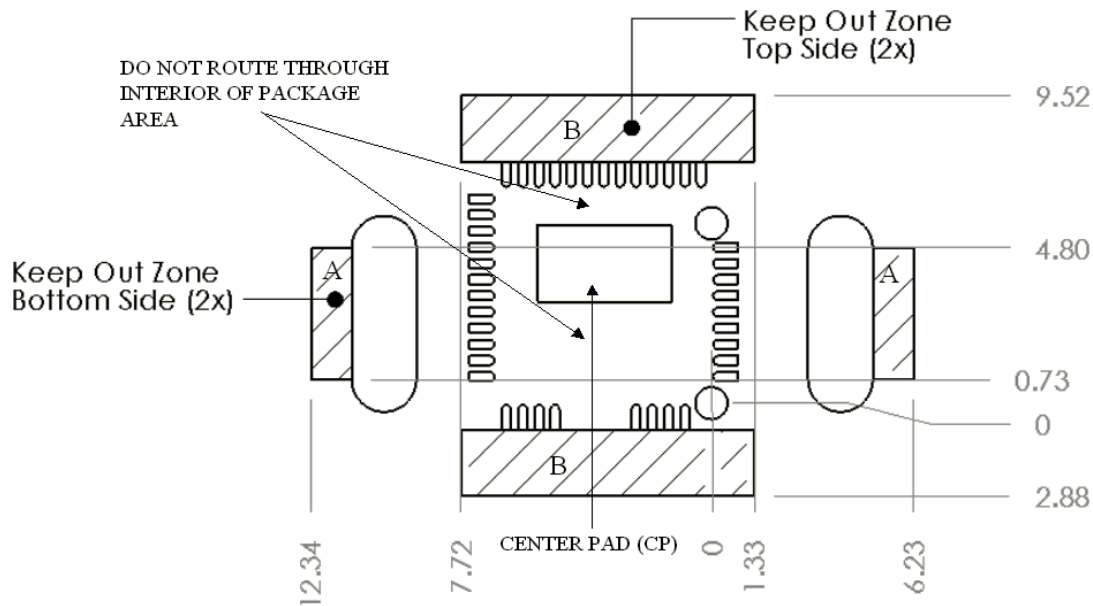
Orientation of Axes

Figure 14 describes the relationship between the package and the x/y axes when using the API provided by Cypress' PSoC Designer software. Users should note that there is a 90 degree rotation between the orientation below and the orientation described in the register section of the Technical Reference Manual. If PSoC Designer is not used, the application firmware should read and invert the Y count register for X data, and read the X count register for Y data.

Figure 14. Sensor Orientation when using Cypress PSoC Designer Software
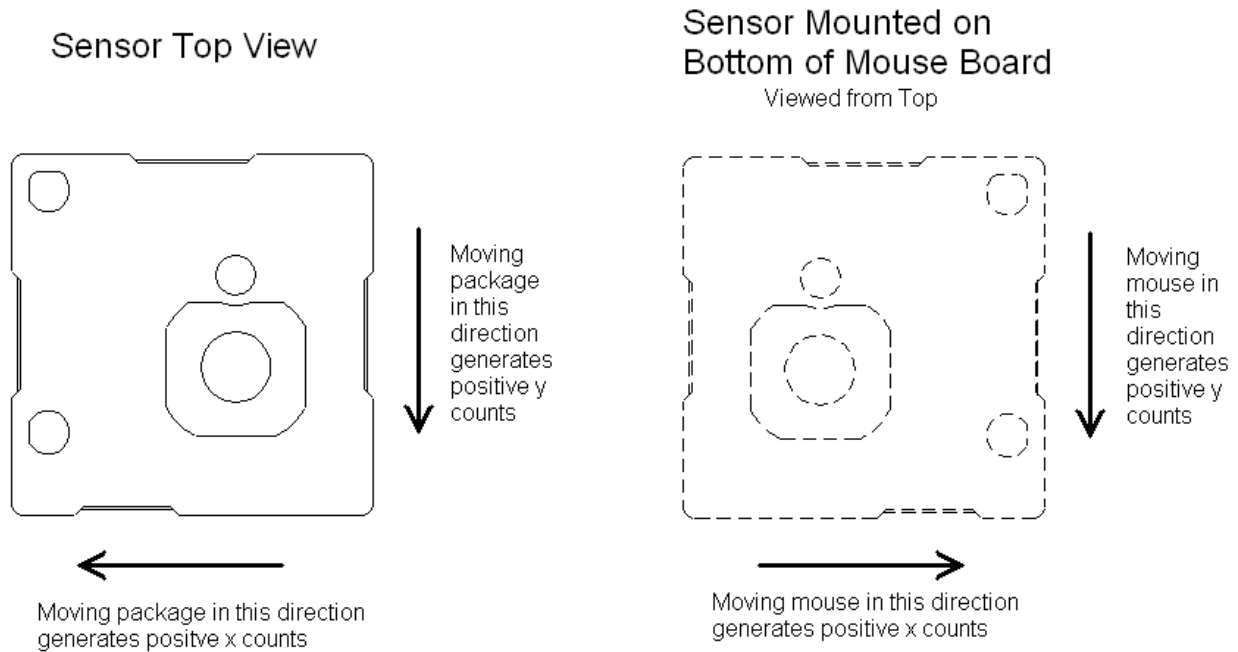
PCB Mounting Height and Thickness

Figure 15 shows the recommended thickness and mounting height of the PCB above the tracking surface.

Figure 15. PCB Height and Thickness

[+] Feedback
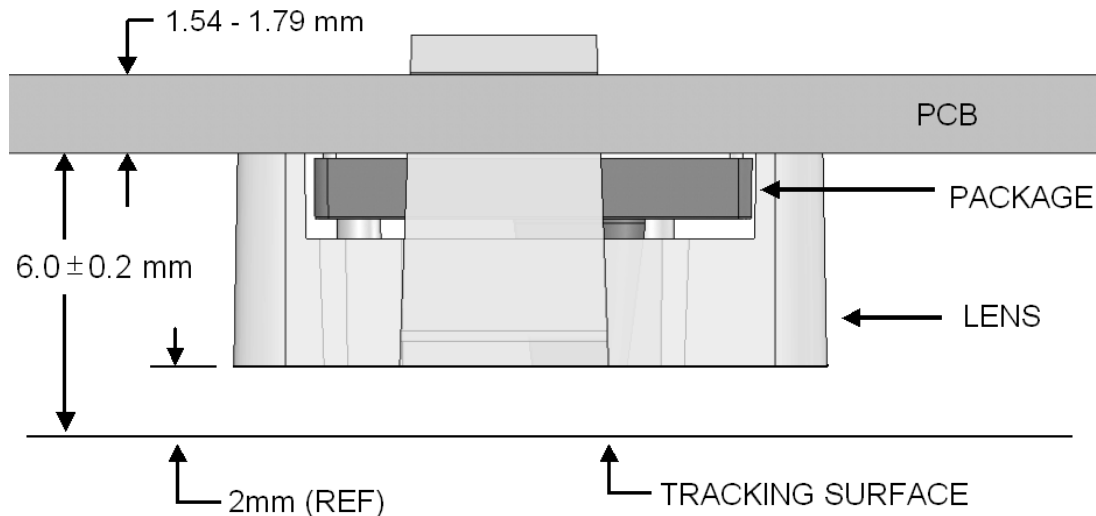
Thermal Impedances

Package	Typical θ_{JA}[12]
42 PQFN[13]	24 °C/W

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Package	Minimum Peak Temperature[14]	Maximum Peak Temperature
42 PQFN	240°C	260°C

Notes
12. $T_J = T_A$ + Power x θ_{JA}.
13. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.
14. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

[+] Feedback

Laser Safety Considerations

The CYONS2000 Laser Navigation SoC and the CYONSLENS2000 lens are designed and tested to enable manufacturers to achieve eye safety certification with minimal effort. This section provides guidelines for complying with the Class 1 emission requirements of IEC/EN 60825-1.

When installed and operated in accordance with all requirements in this data sheet, the kit consisting of the CYONS2000 Laser Navigation SoC and CYONSLENS2000 satisfies CDRH 21 CFR 1040 per Laser Notice 50 and IEC/EN 60825-1 Class 1.

Laser Output Power

The CYONS2000 sensor package contains an integrated VCSEL and drive circuitry. Before shipping, Cypress adjusts the laser output power to eye-safe levels, taking into account specified variations in supply voltage, temperature, lens transmission, and VCSEL polarization, and factors such as VCSEL aging and test equipment accuracy. The output remains within eye-safe limits under reasonably foreseeable single-faults, as required by the IEC standard.

From the perspective of a manufacturer, laser emission remains within the Class 1 limit, as defined in IEC 60825-1, Edition 2, 2007, provided the following requirements are met.

■ The supply voltage applied to pins DVDD and AVDD of the SoC must be in the range of 2.7 to 3.6V.

■ The operating temperature must be between 5 and 45 °C.

■ The laser output power must not be increased by any means, including but not limited to firmware, hardware, or mechanical modifications to the sensor or lens.

■ The mechanical housing must be designed such that the CYONSLENS2000 cannot be removed by the user.

■ The device firmware must initialize the VCSEL driver as described in the "VCSEL Driver" chapter of the OvationONS II Technical Reference Manual.

It is the responsibility of the manufacturer to ensure these conditions are always met and to demonstrate end-product compliance to the appropriate regulatory standards.

Laser Output Power Test Procedure

To verify the laser output level, follow the steps shown in the "VCSEL Power Calibration and Verification" section of the Technical Reference Manual.

Registration Assistance

The mouse or end-product supplier is responsible for certifying the end-use product with respect to the drive voltage, manuals and labels, and operating temperature specifications. Additionally, for products sold in the US, a CDRH report must be filed for each model produced, and test and inspection of the product's characteristics as they relate to laser safety and the CDRH requirements must be performed.

When filing a report with the CDRH, the supplier can refer to the product report filed by Cypress for the CYONS2xxx family of products. The Cypress report is based on the previously-noted limits for voltage and temperature, and describes how the sensor design includes consideration of drive circuit failures, laser output variation with temperature, drive circuit variation with temperature and voltage, polarization sensitivity of molded optics, and measurement uncertainties.

Cypress can provide assistance to customers who want to obtain registration. Supporting documentation, including a verification test procedure to demonstrate end-product compliance with IEC and CDRH requirements is available. An application note, "Meeting Laser Safety Requirements with the CYONS2xxx Family of Laser Navigation SoCs", is also available. For further information, contact a Cypress representative.

Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CYONS2000.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com/psocdesigner and includes a free C compiler with version Service Pack 4.5 or later.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

Mouse Design Kits

Two kits featuring the OvationONS™ II family of products are available. The reference design kit provides a complete hardware, firmware, and software solution, ready for production. The demonstration kit provides tested hardware and firmware that demonstrate the capabilities of the OvationONS II device.

■ CY4631 Wired Mouse Reference Design Kit

■ Wireless Mouse Demonstration Kit

Development Kits

You can purchase the development kits from the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK kit enables prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

■ PSoC Designer Software CD

■ ICE-Cube In-Circuit Emulator

■ ICE Flex-Pod for CY8C29x66 Family

■ Cat-5 Adapter

■ Mini-Eval Programming Board

■ 110 ~ 240V Power Supply, Euro-Plug Adapter

■ iMAGEcraft C Compiler (Registration Required)

■ ISSP Cable

■ USB 2.0 Cable and Blue Cat-5 Cable

■ Two CY8C29466-24PXI 28-PDIP Chip Samples

CY3210-ExpressDK PSoC Express Development Kit

The CY3210-ExpressDK enables advanced prototyping and development with PSoC Express (may be used with ICE-Cube In-Circuit Emulator). It provides access to voltage reference, switches, upgradeable modules and more. The kit includes:

■ PSoC Express Software CD

■ Express Development Board

■ Four Fan Modules

■ Two Proto Modules

■ MiniProg In-System Serial Programmer

■ MiniEval PCB Evaluation Board

■ Jumper Wire Kit

■ USB 2.0 Cable

■ Serial Cable (DB9)

■ 110 ~ 240V Power Supply, Euro-Plug Adapter

■ Two CY8C24423A-24PXI 28-PDIP Chip Samples

■ Two CY8C27443-24PXI 28-PDIP Chip Samples

■ Two CY8C29466-24PXI 28-PDIP Chip Samples

[+] Feedback

Evaluation Tools

You can purchase the evaluation tools from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables a user to program PSoC devices using the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

■ MiniProg Programming Unit

■ MiniEval Socket Programming and Evaluation Board

■ 28-pin CY8C29466-24PXI PDIP PSoC Device Sample

■ 28-pin CY8C27443-24PXI PDIP PSoC Device Sample

■ PSoC Designer Software CD

■ Getting Started Guide

■ USB 2.0 Cable

■ CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all your evaluation needs. The kit includes:

■ Evaluation Board with LCD Module

■ MiniProg Programming Unit

■ 28-pin CY8C29466-24PXI PDIP PSoC Device Sample (2)

■ PSoC Designer Software CD

■ Getting Started Guide

■ USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

■ PSoCEvalUSB Board

■ LCD Module

■ MIniProg Programming Unit

■ Mini USB Cable

■ PSoC Designer and Example Projects CD

■ Getting Started Guide

■ Wire Pack

Device Programmers

You can purchase the device programmers from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

■ Modular Programmer Base

■ Three Programming Module Cards

■ MiniProg Programming Unit

■ PSoC Designer Software CD

■ Getting Started Guide

■ USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer.
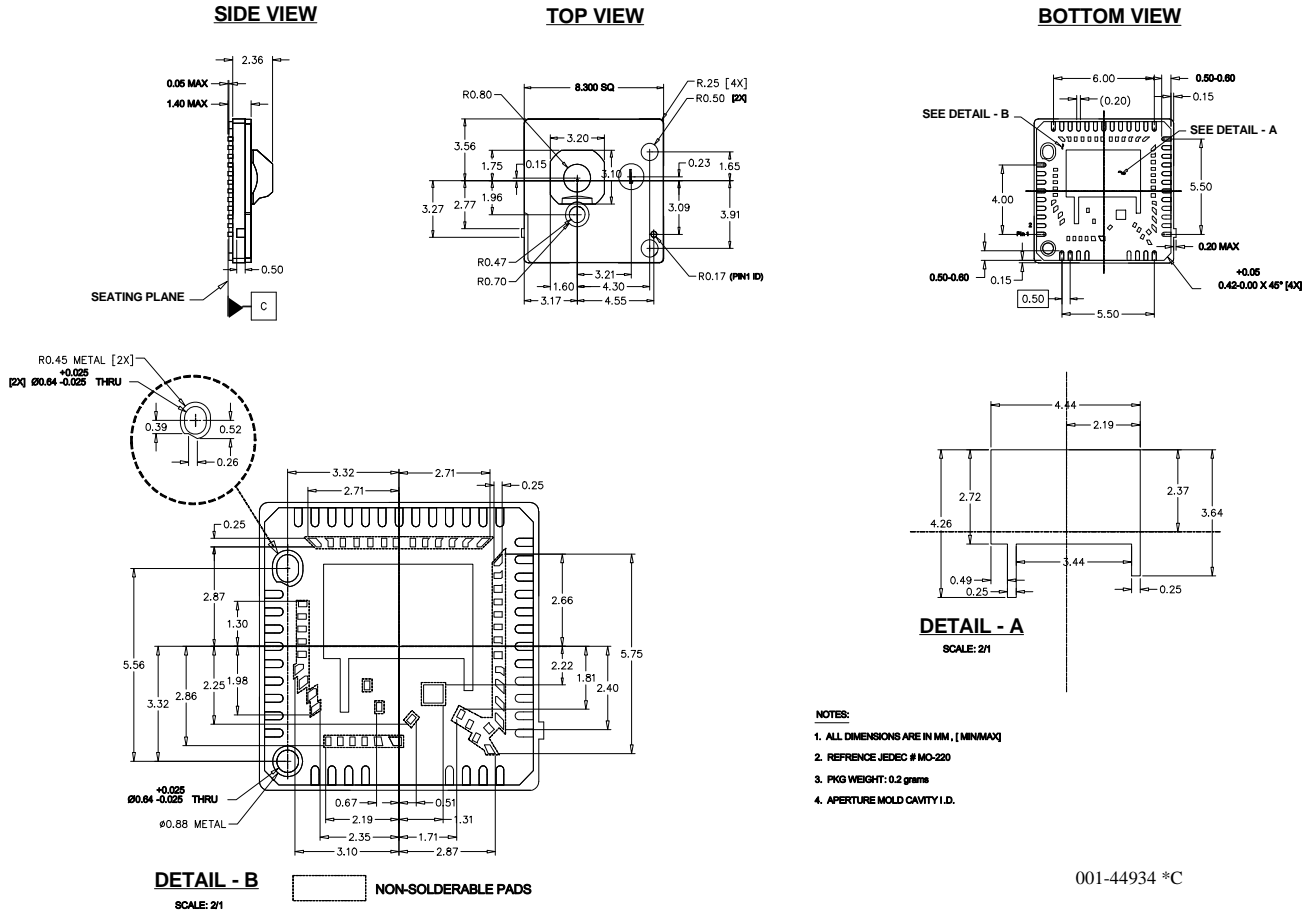
The kit includes:

■ CY3207 Programmer Unit

■ PSoC ISSP Software CD

■ 110 ~ 240V Power Supply, Euro-Plug Adapter

■ USB 2.0 Cable

Third-Party Tools

Several tools have been specially designed by third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools are found at http://www.cypress.com.
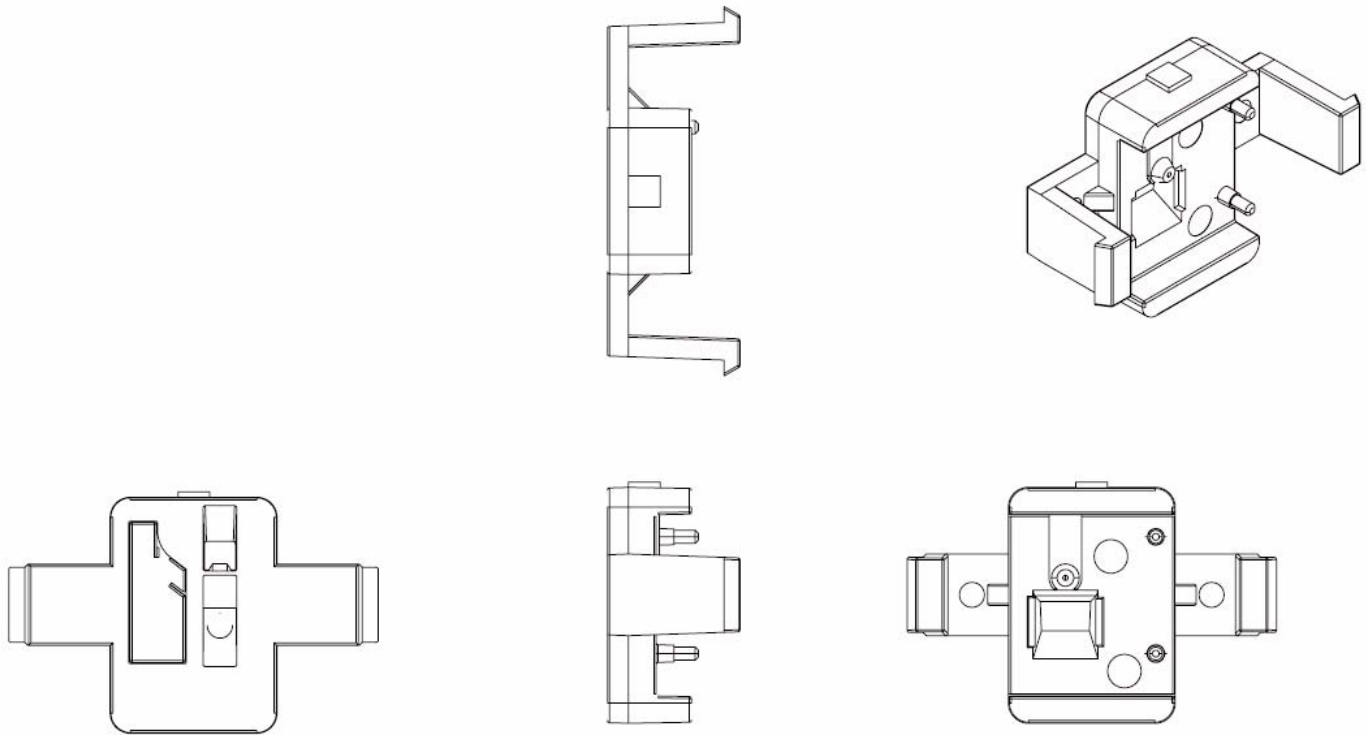
Package Diagrams

Figure 16. QFN Package

SIDE VIEW   TOP VIEW   BOTTOM VIEW

DETAIL - B
SCALE: 2/1

NON-SOLDERABLE PADS

DETAIL - A
SCALE: 2/1

NOTES:
1. ALL DIMENSIONS ARE IN MM, [MIN/MAX]
2. REFRENCE JEDEC # MO-220
3. PKG WEIGHT: 0.2 grams
4. APERTURE MOLD CAVITY I.D.

001-44934 *C

Figure 17. Lens

001-44677 *A

Ordering Information

The CYONS2000 and CYONSLENS2000 are sold separately. When placing orders, order both part numbers.

Part Number	Package	Application
CYONS2000-LBXC	42 pin PQFN	Desktop Wired
CYONSLENS2000-C	Lens - 4 mm Height	Molded Optic

[+] Feedback

Document History Page

Document Title: CYONS2000 OvationONS™ II Wired Laser Navigation System on Chip Document Number: 001-44044				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2261927	FJZ	See ECN	New Data Sheet.
*A	2580125	FJZ/PYRS	10/07/08	Extensive Updates
*B	2769396	FJZ/AESA	25/09/09	Updated Getting Started and Development Tools sections. Updated thermal impedance, wireless kit part number, Flash specs, storage temperature, I2C footnote, pin table, and c compiler information.
*C	2889331	FJZ	03/09/10	Added Table of Contents. Updated package diagram and sales links.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

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