SM530

Low EMI Spectrum Spread Clock

Features

- Reduces systemic EMI
- Modulates external source clock
- 3–5 Volt power supply
- 14 to 120 MHz operating frequency range
- Output is multiplied or divided by 1, 2 or 4
- Digitally controlled modulation
- TTL and CMOS compatible outputs
- Center and down spread modulation
- Compliant with all major CISC, RISC, and DSP processors
- Low short term jitter
- Synchronous output enable
- Power down mode for low current operation
- Available in 20 pin SSOP and TSSOP packages

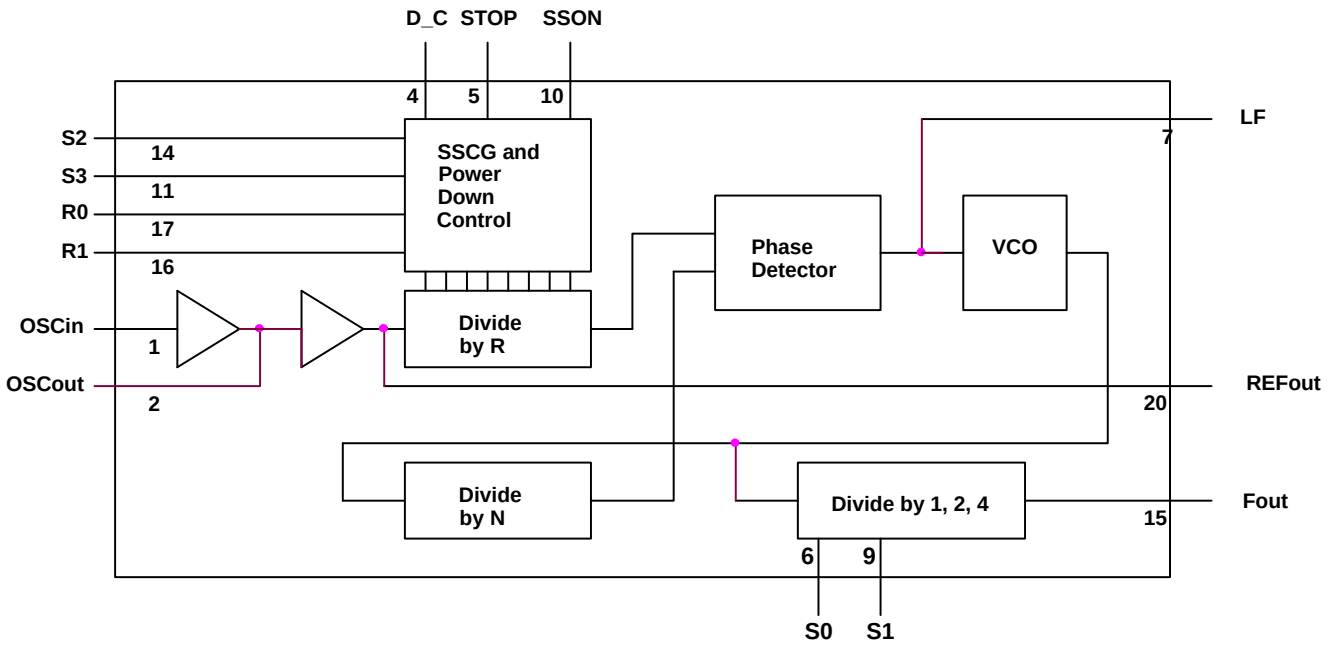
Applications

- Desktop or laptop computers
- Modems
- Scanners, printers, copiers, fax machines, and MFPs
- Disk and CD-ROM drives
- Automotive and embedded systems
- Networking, LAN/WAN
- Digital cameras, games
- LCD displays

Benefits

- Time to market
- Lower cost of compliance
- Programmable EMI reduction
- No degradation in rise and fall times
- Lower component and PCB layer count

Block Diagram



General Description

The SM530 is a Spectrum Spread Clock Modulator designed to reduce the electromagnetic interference (EMI) found in today's high speed digital systems. The SM530 is well suited for a wide range of digital system applications that require a reduction of radiated energy. This unwanted radiated energy is usually found in the odd harmonics of digital system clocks. Increasing the bandwidth of the digital clock, greatly reduces measured EMI at the fundamental and harmonic frequencies. This reduction in radiated energy significantly reduces the cost of complying with regulatory requirements and time to market, without degrading clock and timing signals.

The SM530 is extremely versatile and flexible in that program control is available for each of the operating modes. Program control provides for input frequency, output frequency multiplication, output bandwidth, center/down spread of Fout, modulation ON/OFF, and Fout state during power down mode.

Depending on the range of operation, the output clock Fout is a multiple (1, 2, 4) or a fraction (1, 1/2, 1/4) of the input frequency. The SM530 synchronously stops the modulated output at the low logic level. The power down mode adds the flexibility of operating in a completely static mode for reduced standby current and simplified system board testing.

There are many benefits to using the SM530 Low EMI Clock Modulator. The most important benefit is reducing the amount of clock related EMI by as much as 12–18 dB, depending on the application. Refer to SM532 data sheet for the 16 pin SOIC version, which only supports center spread operation.

Figure 1. SM530 SSOP/TSSOP Package Pin Assignment

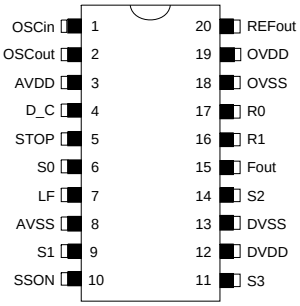


Table 1. Pin Descriptions

Pin No.	Pin Name	IO	Type	Description
1, 2	OSCin OSCout	IO	CMOS	These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. OSCin connects to a TTL or CMOS external clock source. AC coupling is required. If OSCin connects to an external clock other than a crystal, leave OSCout (pin 2) unconnected. The input frequency range is 14 to 120 MHz @ 5.0 Vdc.
3	AVDD	Power	Power	Analog circuit positive power supply.
4	D_C	I	TTL	Input selection pin used to determine the center frequency position of modulated Fout (pin 15). Pin 4 has an internal pull down resistor. D_C = 0: Down spread. D_C = 1: Center spread.
5	STOP	I	TTL	When = 1, pin 5 synchronously stops Fout clock at a logic low state. Pin 5 has an internal pull down resistor.
6, 9	S0, S1	I	TTL	Input control used to select the frequency multiplication at Fout, relative to the reference clock. See Table 2 on page 3. S0 has an internal pull down resistor. S1 has an internal pull up resistor.
7	LF	O	Analog	Single ended tri-state output of the phase detector. A two pole passive loop filter connects to LF. See Table 5 on page 5 for proper values.
8	AVSS	Ground	Ground	Analog circuit ground.
10	SSON	I	TTL	Input control pin used to enable modulation at the Fout pin. SSON = 0 = Modulation ON. SSON = 1 = Modulation OFF. SSON has an internal pull down resistor.

Table 1. Pin Descriptions (continued)

Pin No.	Pin Name	IO	Type	Description
11, 14	S2, S3	I	TTL	Input control pins. These pins set the amount of modulation at Fout. See Table 2 on page 3 for settings. S2 has an internal pull up resistor. S3 has an internal pull down resistor.
12	DVDD	Power	Power	Digital positive power supply. Keep separate from analog power for best performance.
13	DVSS	Ground	Ground	Digital circuit ground.
15	Fout	O	TTL	Modulated clock output.
16, 17	R1, R0	I	TTL	These input pins control the input frequency range as described in Table 2. R0 and R1 have internal pull up resistor.
18	OVSS	Ground	Ground	Oscillator circuit ground. Is common to DVSS.
19	OVDD	Power	Power	Oscillator circuit positive power supply. Is common to DVDD.
20	REFout	O	TTL	Buffered output of the crystal or external clock input (unmodulated).

Frequency Selection Table

Table 2 provides the necessary information for setting the control lines for proper operation of the SM530 and for any frequency within its operating range. Note that the table includes operating frequencies at 3.3 and 5.0 Vdc. The 3.3 Vdc columns are lower in frequency than the 5.0 Vdc operation due to the characteristics of the VCO.

Table 2. Frequency Selection

Vdd = 5		Volts	±10%						Vdd = 3.3		Volts	±5%	
Fin (Range) (MHz)		Fout/Fin	Fout (Range) (MHz)		Multiplier Settings		Input Range Settings		Fin (Range) (MHz)		Fout/Fin	Fout (Range) (MHz)	
Min	Max	X	Min	Max	S1	S0	R1	R0	Min	Max	X	Min	Max
	See note[1]				0	0	X	X		See note[1]			
14	30	1	14	30	0	1	0	1	14	22.5	1	14	22.5
14	30	2	28	60	1	0	0	1	14	22.5	2	28	45
14	30	4	56	120	1	1	0	1	14	22.5	4	56	90
30	60	0.5	15	30	0	1	1	0	25	45	0.5	12.5	22.5
30	60	1	30	60	1	0	1	0	25	45	1	25	45
30	60	2	60	120	1	1	1	0	25	45	2	50	90
60	120	0.25	15	30	0	1	1	1	50	90	0.25	12.5	22.5
60	120	0.5	30	60	1	0	1	1	50	90	0.5	25	45
60	120	1	60	120	1	1	1	1	50	90	1	50	90

Note
1. Selects ‘power down state’, see Table 4 on page 4. X = don’t care condition.

Modulation and Power Down Selections

The two input control lines, S2 and S3, control the bandwidth of the modulation applied to Fout. Also, S2 and S3 control the state the SM530 goes to when the power down mode is selected. Setting both S0 and S1 to a logic state ‘0’, selects the power down mode. Refer to the Table 3 and Table 4 for the proper selection of modulation bandwidth and power down state.

Table 3. Modulation Selection

	Modulation Settings\		D_C = 0 Down Spread		D_C = 1 Center Spread	
Total Bandwidth	**S3**	**S2**	**Low**	**High**	**Low**	**High**
1.25%	0	0	98.75%	100%	99.375%	100.625%
2.50%	0	1	97.50%	100%	98.75%	101.25%
5.00%	1	0	95.00%	100%	97.50%	102.50%
10.0%	1	1	90.00%	100%	95.00%	105.00%

Table 4. Power Down Selection[2]

Fout State	S3	S2
Factory Test	1	0
Hi-Z	1	1
0	0	0
1	0	1

Note The ‘Stop’ and ‘Power Down’ functions are two separate operations. Selecting ‘Stop’ does not place the SM530 in the power down mode. To select ‘Power Down’, set S0 = 0 and S1 = 0.

Note
2. S0 = 0, S1 = 0. For all other states, see Table 2 on page 3.

Loop Filters

The SM530 requires an external loop filter to provide the proper operation and modulation profile for a given input frequency. The loop filter connects to pin 7 (LF) of the SM530 and is a typical 2 pole low pass filter. Because the SM530 operates over such a wide range of frequencies, the loop filter changes depending on the frequency of operation. Use the following loop filter values for best performance and modulation profile at 3.0 volts and 5.0 volts Vdd. Measure the operating voltage at the Vdd pin of the SM530.

Note The selection of loop filter values only depends on the input frequency and Vdd voltage, and does not depend on the R and S settings.

Figure 2. Recommended Loop Filter

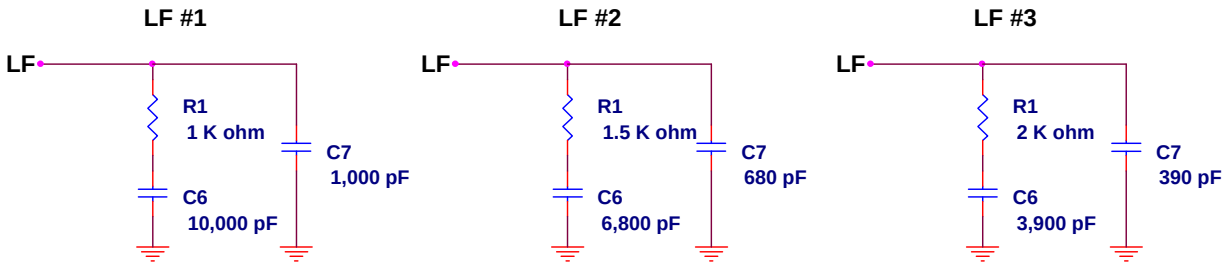


Table 5. Recommended Loop Filter Values

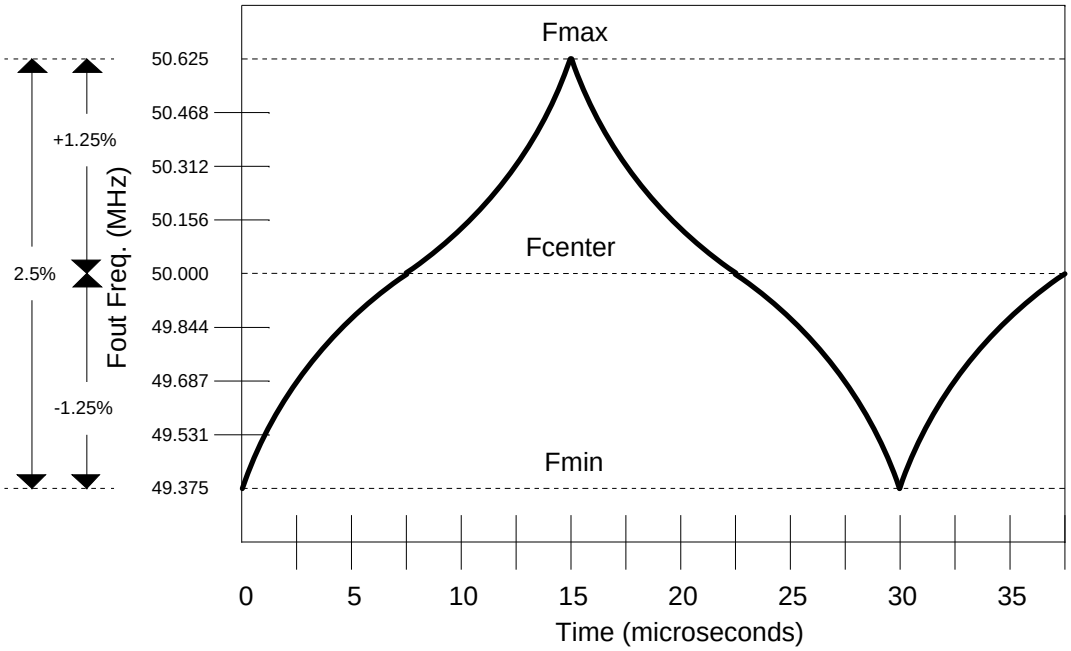
Input Range	Vdd ±5%	Input Frequency Range (MHz)	R1 (KΩ)	C6 (pF)	C7 (pF)	Loop Filter #
Low	3.3	14.0 to 22.5	1.0	10,000	1,000	1
Middle	3.3	25.0 to 45.0	1.0	10,000	1,000	1
High	3.3	50.0 to 90.0	1.0	10,000	1,000	1
Input Range	**Vdd ±10%**	**Input Frequency Range (MHz)**	**R1 (KΩ)**	**C6 (pF)**	**C7 (pF)**	**Loop Filter #**
Low	5.0	14.0 to 19.9	1.0	10,000	1,000	1
Low	5.0	20.0 to 24.9	1.5	6,800	680	2
Low	5.0	25.0 to 29.9	2.0	3,900	390	3
Middle	5.0	30.0 to 39.9	1.0	10,000	1,000	1
Middle	5.0	40.0 to 49.9	1.5	6,800	680	2
Middle	5.0	50.0 to 59.9	2.0	3,900	390	3
High	5.0	60.0 to 79.9	1.0	10,000	1,000	1
High	5.0	80.0 to 99.9	1.5	6,800	680	2
High	5.0	100.0 to 120.0	2.0	3,900	390	3

The component values listed in Table 5 are recommended values using commonly manufactured components. Notice that there are actually three different sets of loop filter values. Due to the VCO characteristics, the table distinguishes between the 3-volt operations and 5-volt operations. Referring to the Table 5, it is apparent that the 3-volt operation requires only one set of loop filter values. In the 5-volt operation, each input operating range is divided into three sections which require a different loop filter for optimal performance. The best loop filter for any application is the one that provides the required EMI reduction, maintains system integrity, has a modulation profile similar to Figure 3 on page 6, and uses commonly available components.

SSCG Modulation Profile

The modulation rate of the SM530 within any range is typically 20–40 kHz. With the correct loop filter connected to pin 7, the following profile provides the best EMI reduction. Figure 3 is the profile that displays on a time domain analyzer.

Figure 3. Modulation Profile



Theory of Operation

The SM530 is a phase-locked loop (PLL) type clock generator that uses direct digital synthesis (DDS). By precisely controlling the bandwidth of the output clock, the SM530 becomes a low EMI clock generator. The sections that follow discuss the theory and detailed operation of the SM530.

EMI

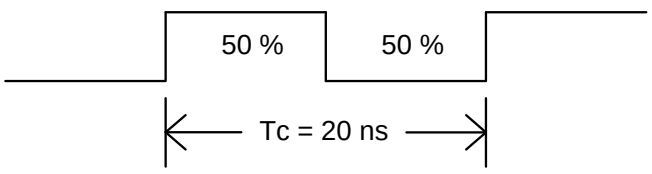
All digital clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50%. Because of the 50/50 duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, such as 3rd, 5th, 7th, and so on. It is possible to reduce the amount of energy contained in the fundamental and harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth with onsequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test can satisfy agency requirements for electromagnetic interference (EMI). Conventional methods of reducing EMI are to use shielding, filtering, multi-layer PCBs, and others. The SM530 uses the approach of reducing the peak energy in the clock by increasing the clock bandwidth, and lowering the Q.

SSCG

SSCG uses a patented technology of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak and cycle to cycle. The SM530 takes a narrow band digital reference clock in the range of 14–120 MHz and produces a clock that sweeps between a controlled start and stop frequency and precise rate of change. The bandwidth of the output clock is programmable. Using two control lines on the SM530, you can control the bandwidth of the modulated clock over four discrete settings: 1.25, 2.50, 5.0, and 10%. To understand what happens to an SSCG clock, consider that we have a 50 MHz clock with a 50% duty cycle. From a 50 MHz clock we know the following:

Clock frequency = **Fc** = 50 MHz
Clock period = **Tc** = 1/50 MHz = 20 ns

Figure 4. Unmodulated Clock



You can apply the 50 MHz clock to the OSCin input of the SM530, either as an externally driven clock or as the result of a parallel resonant crystal connected to pins 1 and 2 of the SM530. The SM530 is programmed for the following operation:

Range (R0, R1) =	0, 1	Mid Range
Multiplier (S0, S1) =	0, 1	X1
D_C =	1	Center Spread
SSON =	1	Modulation is OFF
% Modulation (S2, S3) =	1, 0	2.50% Spread

From these parameters, the output clock at Fout is 50.625 MHz. With modulation turned OFF, the frequency of Fout always rests at the high end of the programmed spectrum. In this case, +1.25% of 50 MHz equals 50.625 MHz.

When you turn modulation ON, the clock at Fout begins sweeping downward to the minimum extreme of -1.25% of 50 MHz which is 50 MHz – 0.625 MHz = 49.375 MHz. When the clock reaches 49.375, the SM530 begins sweeping back up to the maximum extreme of 50.625 MHz. On a spectrum analyzer, the clock looks similar to the picture in Figure 5. Keep in mind that this is a drawing of a perfect clock with no noise.

Notice that the original 50 MHz reference clock is at the center frequency, Cf, and the minimum and maximum extremes are positioned symmetrically around the center frequency. This type of modulation is called ‘center spread’. Figure 5 illustrates this as it displays on a spectrum analyzer. Notice that when modulation is OFF, the Fout clock is at the maximum extreme of the bandwidth.

Figure 5. Output Clock

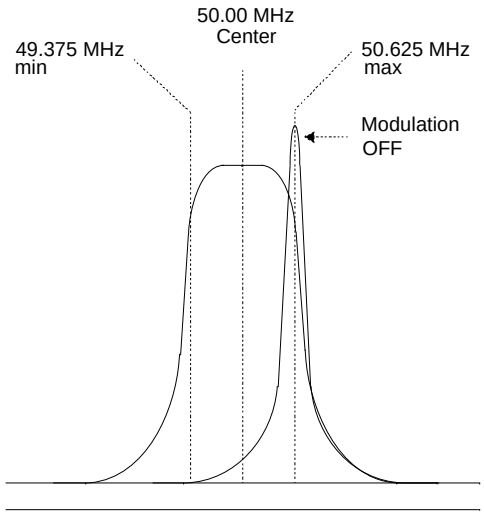
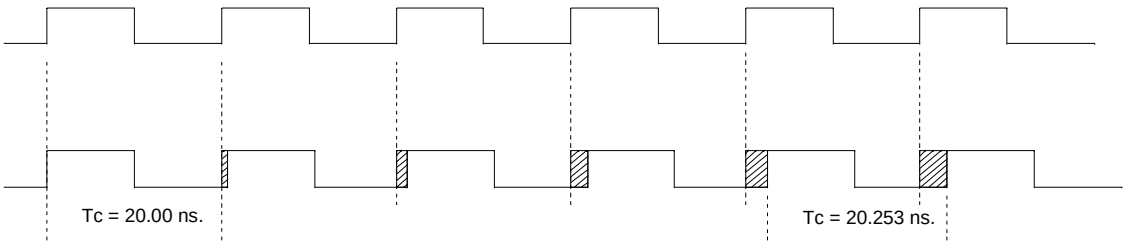


Figure 6 shows the 50 MHz clock as it appears on an oscilloscope. The top trace is the non-modulated reference clock, or the REFout clock at pin 20. The bottom trace is the modulated clock at pin 15. From this comparison chart you can see that the frequency is decreasing and the period of each successive clock is increasing. The Tc measurements on the left and right of the bottom trace indicate the period of the clock as it moves from the center frequency at 50 MHz and the minimum frequency at 49.375 MHz extremes of the clock. Intermediate clock changes are small and accumulate to achieve the total period deviation. The reverse of this diagram shows the clock period getting smaller as the frequency increases.

Figure 6. Period Comparison Chart



There are certain cases where center spread modulation is not applicable. If the maximum design frequency of the intended application is 50 MHz and becomes unstable above 50 MHz, then increasing the clock to 50.625 MHz might cause unwanted system problems.

To accommodate this situation, the SM530 has an operating mode where the maximum Fout frequency never exceeds the reference frequency, not including any multiplier. This type of modulation is ‘down spread’. The effective center frequency of the Fout clock shifts down by one-half the amount of the applied modulation.

If the amount of clock spread is set for 2.50%, the effective center frequency of Fout is 1.25% less than 50 MHz, or 49.375 MHz, when modulation is ON. When modulation is OFF, the Fout frequency goes to 50.0 MHz, since this is the maximum extreme of the applied modulation settings. The one drawback to down spread modulation is that the effective center frequency of the clock is, in this case, 1.25% slower. This means that the performance of the system is 1.25% slower.

Using the previous operating parameters for the SM530 and selecting down spread, the operating bandwidth is as follows:

Range (R0, R1) =	0, 1	Mid Range
Multiplier (S0, S1) =	0, 1	X1
D_C =	0	Down Spread
SSON =	0	Modulation is ON
% Modulation (S2, S3) =	1, 0	2.50% Spread

To calculate the frequency extremes for these conditions in down spread mode, first determine the effective center frequency, Cf. In this case Cf is:

Cf = OSCin – (OSCin X % Spread)

Cf = 50 MHz – (50 MHz X .0125)

Cf = 50 MHz – 0.625 MHz

Cf = 49.375 MHz

With the effective center frequency at 49.375 MHz, you can now determine the minimum and maximum extremes.

Fmax = Cf + (Cf X % Spread)	Fmin = Cf – (Cf X % Spread)
Fmax = 49.375 + (49.375 X 0.0125)	Fmin = 49.375 – (49.375 X 0.0125)
Fmax = 49.375 + .617	Fmin = 49.375 – 0.617
Fmax = 49.99 MHz	Fmin = 48.758 MHz

Another way of calculating the bandwidth in the down spread mode is to use the OSCin frequency as the starting point and multiplying the % spread by ‘2’. This assumes that the multiplier is ‘1’. If the multiplier is ‘2’, then use two times the OSCin in the formula.

Fmax = OSCin

Fmin = OSCin - (OSCin X (2 X % Spread))

Fmin = 50 MHz - (50 X (2 X 0.0125))

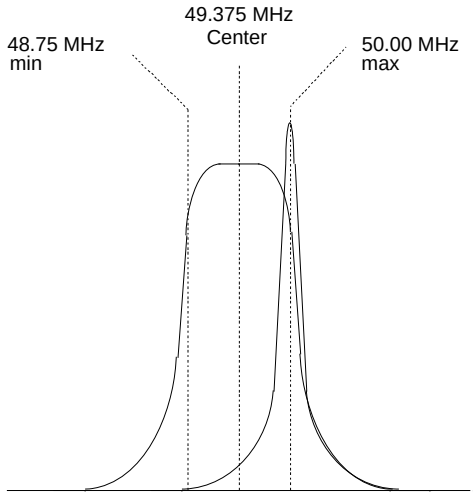
Fmin = 50 – 1.25

Fmin = 48.75 MHz

Figure 7 illustrates this. The effective center frequency is 49.375 MHz and the minimum and maximum extremes are 1.25% on either side of the center. Or using the second approach, the OSCin frequency is the maximum frequency and the minimum frequency is 2.5% down from the reference.

Looking at Figure 7, notice that the peak amplitude of the 50 MHz non-modulated clock is higher than the wide band modulated clock. This difference in peak amplitudes between modulated and unmodulated clocks is the reason why SSCG clocks are so effective in digital systems. This and the previous illustrations refer to the fundamental frequency of a clock. A very important characteristic of the SSCG clock is that the bandwidth of the harmonics is multiplied by the harmonic number. In other words, if the bandwidth of a 50 MHz clock is 1.35 MHz, the bandwidth of the 3rd harmonic is three times 1.35, or 4.05 MHz. The amount of bandwidth is relative to the amount of peak energy in the clock. Consequently, the wider the bandwidth, the greater the energy reduction of the clock.

Figure 7. Clock Spread



Most applications do not have a problem meeting agency specifications at the fundamental frequency. It is the higher harmonics that usually cause the most problems. With an SSCG clock, the bandwidth and peak energy reduction increases with the harmonic number. Consider that the 11th harmonic of our 50 MHz clock is 550 MHz. With a total spread of 1.35 MHz at 50 MHz, the spread at the 11th harmonic is 14.85 MHz which greatly reduces the peak energy content. It is typical to see as much as 12 to 18 dB of reduction at the higher harmonics, due to a modulated clock.

Referring to Figure 5 on page 7 and Figure 7, you can see that the peak amplitude of the unmodulated clock is much higher than the peak amplitude of the modulated clock. This is the reason the SM530 is used for EMI reduction. The amount of EMI reduction is dependent on the application. The difference in the peak energy of the modulated clock and the non-modulated clock in typical applications sees a 2–3 dB reduction at the fundamental and as much as 8–10 dB reduction at the intermediate harmonics: 3rd, 5th, 7th, and so on. At the higher harmonics, it is quite possible to reduce the peak harmonic energy, compared to the unmodulated clock, by as much as 12 to 18 dB.

You can calculate the dB reduction for a given frequency and spread using a simple formula. This formula is only helpful in determining a relative dB reduction for a given application. This formula assumes an ideal clock with 50% duty cycle and therefore only predicts the EMI reduction of even harmonics. Other circumstances such as non-ideal clock and noise affects the actual dB reduction. The formula is as follows:

dB = 6.5 + 9(Log10(F)) + 9(Log10(P))

Where, F = frequency in MHz, P = total % spread (2.5% = 0.025).

Using a 50 MHz clock with a 2.5% spread, the theoretical dB reduction is:

dB @ 50 MHz (Fund) = 6.5 + 15.29 - 14.42 = 7.37

dB @ 150 MHz (3rd) = 6.5 + 19.58 - 14.42 = 11.66

dB @ 550 MHz (11th) = 6.5 + 24.66 - 14.42 = 16.74

Modulation Profile

The SM530 moves from maximum to minimum frequencies of its bandwidth at a predetermined rate and profile. You can determine the modulation frequency using the input frequency and an internal divider. All three operating ranges modulate the Fout clock between 20 to 40 kHz. The three operating ranges are 14–30 MHz, 30–60 MHz, and 60–120 MHz. If OSCin = 15 MHz, the modulation rate is 20 kHz. If OSCin is 60 MHz, in mid-range, the modulation rate is 40 kHz. To provide the proper modulation rate, divide the input reference frequency by a fixed number in each range. Divide the input reference frequency by 750 in low range, 1500 in mid range and 3000 in the high range. From these numbers, you can determine the modulation rate for any input frequency.

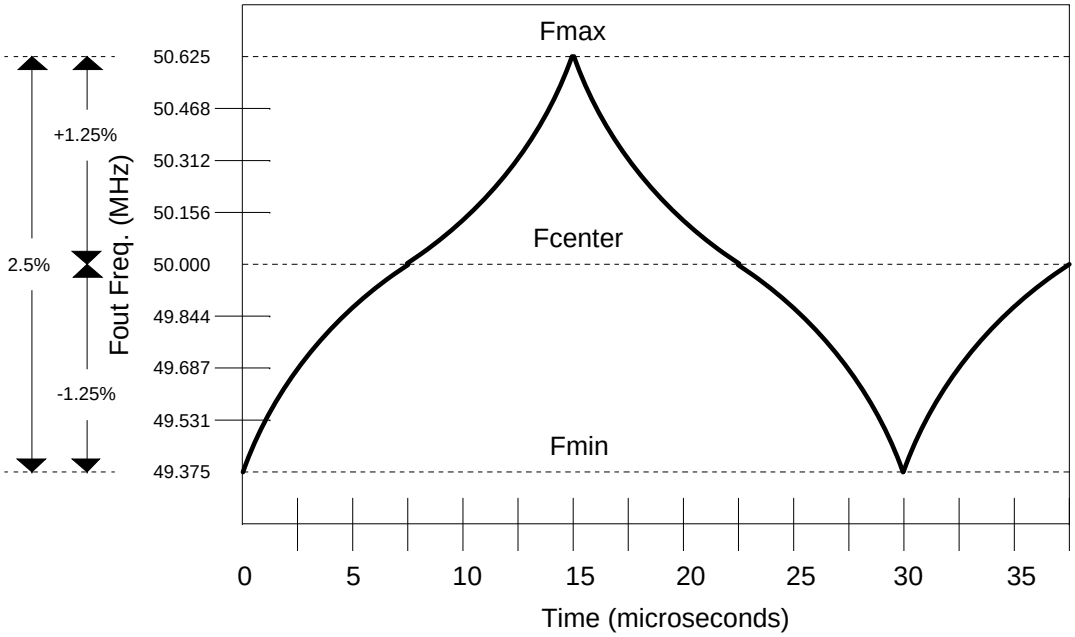
Example

OSCin = 45.378 MHz, Input Range = Mid, Input divisor = 1500
Fmod = OSCin /1500
Fmod = 30.252 kHz

If you have a clock frequency that is on the boundary of the mid-range and high range of operation, you can determine which range to use by knowing which modulation you want. If you choose the mid-range, the modulation rate is 40 kHz, while choosing the high range yields a 20 kHz modulation rate. There is some operational overlap between ranges, such that 58 MHz in the mid-range given the same results as 58 MHz in the high range, except for the modulation rate. This type of operation is not recommended.

The modulation profile of the SM530 is not a linear sweep from maximum to minimum and back. The OSCin reference clock determines the modulation frequency but the internal SSCG control logic determines the actual modulation profile. To best describe the modulation profile compare the instantaneous frequency at Fout with time. The illustration in Figure 8 is a representation of the modulation profile of the SM530 that displays on a time domain analyzer.

Figure 8. Frequency Profile in Time Domain



Notice that in Figure 8, the Fout or Time profile progresses through frequencies depending on where it is in the sweep. If the frequency is in the middle of the sweep, the rate of change is slower compared to the rate at the extremes of the band. When the frequency is nearing the end of the band, it is moving through these frequencies faster, because it has to sweep through these same frequencies again after reversing direction. This modulation profile is one of the key elements to the SM530. Using a linear sweep through all frequencies does not give as good of results in EMI reduction.

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, take precautions to avoid application of any voltage higher than the absolute maximum rated voltages to this circuit. For proper operation, constrain Vin and Vout to within the range, Vss < (Vin or Vout) < Vdd. All digital inputs are tied high or low internally. Refer to the electrical specifications for operating supply range.

Table 6. Supply Range

Parameter	Item	Min	Max	Units
VDD	Supply voltage	0	6.0	Vdc
VIRvss	Input, relative to Vss	–0.3	Vdd + 0.3	Vdc
VORvss	Output, relative to Vss	–0.3	Vdd + 0.3	Vdc
ΔVpp	AVDD relative to DVDD	–100	+100	mV
ΔVss	AVSS relative to DVSS	–100	+100	mV
TOP	Temperature, operating	0	+70	° C
TST	Temperature, storage	– 65	+150	° C

Table 7. Electrical Characteristics [3]

Parameter	Characteristic	Min	Typ	Max	Units
VIL	Input low voltage	-	-	0.8	Vdc
VIH	Input high voltage	2.0	-	-	Vdc
IIL	Input low current	-	-	100	μA
IIH	Input high current	-	-	100	μA
VOL	Output low voltage IOL = 8 mA, Vdd = 5V	-	-	0.4	Vdc
VOH	Output high voltage IOH = 8 mA, Vdd = 5V	Vdd -1.0	-	-	Vdc
VOL	Output low voltage IOL = 5 mA, Vdd = 3.3V	-	-	0.4	Vdc
VOH	Output high voltage IOH = 3 mA, Vdd = 3.3V	2.4	-	-	Vdc
C_{in1}	Input capacitance (pin-1)	-	5	-	pf
C_{in2}	Output capacitance (pin-2)	-	3	-	pf
Rpu	Pull up resistor values (pins 9, 14, 16, and 17)	100K	167K	300K	Ω
Rpd	Pull down resistor values (pins 4, 5, 6, 10, and 11)	150K	250K	350K	Ω
IOZ	Tri-state leakage current (pins 7, 15 and 20)	-	5.0	-	μA
IDD	Static supply current (power down mode)	-	-	250	μA
ICC	5 Volt dynamic supply current (operating mode)	-	25	30	mA
ICC	3 Volt dynamic supply current (operating mode)	-	18	20	mA
ISC	Short circuit current (Fout)	-	-	30	mA

Note
3. Test measurements performed at Vdd = 3.3V ±5% and 5V ±10%, TA = 0°C to 70°C.

Table 8. Timing Characteristics [4]

Characteristic	Symbol	Min	Typ	Max	Units
Output rise time measured at 10%–90% @ 5 Vdc	tTLH	3.3	3.5	3.8	ns
Output fall time measured at 10%–90% @ 5 Vdc	tTHL	2.1	2.3	2.5	ns
Output rise time measured at 0.8V–2.0V @ 5 Vdc	tTLH	0.7	0.75	0.8	ns
Output fall time measured at 0.8V–2.0 V @ 5 Vdc	tTHL	0.6	0.7	0.8	ns
Output rise time measured at 10%–90% @ 3.3 Vdc	tTLH	4.8	5.0	5.4	ns
Output fall time measured at 10%–90% @ 3.3 Vdc	tTHL	2.9	3.2	3.4	ns
Output rise time measured at 0.8V–2.0V @ 3.3 Vdc	tTLH	1.6	1.75	1.9	ns
Output fall time measured at 0.8V–2.0 V @ 3.3 Vdc	tTHL	1.1	1.3	1.5	ns
Output duty cycle	TsymF1	45	50	55	%
Peak-to-peak jitter one sigma (SSON = 1)	tj1s	-	250	500	ps

Note
4. Measurements performed at Vdd = 3.3V ±5% and 5V ±10%, TA = 0°C to 70°C, CL = 15 pF, Fout = 50.0 MHz.

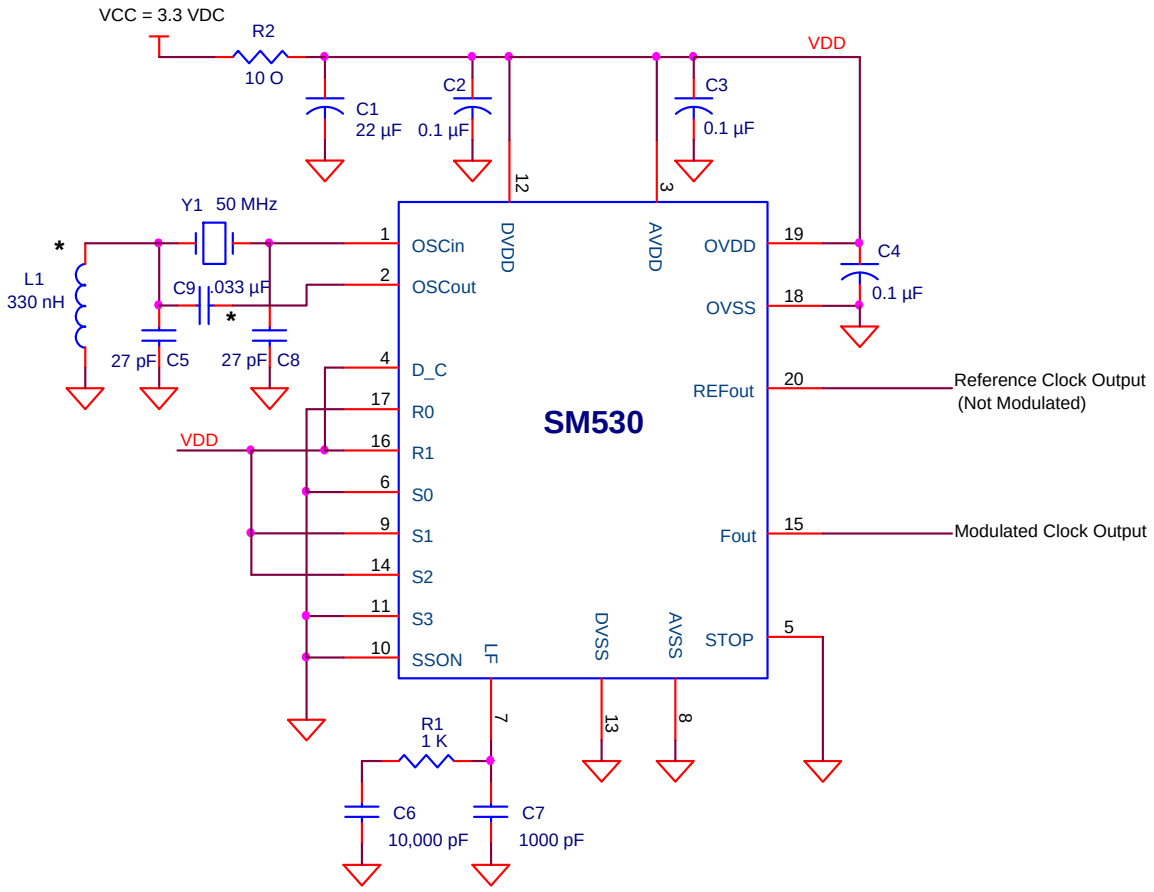
Applications and Schematics

Figure 9 is a simple minimum component application example of an SM530 design. In this example, the configuration of the control lines are for the parameters as follows:

Input frequency: Mid-Range
Multiplier: X1
Modulation: 2.50%
SSON: ON

Refer to loop filter values on Table 5 on page 5 for operation at 3.3 volts DC.

Figure 9. Application Schematic



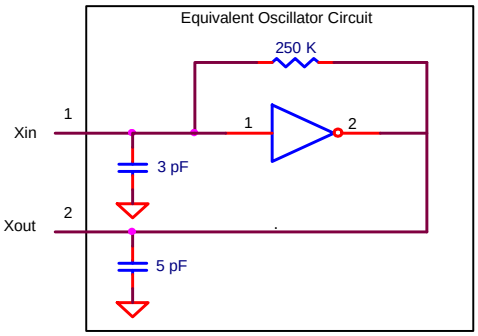
* LI and C9 are required when Y1 is a 3rd overtone crystal.

The SM530 has an internal analog power and ground and a digital power and ground. In the previous example, the digital and analog circuits are connected together. If noise is a concern, separate the analog and digital power and grounds. Use the loop filter in Figure 9 for operations at 3.0–3.6 Vdc. Use this filter also in 5.0 Vdc operations when operating in the low frequency end of each of the three input frequency ranges. Refer to Table 5 on page 5 for loop filter information. Notice that the crystal, Y1, is a third overtone 50 MHz crystal, which requires an inductor and decoupling capacitor to OSCout.

Figure 10 shows the equivalent internal oscillator circuit for the SM530.

Figure 10. Equivalent Oscillator Circuit

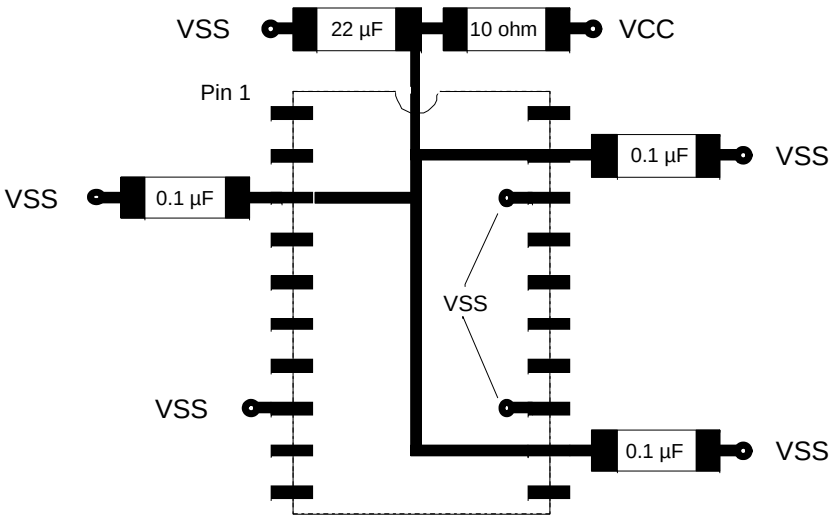
PCB Layout Example



The SM530 Spectrum Spread clock is a PLL type hybrid circuit. This means that it contains both digital and analog circuits on the same die. The phase detector, loop filter and VCO are analog circuits that must operate in a very low noise environment for best performance. There are several ways to keep this noise to a minimum, such as placing bypass capacitors on all power pins and separating the analog and digital power and ground planes.

Figure 11 uses the first approach of placing bypass capacitors as close to every power pin as possible. In addition, make certain to connect all ground pins directly to the ground plane with little or no trace length. Figure 11 shows only the power and ground circuits of the SM530. For best performance, locate other circuits such as the loop filter components as close to the loop filter pin as possible.

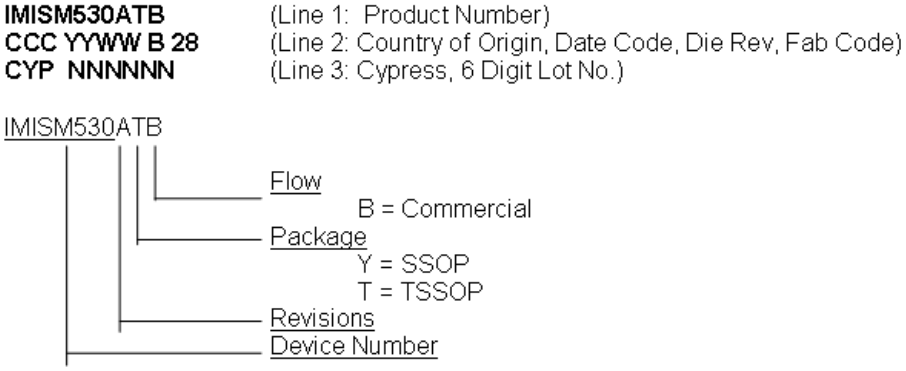
Figure 11. M530 Single Power Plane PCB Layout



Ordering Information

Part No	Package	Operating Temperature Range
IMISM530AYB	20 pin SSOP	0°C to 70°C
IMISM530ATB	20 pin TSSOP	0°C to 70°C
Pb-Free		
CYISM530AYXB[5]	20 pin SSOP	0°C to 70°C
CYISM530AYXBT[5]	20 pin SSOP–Tape and Reel	0°C to 70°C
CYISM530AZXC[5]	20 pin TSSOP	0°C to 70°C
CYISM530AZXCT[5]	20 pin TSSOP–Tape and Reel	0°C to 70°C

Figure 12. Marking Example



Note
5. B = Commercial (IMI Convention), C = Commercial (Cypress Convention)

Package Dimensions and Drawings

Figure 13. 20 Pin SSOP

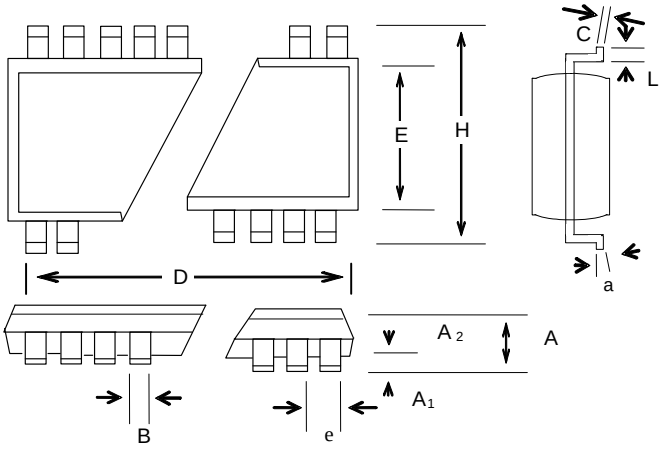


Table 9. 20 PinN SSOP Outline Dimensions

	Inches			Millimeters		
Symbol	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	0.068	0.073	0.078	1.73	1.86	1.99
A_1	0.002	0.005	0.008	0.05	0.13	0.21
A_2	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.278	0.284	0.289	7.07	7.20	7.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95

Figure 14. 20 Pin TSSOP

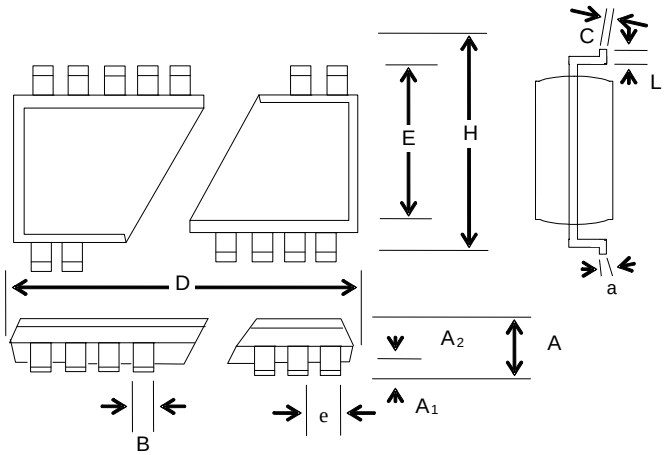


Table 10. 20 Pin TSSOP Outline Dimensions

	Inches			Millimeters		
Symbol	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	-	-	0.047	-	-	1.20
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	-	-	0.035	-	-	0.90
B	0.007	0.95	0.012	0.19	0.245	0.30
C	-	-	-	-	-	-
D	0.252	0.256	0.260	6.40	6.50	6.60
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.026 BSC			0.65 BSC		
H	0.246	0.252	0.258	6.25	6.40	6.55
a	0°	4°	8°	0°	4°	8°
L	0.020	0.025	0.030	0.50	0.625	0.75

Document History Page

Document Title: SM530 Low EMI Spectrum Spread Clock Document Number: 001-10101			
Revision	**ECN**	**Orig. of Change**	**Description of Change**
**	1237224	ARI	New data sheet.