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# FINAL PRODUCT CHANGE NOTIFICATION

**PCN:** PCN084643 **Date:** March 18, 2008

**Subject**: Datasheet Change to Standard SRAM port Read and Write Cycle timing parameters for the 65ns MoBL ADM Dual-Port products.

**To:** EPCN PROGRAM MANAGER
ARROW
epcn@arrow.com

**Description of Change:**
The MoBL ADM Dual-Ports are inter-processor connectivity solutions for mobile handheld devices. The Standard SRAM port Read and Write timing parameters are being changed for the 65ns MoBL ADM Dual-Ports for productivity reasons. Work with lead customer has confirmed that these changes to the 65ns speed product do not adversely affect functionality while enabling Cypress to respond to projected demand ramps.

Currently the access time for the Standard port is set at 40ns. This Notification advises that the Standard port access time is changed to 55ns. The details of the change are described below. No other changes to product functionality have been made.

Associated datasheets and models can be downloaded from the Cypress website (www.cypress.com).

**Benefit of Change:**
Cypress will be better able to respond to customer demand ramps.

**Part Numbers Affected:**
**Affected Parts**: 4

| Item | Marketing Part Number | Description |
|---|---|---|
| 1 | CYDMX064A16-65BVXI | Interprocessor connectivity solutions |
| 2 | CYDMX128A16-65BVXI | Interprocessor connectivity solutions |
| 3 | CYDMX128A16-65BVXIT | Interprocessor connectivity solutions |
| 4 | CYDMX256A16-65BVXI | Interprocessor connectivity solutions |

**Customer Part Numbers Affected:**
**Affected Parts:** N/A

**Qualification Status:**
The MoBL ADM Dual-Port is qualified under Qualification Test Plan QTP# 062201. A copy of QTP# 062201 is attached to this PCN.

**Sample Status:**
Samples are available now. Please contact your local Sales Representative to schedule samples.

**Approximate Implementation Date:**
The change will be effective upon customer approval of this change notification. The datasheet will be updated when this notification has been approved.

**Anticipated Impact:**
The following timing parameters in the datasheet will change for the 65ns MoBL ADM product:

| | | Current Timing | | | New Timing | |
|---|---|---|---|---|---|---|
| | **Standard Port Read Cycle** | | | | | |
| **Parameter** | **Description** | **Min** | **Max** | | **Min** | **Max** |
| tRC | Read Cycle Time | 40 | | | 55 | |
| tAA | Address to Data Valid | | 40 | | | 55 |
| tOHA | Output Hold from Address Change | 5 | | | 5 | |
| tACS | CS# to Data Valid | | 40 | | | 55 |
| tDOE | OE# Low to Data Valid | | 25 | | | 30 |
| tLZOE[24] | OE# Low to Data Low-Z | 5 | | | 5 | |
| tHZOE | OE# High to Data High-Z | | 10 | | | 25 |
| tLZCS | CS# Low to Data Low-Z | 5 | | | 5 | |
| tHZCS | CS# High to Data High-Z | | 10 | | | 25 |
| tLZBE | UB#/LB# Low to Data Low-Z | 5 | | | 5 | |
| tHZBE | UB#/LB# High to Data High-Z | | 10 | | | 25 |
| tABE | UB#/LB# Access Time | | 40 | | | 55 |

| | **Standard SRAM Port Write Cycle** | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min** | **Max** | | **Min** | **Max** |
| tWC | Write Cycle Time | 40 | | | 55 | |
| tSCS | CS# Low to Write End | 30 | | | 45 | |
| tAW | Address Valid to Write End | 30 | | | 45 | |
| tHA | Address Hold from Write End | 0 | | | 0 | |
| tSA | Address Set-Up to Write Start | 0 | | | 0 | |
| tWRL | Write Pulse Width | 25 | | | 40 | |
| tSD | Data Set-Up to Write End | 20 | | | 30 | |
| tHD | Data Hold from Write End | 0 | | | 0 | |
| tHZWE<br>tLZWE | WE# Low to Data High-Z<br>WE# High to Data Low-Z | <br>0 | 15 | | <br>0 | 25 |

| | **Arbitration Timing** | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min** | **Max** | | **Min** | **Max** |
| tBLA | BUSY# Low from Address Match | | 30 | | | 45 |
| tBHA | BUSY# High from Address Match | | 30 | | | 45 |
| tBLC | BUSY# Low from CS# Low | | 30 | | | 45 |
| tBHC | BUSY# High from CS# High | | 30 | | | 45 |
| tPS[27] | Port Set-Up for Priority | 5 | | | 5 | |
| tBDD | BUSY# High to Data Valid | | 30 | | | 45 |

| | | | | | | |
|---|---|---|---|---|---|---|
| tWDD | Write Pulse to Data Delay | | 55 | | | 80 |
| tDDD | Write Data Valid to Read Data Valid | | 45 | | | 65 |

| | **Interrupt Timing** | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min** | **Max** | | **Min** | **Max** |
| tINS | INT# Set Time | | 35 | | | 45 |
| tINR | INT# Reset Time | | 35 | | | 45 |

**Method of Identification:**
The affected parts will retain the same ordering codes as before. There will be no change in the ordering information. Cypress maintains traceability of product to wafer level, including wafer fab location.

**Response Required:**
No response is required.

For additional information regarding this change, contact your local sales representative or by email to pcn_adm@cypress.com.

Sincerely,

Richard Oshiro
PCN Process Manager

# Cypress Semiconductor
# Product Qualification Report

**QTP# 062201 VERSION 1.0**
**September 2007**

| **MoBL ADM Dual Port Static RAM Family**<br>**R52LD-3 Technology, Fab4** | |
|---|---|
| **CYDMX256A16**<br>**CYDMX128A16**<br>**CYDMX064A16** | **4K/8K/16K x 16**<br>**MoBL® ADM Asynchronous Dual–Port Static RAM** |

**CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:**


Rene Rodgers
Principal Reliability Engineer
(408) 943-2732

Mira Ben-Tzur
Quality Engineering Director
(408) 943-2675

## PRODUCT QUALIFICATION HISTORY

| QUAL REPORT | | DESCRIPTION OF QUALIFICATION PURPOSE | | DATE COMP. |
|---|---|---|---|---|
| 99075 | | New Technology R52LD-3 / New Slow Low Power MoBL SRAM, CY62137V | | Apr 99 |
| 052103 | | Qualify 256K Dual Port (Split Voltage) Device Family, R52LD3 Technology from Fab4 | | Nov 05 |
| 062201 | | Qualification of Device 7C02638A (MoBL ADM Dual Port) in R52LD-3 Technology at Fab 4 | | Sep 06 |

| PRODUCT DESCRIPTION (for qualification) | |
|---|---|
| Qualification Purpose: To qualify 3rd Generation MoBL DP ADM on existing package and qualified technology, R52LD-3. | |
| Marketing Part #: | CYDMX256A16, CYDMX128A08, CYDMX064A16 |
| Device Description: | 1.8/2.5/3V 256K/128K/64K (16K/8K/4K x 16) MoBL ADMux Dual port |
| Cypress Division: | Cypress Semiconductor Corporation – Data Communication Division |
| Overall Die (or Mask) REV: | Rev. A |
| What ID markings on Die: | 7C02638A |

| TECHNOLOGY/FAB PROCESS DESCRIPTION – R52LD3 | | | |
|---|---|---|---|
| Number of Metal Layers: | 2 | Metal Composition: | Metal 1: 500 Å-TiW/6000 Å Al-Cu/500 Å TiW<br>Metal 2: 300 Å-Ti/8000 Å Al-Cu/300 Å TiW |
| Passivation Type and Materials: | | 1,000A TEOS + 9,000A SiN | |
| Free Phosphorus contents in top glass layer (%): | | 0% | |
| Die Coating(s), if used: | | N/A | |
| Number of Transistors in Device: | | 2932342 | |
| Number of Gates in Device: | | 733086 | |
| Generic Process Technology/Design Rule ( -drawn): | | R52 TDR (01-30065), 0.25um Technology | |
| Gate Oxide Material/Thickness (MOS): | | 55Å | |
| Name/Location of Die Fab (prime) Facility: | | Cypress Semiconductor – Bloomington Minnesota | |
| Die Fab Line ID/Wafer Process ID: | | 7C02638A | |

## PACKAGE AVAILABILITY

| PACKAGE | ASSEMBLY FACILITY SITE |
|---|---|
| **100-Ball VFBGA** | ASE Taiwan (TAIWN-G) |

**Note: Package Qualification details upon request.**

| MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION | |
|---|---|
| **Package Designation:** | BZ100 |
| **Package Outline, Type, or Name:** | 100-Ball, Very Fine Ball Grid Array (VFBGA) |
| **Mold Compound Name/Manufacturer:** | KE-G2270 |
| **Mold Compound Flammability Rating:** | V-O per UL94 |
| **Oxygen Rating Index:** | N/A |
| **Substrate Material:** | CCL-HL832NX |
| **Lead Finish, Composition / Thickness:** | SnAgCu |
| **Die Backside Preparation Method/Metallization:** | Backgrind |
| **Die Separation Method:** | 100% |
| **Die Attach Supplier:** | Ablestik |
| **Die Attach Material:** | 2025D |
| **Die Attach Method:** | Epoxy |
| **Bond Diagram Designation:** | 001-08055 |
| **Wire Bond Method:** | Thermosonic |
| **Wire Material/Size:** | Au, 0.8mil |
| **Thermal Resistance Theta JA and JC °C/W:** | 44.21 , 19 |
| **Package Cross Section Yes/No:** | N/A |
| **Assembly Process Flow:** | 001-06964 |
| **Name/Location of Assembly (prime) facility:** | ASE Taiwan (TAIWN-G) |

| ELECTRICAL TEST / FINISH DESCRIPTION | |
|---|---|
| **Test Location:** | CML-R |
| **Fault Coverage:** | 100% |

**Note:** Please contact a Cypress Representative for other packages availability.

## RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

| Stress/Test | Test Condition (Temp/Bias) | Result P/F |
|---|---|---|
| Alpha Particle Emission | 0.001 CPH/$Cm^2$ | P |
| Data Retention (Hermetic) | 250 C, non-biased | P |
| Data Retention (Plastic) | 150 C, non-biased | P |
| Electrostatic Discharge Charge Device Model (ESD-CDM) | 500V<br>Cypress Spec. 25-00020 | P |
| Electrostatic Discharge Human Body Model (ESD-HBM) | 2,200V MIL-STD-883, Method 3015<br>JESD22, Method A114-B | P |
| High Accelerated Saturation Test (HAST) | 140°C, 3.63V, 85%RH<br>Precondition: JESD22 Moisture Sensitivity MSL 3<br>192 Hrs, 30°C/60%RH+3IR-Reflow, 260°C+0, -5°C | P |
| High Temperature Operating Life Early Failure Rate | Dynamic Operating Condition, Vcc Max = 3.45V, 125°C<br>Dynamic Operating Condition, Vcc Max = 3.45V, 150°C<br>Dynamic Operating Condition, Vcc Max = 3.8V, 150°C | P |
| High Temperature Operating Life Latent Failure Rate | Dynamic Operating Condition, Vcc Max = 3.45V, 125°C<br>Dynamic Operating Condition, Vcc Max = 3.45V, 150°C<br>Dynamic Operating Condition, Vcc Max = 3.8V, 150°C | P |
| High Temperature Steady State Life | Static Operating Condition, Vcc Max = 3.63V, 150°C | P |
| High Temperature Storage | 165C, no bias | P |
| Long Life Verification | Dynamic Operating Condition, Vcc Max = 3.8V, 150°C | P |
| Low Temperature Operating Life | -30C, 3.8V, 8 MHz | P |
| Pressure Cooker | 121°C, 100%RH<br>Precondition: JESD22 Moisture Sensitivity MSL 3<br>192 Hrs, 30°C/60%RH+3IR-Reflow, 260°C+0, -5°C | P |
| Static Latch-up | 125C, ± 200mA<br>In accordance with JEDEC 17. Cypress Spec. 01-00081 | P |
| Temperature Cycle | MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C<br>Precondition: JESD22 Moisture Sensitivity MSL 3<br>192 Hrs, 30°C/60%RH+3IR-Reflow, 260°C+0, -5°C | P |
| Thermal Series | MIL-STD-883-5005, D3 | P |

## RELIABILITY FAILURE RATE SUMMARY

| Stress/Test | Device Tested/ Device Hours | # Fails | Activation Energy | Acceleration Factor[3] | Failure Rate |
|---|---|---|---|---|---|
| High Temperature Operating Life Early Failure Rate | 1078 Devices | 0 | N/A | N/A | 0 PPM |
| High Temperature Operating Life[1,2] Long Term Failure Rate | 400,500 HRs | 1 | 0.7 | 170 | 30 FITs |

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[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

$E_A$ =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = $8.62 \times 10^{-5}$ eV/Kelvin.
$T_1$ is the junction temperature of the device under stress and $T_2$ is the junction temperature of the device at use conditions.

# Reliability Test Data

**QTP #: 99075**

| Device | Fab Lot # | Assy Lot # | Assy Loc | Duration | Samp | Rej | Failure Mechanism |
|---|---|---|---|---|---|---|---|
| ***STRESS: ESD-CHARGE DEVICE MODEL, 500V*** | | | | | | | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | COMP | 3 | 0 | |
| CY62137V-ZSIB | 4851023 | 619907600 | CSPI-R | COMP | 3 | 0 | |
| ***STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V, >Vcc Max)*** | | | | | | | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 48 | 1505 | 0 | |
| CY62137V-ZSIB | 4902501 | 619905577 | CSPI-R | 48 | 1504 | 0 | |
| ***STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V, >Vcc Max)*** | | | | | | | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 80 | 405 | 0 | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 500 | 405 | 1 | UNKNOWN |
| CY62137V-ZSIB | 4902501 | 619905577 | CSPI-R | 80 | 396 | 0 | |
| CY62137V-ZSIB | 4902501 | 619905577 | CSPI-R | 500 | 396 | 0 | |
| ***STRESS: LONG LIFE VERIFICATION, (150C, 3.8V, >Vcc Max)*** | | | | | | | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 1000 | 404 | 0 | |
| ***STRESS: HIGH TEMP DYNAMIC STEADY STATE LIFE TEST, (150C, 3.63V, >Vcc Max)*** | | | | | | | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 80 | 80 | 0 | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 168 | 80 | 0 | |
| ***STRESS: LOW TEMPERATURE OPERATING LIFE, (-30C, 3.8V, 8 MHZ)*** | | | | | | | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 500 | 45 | 0 | |
| ***STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2,200V*** | | | | | | | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | COMP | 3 | 0 | |
| CY62137V-ZSIB | 4851023 | 619907600 | CSPI-R | COMP | 3 | 0 | |
| ***STRESS: HIGH TEMPERATURE STORAGE, 165C, no bias*** | | | | | | | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 336 | 47 | 0 | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 1000 | 47 | 0 | |
| CY62137V-ZSIB | 4902501 | 619905577 | CSPI-R | 336 | 48 | 0 | |
| ***STRESS: TC CONDITION C, -65C TO 150C, PRE COND 192 HRS 30C/60% RH, MSL3*** | | | | | | | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 300 | 48 | 0 | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 1000 | 48 | 0 | |
| CY62137V-ZSIB | 4902501 | 619905577 | CSPI-R | 300 | 48 | 0 | |
| CY62137V-ZSIB | 4902501 | 619905577 | CSPI-R | 1000 | 48 | 0 | |

# Reliability Test Data

**QTP #: 99075**

| Device | Fab Lot # | Assy Lot # | Assy Loc | Duration | Samp | Rej | Failure Mechanism |
|---|---|---|---|---|---|---|---|
| ***STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE COND 192HRS 30C/60%RH, MSL3*** | | | | | | | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 168 | 48 | 0 | |
| ***STRESS: HI-ACCEL SATURATION TEST, (140C, 3.63V), 85%RH, PRE COND 192 HR 30C/60%RH, MSL3*** | | | | | | | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 128 | 48 | 0 | |
| CY62137V-ZSIB | 4852210 | 619903364 | CSPI-R | 256 | 48 | 0 | |
| CY62137V-ZSIB | 4902501 | 619905577 | CSPI-R | 128 | 48 | 0 | |
| CY62137V-ZSIB | 4902501 | 619905577 | CSPI-R | 256 | 48 | 0 | |
| CY62137V-ZSIB | 4903568 | 619907944 | CSPI-R | 128 | 48 | 0 | |

# Reliability Test Data

## QTP #: 052103

| Device | Fab Lot # | Assy Lot # | Assy Loc | Duration | Samp | Rej | Failure Mechanism |
|---|---|---|---|---|---|---|---|
| ***STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 3.45V, Vcc Max*** | | | | | | | |
| CYDC256B16 (7C02628A) | 4531145 | 610540035 | TAIWN-G | 48 | 330 | 0 | |
| CYDC256B16 (7C02628A) | 4531145 | 610540036 | TAIWN-G | 48 | 328 | 0 | |
| CYDC256B16 (7C02628A) | 4531145 | 610540037 | TAIWN-G | 48 | 332 | 0 | |
| ***STRESS: ESD-CHARGE DEVICE MODEL, 500V*** | | | | | | | |
| CYDM256B16 (7C02628A) | 4531145 | 610539449 | TAIWN-G | COMP | 9 | 0 | |
| CYDC256B16 (7C02628A) | 4531145 | 610540035/6/7 | TAIWN-G | COMP | 9 | 0 | |
| ***STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2,200V*** | | | | | | | |
| CYDM256B16 (7C02628A) | 4531145 | 610539449 | TAIWN-G | COMP | 9 | 0 | |
| CYDC256B16 (7C02628A) | 4531145 | 610540035/6/7 | TAIWN-G | COMP | 9 | 0 | |
| ***STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V*** | | | | | | | |
| CYDM256B16 (7C02628A) | 4531145 | 610539449 | TAIWN-G | COMP | 3 | 0 | |
| CYDC256B16 (7C02628A) | 4531145 | 610540035/6/7 | TAIWN-G | COMP | 3 | 0 | |
| ***STRESS: STATIC LATCH-UP TESTING (125C, 7.0V, +/-300mA)*** | | | | | | | |
| CYDM256B16 (7C02628A) | 4531145 | 610539449 | TAIWN-G | COMP | 3 | 0 | |
| ***STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3*** | | | | | | | |
| CYDM256A16 (7C02618A) | 4503160 | 610510254 | TAIWN-G | 168 | 50 | 0 | |
| ***STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3*** | | | | | | | |
| CYDM256A16 (7C02618A) | 4503160 | 610510254 | TAIWN-G | 300 | 50 | 0 | |
| CYDM256A16 (7C02618A) | 4503160 | 610510254 | TAIWN-G | 500 | 50 | 0 | |
| CYDM256A16 (7C02618A) | 4503160 | 610510254 | TAIWN-G | 1000 | 50 | 0 | |

# Reliability Test Data

## QTP #: 062201

| Device | Fab Lot # | Assy Lot # | Assy Loc | Duration | Samp | Rej | Failure Mechanism |
|---|---|---|---|---|---|---|---|
| ***STRESS: ALPHA PARTICLE EMISSION*** | | | | | | | |
| CYDC256B16 (7C02628A) | 4522569 | 610543349 | TAIWN-G | COMP | 5 | 0 | |
| ***STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 3.45V, Vcc Max*** | | | | | | | |
| CYDCX256A16 (7C02638A) | 4622252 | 610647256 | CML-R | 48 | 485 | 0 | |
| CYDCX256A16 (7C02638A) | 4622252 | 610647257 | CML-R | 48 | 400 | 0 | |
| ***STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 3.45V, Vcc Max*** | | | | | | | |
| CYDMX256A16 (7C02638A) | 4622252 | 610646577 | TAIWN-G | 96 | 193 | 0 | |
| ***STRESS: ESD-CHARGE DEVICE MODEL, 500V*** | | | | | | | |
| CYDMX256A16 (7C02638A) | 4622252 | 610646577 | TAIWN-G | COMP | 9 | 0 | |
| ***STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2,200V*** | | | | | | | |
| CYDMX256A16 (7C02638A) | 4622252 | 610646577 | TAIWN-G | COMP | 9 | 0 | |
| ***STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V*** | | | | | | | |
| CYDMX256A16 (7C02638A) | 4622252 | 610646577 | TAIWN-G | COMP | 3 | 0 | |
| ***STRESS: STATIC LATCH-UP TESTING (125C, 5.4V, +/-200mA)*** | | | | | | | |
| CYDMX256A16 (7C02638A) | 4622252 | 610646577 | TAIWN-G | COMP | 3 | 0 | |
| ***STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3*** | | | | | | | |
| CYDM256A16 (7C02618A) | 4503160 | 610510254 | TAIWN-G | 168 | 50 | 0 | |
| ***STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3*** | | | | | | | |
| CYDM256A16 (7C02618A) | 4503160 | 610510254 | TAIWN-G | 300 | 50 | 0 | |
| CYDM256A16 (7C02618A) | 4503160 | 610510254 | TAIWN-G | 500 | 50 | 0 | |
| CYDM256A16 (7C02618A) | 4503160 | 610510254 | TAIWN-G | 1000 | 50 | 0 | |

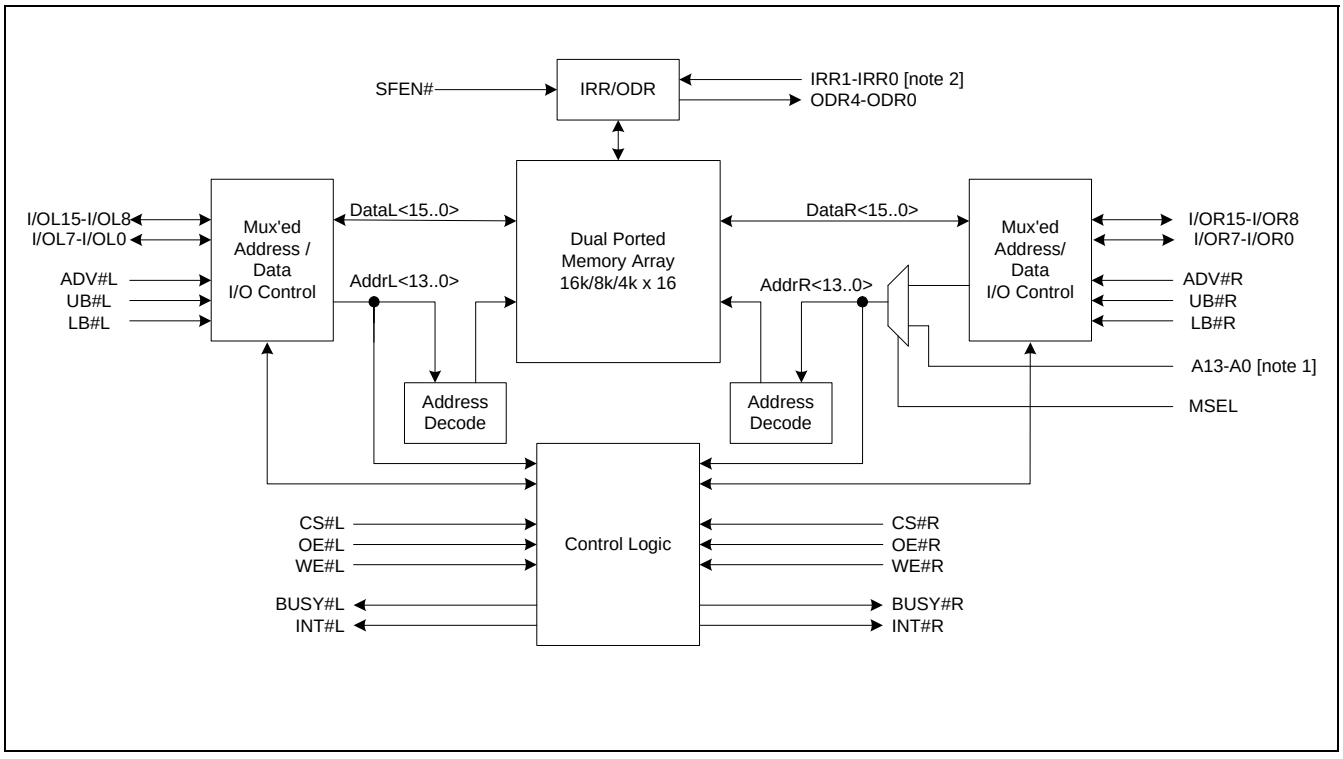
**CYDMX256A16**
**CYDMX128A16**
**CYDMX064A16**

# 16k/8k/4k x 16 MoBL® ADM Asynchronous Dual-Port Static RAM

## Features

- True dual-ported memory block that allow simultaneous access
  - — One port with dedicated time-multiplexed address/data (ADM) interface
  - — One port configurable to standard SRAM or time-multiplexed address/data interface
- 16k/8k/4k × 16 memory configuration
- High-speed access
  - — 65 ns or 90 ns ADM interface
  - — 40 ns or 60 ns standard SRAM interface
- Fully asynchronous operation
- Port-independent 1.8V, 2.5V, and 3.0V I/Os
- Ultra Low operating power
  - — Active: $I_{CC}$ = 15 mA (typical) at 90 ns
  - — Active: $I_{CC}$ = 25 mA (typical) at 65 ns
  - — Standby: $I_{SB3}$ = 2 μA (typical)
- Port-independent power-down
- On-chip arbitration logic
- Mailbox interrupt for port-to-port communication
- Input Read/Output Drive Registers
- Upper-byte and lower-byte control
- Small Package: 6x6 mm, 100-ball Pb-free BGA
- Industrial temperature range

**Figure 1. Top Level Block Diagram**




**Notes**
1. A13-A0 for CYDMX256A16; A12-A0 for CYDMX128A16 and A11-A0 for CYDMX064A16.
2. IRR1 and IRR2 not available for CYDMX256A16.

## Pin Configurations

**100-Ball 0.5-mm Pitch BGA**
**Top View**
**CYDMX256A16/CYDMX128A16/CYDM064A16**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | A5 | A8 | A11 | UB#R | VSS | ADV#R | I/OR15 | I/OR12 | I/OR10 | VSS | A |
| B | A3 | A4 | A7 | A9 | CE#R | WE#R | OE#R | VDDIOR | I/OR9 | I/OR6 | B |
| C | A0 | A1 | A2 | A6 | LB#R | IRR1[3] | I/OR14 | I/OR11 | I/OR7 | VSS | C |
| D | ODR4 | ODR2 | BUSY#R | INT#R | A10 | A12[4] | I/OR13 | I/OR8 | I/OR5 | I/O2R | D |
| E | VSS | DNU | ODR3 | INT#L | VSS | VSS | I/OR4 | VDDIOR | I/OR1 | VSS | E |
| F | SFEN# | ODR1 | BUSY#L | DNU | VCC | VSS | I/OR3 | I/OR0 | I/OL15 | VDDIOL | F |
| G | ODR0 | DNU | DNU | DNU | OE#L | I/OL3 | I/OL11 | I/OL12 | I/OL14 | I/OL13 | G |
| H | DNU | DNU | DNU | LB#L | CE#L | I/OL1 | VDDIOL | MSEL | DNU | I/OL10 | H |
| J | DNU | DNU | DNU | IRR0[5] | VCC | VSS | I/OL4 | I/OL6 | I/OL8 | I/OL9 | J |
| K | DNU | DNU | DNU | UB#L | ADV#L | WE#L | I/OL0 | I/OL2 | I/OL5 | I/OL7 | K |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |

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**Notes**
3. This pin is A13 for CYDMX256A16.
4. This pin is DNU for CYDMX064A16.
5. This pin is DNU for CYDMX256A16.
6. DNU pins are “do not use” pins. No trace or power component can be connected to these pins.

## Pin Definitions

| Left Port | Right Port | Description |
|---|---|---|
| CS#L | CS#R | **Chip Select** |
| WE#L | WE#R | **Read/Write Enable** |
| OE#L | OE#R | **Output Enable** |
| | A0–A13 | **Address (A0–A11 for 4k device; A0–A12 for 8k device; A0–A13 for 16k device)** |
| | MSEL | **Right Port Interface Mode Select (0: Standard SRAM; 1: Address/Data Mux)** |
| I/OL0–I/OL15 | I/OR0–I/OR15 | **Address/Data Bus Input/Output** |
| ADV#L | ADV#R | **Address Latch Enable; ADV#R only use when R-port is in ADM mode** |
| UB#L | UB#R | **Upper Byte Select (I/O8–I/O15)** |
| LB#L | LB#R | **Lower Byte Select (I/O0–I/O7)** |
| INT#L | INT#R | **Interrupt Flag** |
| BUSY#L | BUSY#R | **Busy Flag** |
| SFEN# | | **Special Function Enable Signal** |
| IRR0-IRR1 | | **Input Signals for Input Read Registers for CYDM128A16 and CYDMX064A16; IRR0 is DNU and IRR1 is A13 for CYDMX256A16** |
| ODR0-ODR4 | | **Output Signals for Output Drive Registers; These are open-drained outputs.** |
| VCC | | **Core Power Supply** |
| GND | | **Ground** |
| VDDIOL | | **Left Port I/O Power Supply** |
| VDDIOR | | **Right Port I/O Power Supply** |
| DNU | | **No Connect; Do not connect trace or power component to these pins.** |

## Functional Description

The CYDMX256A16, CYDMX128A16 and CYDMX064A16 are low-power CMOS 16k/8k/4k x 16 dual-port static RAMs. The two ports are: one dedicated time-multiplexed address and data (ADM) interface and one configurable standard SRAM or ADM interface. The two ports permit independent, asynchronous read and write access to any memory locations. Each port has independent control pins: Chip Select (CS#), Write Enable (WE#), and Output Enable (OE#). Two output flags are provided on each port (BUSY# and INT#). BUSY# flag is triggered when the port is trying to access the same memory location currently being accessed by the other port. The Interrupt flag (INT#) permits communication between ports or systems by means of a mailbox. Power-down feature is controlled independently on each port by a Chip Select (CS#) pin.

The CYDMX256A16, CYDMX128A16 and CYDMX064A16 are available in 100-ball 0.5-mm pitch Ball Grid Array (BGA) packages. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

### Power Supply

The core voltage ($V_{CC}$) can be 1.8V, 2.5V or 3.0V, as long as it is lower than or equal to the I/O voltage. Each port can operate on independent I/O voltages. This is determined by what is connected to the $V_{DDIOL}$ and $V_{DDIOR}$ pins. The supported I/O standards are 1.8V/2.5V LVCMOS and 3.0V LVTTL.

### ADM Interface Read/Write Operation

The description of this section is applicable to both the left ADM port and right port configured as an ADM port.

Three control signals, ADV#, WE# and CS# are used to perform the read/write operation. Address signals are first applied to the I/O bus along with CS# LOW. The addresses are loaded from the I/O bus in response to the rising edge of the Address Latch Enable (ADV#) signal. It is necessary to meet the set-up ($t_{AVDS}$) and hold ($t_{AVDH}$) times given in the AC specifications with valid address information in order to properly latch the addresses.

Once the address signals are latched in, a read operation is issued when WE# stays HIGH. The I/O bus becomes HIGH-Z once the address signals meet $t_{AVDH}$. The read data is driven on the I/O bus $t_{OE}$ after the OE# is asserted LOW, and held until $t_{HZOE}$ or $t_{HZCS}$ after the rising edge of OE# or CS#, whichever comes first.

A write operation is issued when WE# is asserted LOW. The write data is applied to the I/O bus right after address meets the hold time ($t_{AVDH}$). And write data is written with the rising edge of either WE# or CS#, whichever comes first, and meets data set-up ($t_{SD}$) and hold ($t_{HD}$) times.

### Standard SRAM Interface Read/Write Operation

The description of this section is applicable to the right access port configured as standard SRAM port. Read/write operation with standard SRAM interface configuration is the same as the ADM port except addresses are presented on the A bus. Operation is controlled by CS#, OE# and WE#. A read operation is issued when WE# is asserted HIGH. A write operation is issued when WE# is asserted LOW. The I/O bus is the destination for read data and the source for write data when the read operation is issued. However, write data needs to be driven to I/O when the write operation is issued.

### Byte Select Operation

The fundamental word size is 16 bits. Each word is broken up into two 8-bit bytes. Each port has two active-LOW byte enables: UB# and LB#. Activating or deactivating the byte enables alters the result of read and write operations to the port. During a write, byte enable asserted HIGH inhibits the corresponding byte to be updated in the addressed memory location. During a read, both byte enables are inputs to the asynchronous output enable control logic. When a byte enable is asserted HIGH, the corresponding data byte is tri-stated. Subsequently, when the byte enable is asserted LOW, the corresponding data byte is driven with the read data.

### Chip Select Operation

Each port has one active-LOW chip select signal, CS#. CS# must be asserted LOW for the port to be considered active. In order to issue a valid read or write operation, the chip select input must be asserted LOW throughout the read or write cycle. When CS# is deasserted HIGH during a write, if $t_{WRL}$, $t_{SD}$ and $t_{HD}$ are not met and the contents of the addressed location is not altered.

An automatic power-down feature controlled by deactivating the chip select (CS# HIGH) permits the on-chip circuitry of each port to enter a very low standby power mode.

### Output Enable Operation

Each port has one output enable signal, OE#. When OE# is asserted HIGH, I/O bus is tri-stated after $t_{HZOE}$. When OE# is asserted LOW, control of the I/O bus is assumed by the asynchronous output enable logic (the logic is controlled by inputs WE#, CS#, UB#, LB#).

### Mailbox Interrupts

The upper two memory locations may be used for message passing. The highest memory location (0xFFF for the CYDMX064A16, 0x1FFF for the CYDMX128A16, and 0x3FFF for CYDMX256A16) is the mailbox for the right port. The second-highest memory location (0xFFE for the CYDMX064A16, 0x1FFE for the CYDMX128A16, and 0x3FFE for CYDMX256A16) is the mailbox for the left port. When one port writes to the opposite port's mailbox, an interrupt signal is generated to the opposite port. The interrupt resets when the owner reads the contents of its own mailbox. The message written to the mailbox is user-defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

On power-up, both interrupts are set by default. An initialization program must be run to reset the interrupts.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

### Arbitration Logic

The CYDMX256A16, CYDMX128A16 and CYDMX064A16 provide on-chip arbitration to resolve simultaneous memory location access (collision). If both ports' CS# signals are asserted and an address match occurs within of each other, the busy logic determines which port has access. If $t_{PS}$ is violated, one of the two ports gains permission to the location, but it is not predictable which port gets the permission. BUSY# is asserted $t_{BLA}$ after an address match or $t_{BLC}$ after CS# is taken LOW.

### Input Read Register

The Input Read Register feature is only available for CYDMX128A16 and CYDMX064A16 devices. When SFEN# = $V_{IL}$, the Input Read Register (IRR) captures the status of two external devices connected to the Input Read pins (IRR0 and IRR1) to address location 0x0000. Address 0x0000 is not available for standard memory accesses when SFEN# = $V_{IL}$. When SFEN# = $V_{IH}$, address 0x0000 is available for normal memory accesses. Either port accesses the contents of IRR with normal read operation from address 0x0000. During reads from the IRR, I/O<1:0> are valid bits and I/O<15:2> are don't care. The IRR inputs will be 1.8V/2.5V LVCMOS or 3.0V LVTTL, depending on the core voltage supply ($V_{CC}$).

### Output Drive Register

The Output Drive Register (ODR) determines the state of up to five external binary state devices by providing a path to $V_{SS}$ for the external circuit. These outputs are Open Drain. The five external devices can operate at different voltages ($1.5V \le V_{DDIO} \le 3.5V$) but the combined current cannot exceed 40 mA (8 mA max for each external device). The status of the ODR bits are set using standard write accesses from either port to address 0x0001 with a '1' corresponding to on and '0' corresponding to off. The status of the ODR bits are read with a normal read access to address 0x0001. When SFEN# = $V_{IL}$, the ODR is active and address 0x0001 is not available for memory accesses. When SFEN# = $V_{IH}$, the ODR is inactive and address 0x0001 is used for standard accesses. During reads and writes to ODR, I/O<4:0> are valid and I/O<15:5> are don't care.

## Architecture

The CYDMX256A16, CYDMX128A16, and CYDMX064A16 consist of an array of 16k, 8k and 4k words of 16 dual-ported SRAM cells, I/O, address lines, and control signals (CS#, ADV#, OE# and WE#). Between the two access ports, one is a dedicated time-multiplexed address/data interface; the other is a pin selectable port to either standard SRAM or time-multiplexed address/data interface. Independent control signals for each port permit simultaneous access to any location in memory. To handle the situation of writing/reading to the same location, a BUSY# pin is provided on each port. For port-to-port communication, an Interrupt (INT#) pin is also available on each port.

**Table 1. ADM Interface Read/Write with Byte Select Operations**

| ADV# | CS# | WE# | OE# | UB# | LB# | I/O0 - I/O15 | Mode |
|---|---|---|---|---|---|---|---|
| X | H | X | X | X | X | High-Z | Deselected/Power down |
| X | X | X | H | X | X | High-Z | Output Disable |
| X | X | X | X | H | H | High-Z | Upper and lower byte deselected |
| Pulse | L | H | L | L | L | Data Out (I/O0-I/O15) | Read upper and lower bytes |
| Pulse | L | H | L | H | L | Data Out (I/O0-I/O7) High-Z (I/O8-I/O15) | Read lower byte only |
| Pulse | L | H | L | L | H | High-Z (I/O0-I/O7) Data Out (I/O8-I/O15) | Read upper byte only |
| Pulse | L | L | X | L | L | Data In (I/O0-I/O15) | Write upper and lower bytes |
| Pulse | L | L | X | H | L | Data In (I/O0-I/O7) High-Z (I/O8-I/O15) | Write lower byte only |
| Pulse | L | L | X | L | H | High-Z (I/O0-I/O7) Data In (I/O8-I/O15) | Write upper byte only |

**Table 2. Standard SRAM Interface Read/Write with Byte Select Operations**

| CS# | WE# | OE# | UB# | LB# | I/O0-I/O15 | Mode |
|---|---|---|---|---|---|---|
| H | X | X | X | X | High-Z | Deselected/Power down |
| X | X | H | X | X | High-Z | Output Disable |
| X | X | X | H | H | High-Z | Upper and lower byte deselected |
| L | H | L | L | L | Data Out (I/O0-I/O15) | Read upper and lower bytes |
| L | H | L | H | L | Data Out (I/O0-I/O7) High-Z (I/O8-I/O15) | Read lower byte only |
| L | H | L | L | H | High-Z (I/O0-I/O7) Data Out (I/O8-I/O15) | Read upper byte only |
| L | L | X | L | L | Data In (I/O0-I/O15) | Write upper and lower bytes |
| L | L | X | H | L | Data In (I/O0-I/O7) High-Z (I/O8-I/O15) | Write lower byte only |
| L | L | X | L | H | High-Z (I/O0-I/O7) Data In (I/O8-I/O15) | Write upper byte only |

**Table 3. Interrupt Operation Example (Assumes BUSY#L = BUSY#R = HIGH)**

| Function | Left Port | | | | | Right Port | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | WE#L | CS#L | OE#L | AddressL | INT#L | WE#R | CS#R | OE#R | AddressR | INT#R |
| Set Right INT#R Flag | L | L | X | 0x3FFF[7] | X | X | X | X | X | L |
| Reset Right INT#R Flag | X | X | X | X | X | X | L | L | 0x3FFF[7] | H |
| Set Left INT#L Flag | X | X | X | X | L | L | L | X | 0x3FFE[8] | X |
| Reset Left INT#L Flag | X | L | L | 0x3FFE[8] | H | X | X | X | X | X |

**Notes**
7. 0x3FFF for CYDMX256A16, 0x1FFF for CYDMX128A16, 0xFFF for CYDMX064A16.
8. 0x3FFE for CYDMX256A16, 0x1FFE for CYDMX128A16, 0xFFE for CYDMX064A16.

**Table 4. Arbitration Winning Port**

| CS#L | CS#R | Address Match Left/Right Port | BUSY#L | BUSY#R | Function |
|---|---|---|---|---|---|
| X | X | No Match | H | H | Normal |
| H | X | Match | H | H | Normal |
| X | H | Match | H | H | Normal |
| L | L | Match | See Note[9] | See Note[9] | Write Inhibit[10] |

**Table 5. Input Read Register Operation**[11]

| SFEN# | CS# | WE# | OE# | UB# | LB# | ADDR | $I/O_0$–$I/O_1$ | $I/O_2$–$I/O_{15}$ | Mode |
|---|---|---|---|---|---|---|---|---|---|
| H | L | H | L | L | L | x0000-Max | VALID[12] | VALID[12] | Standard Memory Access |
| L | L | H | L | X | L | x0000 | VALID[13] | X | IRR Read |

**Table 6. Output Drive Register**[15]

| SFEN# | CS# | WE# | OE# | UB# | LB# | ADDR | $I/O_0$–$I/O_4$ | $I/O_5$–$I/O_{15}$ | Mode |
|---|---|---|---|---|---|---|---|---|---|
| H | L | H | X[16] | L[12] | L[12] | x0000-Max | VALID[12] | VALID[12] | Standard Memory Access |
| L | L | L | X | X | L | x0001 | VALID[13] | X | ODR Write[17] |
| L | L | H | L | X | L | x0001 | VALID[13] | X | ODR Read |

**Notes**
9. If it meets tPS, "L" if the CS# and address of the opposite port become stable BEFORE the current port; "H" if the CS# and address of the opposite port become stable AFTER the current port. If tPS is not met, either BUSY#L or BUSY#R will result “L”. BUSY#L and BUSY#R can not be “L” simultaneously.
10. Write operations to the left port are internally ignored when BUSY#L is driving LOW regardless of actual logic level on the pin; Write operations to the right port are internally ignored when BUSY#R is driving LOW regardless of actual logic level on the pin.
11. SFEN# = VIL for IRR reads
12. UB# or LB# = VIL. If LB# = VIL, then I/O<7:0> are valid. If UB# = VIL then I/O<15:8> are valid.
13. LB# must be active (LB# = VIL) for these bits to be valid.
14. SFEN# active when either CS#L = VIL or CS#R = VIL. It is inactive when CS#L = CS#R = VIH.
15. SFEN# = VIL for ODR reads and writes.
16. Output enable must be low (OE# = VIL) during reads for valid data to be output.
17. During ODR writes data will also be written to the memory.

## Maximum Ratings[18]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +3.3V

DC Voltage Applied to Outputs in High-Z State..... –0.5V to $V_{CC}$ + 0.5V

DC Input Voltage[19]..... –0.5V to $V_{CC}$ + 0.5V

Output Current into Outputs (LOW)..... 90 mA

Static Discharge Voltage..... > 2000V

Latch-up Current..... > 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Industrial | –40°C to +85°C | 1.8V ± 100 mV<br>2.5V ± 100 mV<br>3.0V ± 300 mV |

## Electrical Characteristics for $V_{CC}$ = 1.8V Over the Operating Range

| Parameter | Description | P1 I/O Voltage | P2 I/O Voltage | CYDMX256A16 CYDMX128A16 CYDMX064A16 –65 Min. | Typ. | Max. | CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage ($I_{OH}$ = –100 µA) | 1.8V (any port) | | $V_{DDIO}$ – 0.2 | | | $V_{DDIO}$ – 0.2 | | | V |
| | Output HIGH Voltage ($I_{OH}$ = –2 mA) | 2.5V (any port) | | 2.0 | | | 2.0 | | | V |
| | Output HIGH Voltage ($I_{OH}$ = –2 mA) | 3.0V (any port) | | 2.1 | | | 2.1 | | | V |
| $V_{OL}$ | Output LOW Voltage ($I_{OL}$ = 100 µA) | 1.8V (any port) | | | | 0.2 | | | 0.2 | V |
| | Output HIGH Voltage ($I_{OH}$ = 2 mA) | 2.5V (any port) | | | | 0.4 | | | 0.4 | V |
| | Output HIGH Voltage ($I_{OH}$ = 2 mA) | 3.0V (any port) | | | | 0.4 | | | 0.4 | V |
| $V_{OL}$ ODR | ODR Output LOW Voltage ($I_{OL}$ = 8 mA) | 1.8V (any port) | | | | 0.2 | | | 0.2 | V |
| | | 2.5V (any port) | | | | 0.2 | | | 0.2 | V |
| | | 3.0V (any port) | | | | 0.2 | | | 0.2 | V |
| $V_{IH}$ | Input HIGH Voltage | 1.8V (any port) | | 1.2 | | $V_{DDIO}$ + 0.2 | 1.2 | | $V_{DDIO}$ + 0.2 | V |
| | | 2.5V (any port) | | 1.7 | | $V_{DDIO}$ + 0.3 | 1.7 | | $V_{DDIO}$ + 0.3 | V |
| | | 3.0V (any port) | | 2.0 | | $V_{DDIO}$ + 0.2 | 2.0 | | $V_{DDIO}$ + 0.2 | V |
| $V_{IL}$ | Input LOW Voltage | 1.8V (any port) | | –0.2 | | 0.4 | –0.2 | | 0.4 | V |
| | | 2.5V (any port) | | –0.3 | | 0.6 | –0.3 | | 0.6 | V |
| | | 3.0V (any port) | | –0.2 | | 0.7 | –0.2 | | 0.7 | V |
| $I_{OZ}$ | Output Leakage Current | 1.8V | 1.8V | –1 | | 1 | –1 | | 1 | µA |
| | | 2.5V | 2.5V | –1 | | 1 | –1 | | 1 | µA |
| | | 3.0V | 3.0V | –1 | | 1 | –1 | | 1 | µA |
| $I_{CEX}$ ODR | ODR Output Leakage Current. $V_{OUT}$ = $V_{DDIO}$ | 1.8V | 1.8V | –1 | | 1 | –1 | | 1 | µA |
| | | 2.5V | 2.5V | –1 | | 1 | –1 | | 1 | µA |
| | | 3.0V | 3.0V | –1 | | 1 | –1 | | 1 | µA |

**Notes**
18. The voltage on any input or I/O pin can not exceed the power pin during power-up.
19. Pulse width < 20 ns.

## Electrical Characteristics for $V_{CC}$ = 1.8V Over the Operating Range (continued)

| Parameter | Description | | P1 I/O Voltage | P2 I/O Voltage | CYDMX256A16 CYDMX128A16 CYDMX064A16 –65 Min. | –65 Typ. | –65 Max. | CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Min. | –90 Typ. | –90 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{IX}$ | Input Leakage Current | | 1.8V | 1.8V | –1 | | 1 | –1 | | 1 | µA |
| | | | 2.5V | 2.5V | –1 | | 1 | –1 | | 1 | µA |
| | | | 3.0V | 3.0V | –1 | | 1 | –1 | | 1 | µA |
| $I_{CC}$ | Operating Current ($V_{CC}$ = Max., $I_{OUT}$ = 0 mA) Outputs Disabled | Ind. | 1.8V | 1.8V | | 25 | 40 | | 15 | 25 | mA |
| $I_{SB1}$ | Standby Current (Both Ports TTL Level) CE#L and CE#R ≥ $V_{CC}$ – 0.2, f = $f_{MAX}$ | Ind. | 1.8V | 1.8V | | 2 | 6 | | 2 | 6 | µA |
| $I_{SB2}$ | Standby Current (One Port TTL Level) CE#L or CE#R ≥ $V_{IH}$, f = $f_{MAX}$ | Ind. | 1.8V | 1.8V | | 8.5 | 18 | | 8.5 | 14 | mA |
| $I_{SB3}$ | Standby Current (Both Ports CMOS Level) CE#L and CE#R ≥ $V_{CC}$ – 0.2V, f = 0 | Ind. | 1.8V | 1.8V | | 2 | 6 | | 2 | 6 | µA |
| $I_{SB4}$ | Standby Current (One Port CMOS Level) CE#L or CE#R ≥ $V_{IH}$, f = $f_{MAX}$[20] | Ind. | 1.8V | 1.8V | | 8.5 | 18 | | 8.5 | 14 | mA |

**Note**

20. $f_{MAX}$ = 1/$t_{RC}$ = All inputs cycling at f = 1/$t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby $I_{SB3}$.

## Electrical Characteristics for $V_{CC}$ = 2.5V Over the Operating Range

| Parameter | Description | | P1 I/O Voltage | P2 I/O Voltage | CYDMX256A16 CYDMX128A16 CYDMX064A16 –65 Min. | –65 Typ. | –65 Max. | CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Min. | –90 Typ. | –90 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage ($I_{OH}$ = –2 mA) | | 2.5V (any port) | | 2.0 | | | 2.0 | | | V |
| | | | 3.0V (any port) | | 2.1 | | | 2.1 | | | V |
| $V_{OL}$ | Output LOW Voltage ($I_{OL}$ = 2 mA) | | 2.5V (any port) | | | | 0.4 | | | 0.4 | V |
| | | | 3.0V (any port) | | | | 0.4 | | | 0.4 | V |
| $V_{OL}$ ODR | ODR Output LOW Voltage ($I_{OL}$ = 8 mA) | | 2.5V (any port) | | | | 0.2 | | | 0.2 | V |
| | | | 3.0V (any port) | | | | 0.2 | | | 0.2 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.5V (any port) | | 1.7 | | $V_{DDIO}$ + 0.3 | 1.7 | | $V_{DDIO}$ + 0.3 | V |
| | | | 3.0V (any port) | | 2.0 | | $V_{DDIO}$ + 0.2 | 2.0 | | $V_{DDIO}$ + 0.2 | V |
| $V_{IL}$ | Input LOW Voltage | | 2.5V (any port) | | –0.3 | | 0.6 | –0.3 | | 0.6 | V |
| | | | 3.0V (any port) | | –0.2 | | 0.7 | –0.2 | | 0.7 | V |
| $I_{OZ}$ | Output Leakage Current | | 2.5V | 2.5V | –1 | | 1 | –1 | | 1 | µA |
| | | | 3.0V | 3.0V | –1 | | 1 | –1 | | 1 | µA |
| $I_{CEX}$ ODR | ODR Output Leakage Current. $V_{OUT} = V_{CC}$ | | 2.5V | 2.5V | –1 | | 1 | –1 | | 1 | µA |
| | | | 3.0V | 3.0V | –1 | | 1 | –1 | | 1 | µA |
| $I_{IX}$ | Input Leakage Current | | 2.5V | 2.5V | –1 | | 1 | –1 | | 1 | µA |
| | | | 3.0V | 3.0V | –1 | | 1 | –1 | | 1 | µA |
| $I_{CC}$ | Operating Current ($V_{CC}$ = Max., $I_{OUT}$ = 0 mA) Outputs Disabled | Ind. | 2.5V | 2.5V | | 39 | 55 | | 28 | 40 | mA |
| $I_{SB1}$ | Standby Current (Both Ports TTL Level) CE#L and CE#R ≥ $V_{CC}$ – 0.2, f=$f_{MAX}$ | Ind. | 2.5V | 2.5V | | 6 | 8 | | 6 | 8 | µA |
| $I_{SB2}$ | Standby Current (One Port TTL Level) CE#L or CE#R ≥ $V_{IH}$, f = $f_{MAX}$ | Ind. | 2.5V | 2.5V | | 21 | 30 | | 18 | 25 | mA |
| $I_{SB3}$ | Standby Current (Both Ports CMOS Level) CE#L and CE#R ≥ $V_{CC}$ – 0.2V, f = 0 | Ind. | 2.5V | 2.5V | | 4 | 6 | | 4 | 6 | µA |
| $I_{SB4}$ | Standby Current (One Port CMOS Level) CE#L or CE#R ≥ $V_{IH}$, f = $f_{MAX}$[20] | Ind. | 2.5V | 2.5V | | 21 | 30 | | 18 | 25 | mA |

## Electrical Characteristics for 3.0V Over the Operating Range

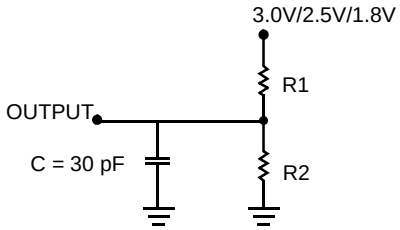
| Parameter | Description | | P1 I/O Voltage | P2 I/O Voltage | CYDMX256A16 CYDMX128A16 CYDMX064A16 –65 Min. | Typ. | Max. | CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage ($I_{OH}$ = –2 mA) | | 3.0V (any port) | | 2.1 | | | 2.1 | | | V |
| $V_{OL}$ | Output LOW Voltage ($I_{OL}$ = 2 mA) | | 3.0V (any port) | | | | 0.4 | | | 0.4 | V |
| $V_{OL}$ ODR | ODR Output LOW Voltage ($I_{OL}$ = 8 mA) | | 3.0V (any port) | | | | 0.2 | | | 0.2 | V |
| $V_{IH}$ | Input HIGH Voltage | | 3.0V (any port) | | 2.0 | | $V_{DDIO}$ + 0.2 | 2.0 | | $V_{DDIO}$ + 0.2 | V |
| $V_{IL}$ | Input LOW Voltage | | 3.0V (any port) | | –0.2 | | 0.7 | –0.2 | | 0.7 | V |
| $I_{OZ}$ | Output Leakage Current | | 3.0V | 3.0V | –1 | | 1 | –1 | | 1 | µA |
| $I_{CEX}$ ODR | ODR Output Leakage Current. $V_{OUT} = V_{CC}$ | | 3.0V | 3.0V | –1 | | 1 | –1 | | 1 | µA |
| $I_{IX}$ | Input Leakage Current | | 3.0V | 3.0V | –1 | | 1 | –1 | | 1 | µA |
| $I_{CC}$ | Operating Current ($V_{CC}$ = Max., $I_{OUT}$ = 0 mA) Outputs Disabled | Ind. | 3.0V | 3.0V | | 49 | 70 | | 42 | 60 | mA |
| $I_{SB1}$ | Standby Current (Both Ports TTL Level) CE#L and CE#R ≥ $V_{CC}$ – 0.2, f=$f_{MAX}$ | Ind. | 3.0V | 3.0V | | 7 | 10 | | 7 | 10 | µA |
| $I_{SB2}$ | | Ind. | 3.0V | 3.0V | | 28 | 40 | | 25 | 35 | mA |
| $I_{SB3}$ | Standby Current (One Port TTL Level) CE#L or CE#R ≥ $V_{IH}$, f = $f_{MAX}$ | Ind. | 3.0V | 3.0V | | 6 | 8 | | 6 | 8 | µA |
| $I_{SB4}$ | | Ind. | 3.0V | 3.0V | | 28 | 40 | | 25 | 35 | mA |

## Capacitance[22]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.0V | 9 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

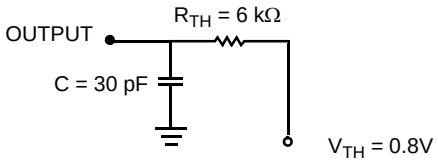
**Notes**
21. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby $I_{SB3}$.
22. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms

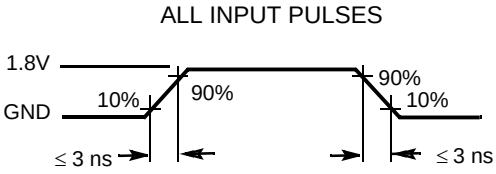


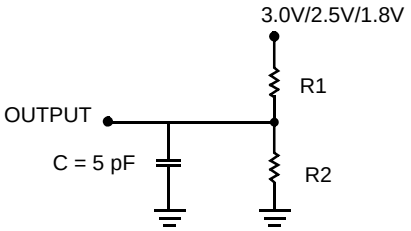

**(a) Normal Load**

| | 3.0V/2.5V | 1.8V |
|---|---|---|
| R1 | 1022Ω | 13500Ω |
| R2 | 792Ω | 10800Ω |




**(b) Thévenin Equivalent (Load 1)**




**(c) Three-State Delay (Load 2)**

(Used for $t_{LZ}$, $t_{HZ}$, $t_{HZWE}$, and $t_{LZWE}$ including scope and jig)

## Switching Characteristics for $V_{CC}$ = 1.8V Over the Operating Range [23]

| Parameter | Description | CYDMX256A16 CYDMX128A16 CYDMX064A16 –65 | | CYDMX256A16 CYDMX128A16 CYDMX064A16 –90 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **AD Mux Port Read Cycle** [25] | | | | | | |
| tRC | Read Cycle Time | 65 | | 90 | | ns |
| tACC1 | Random access ADV# Low to Data Valid | | 65 | | 90 | ns |
| tACC2 | Random access Address to Data Valid | | 65 | | 90 | ns |
| tACC3 | Random access CS# to Data Valid | | 65 | | 90 | ns |
| tAVDA | Random access ADV# High to Data Valid | | 35 | | 50 | ns |
| tAVD | ADV# Low Pulse | 15 | | 20 | | ns |
| tAVDS | Address Setup-up to ADV# rising edge | 15 | | 20 | | ns |
| tAVDH | Address Hold from ADV# rising edge | 3 | | 5 | | ns |
| tCSS | CS# Set-up to ADV# rising edge | 7 | | 10 | | ns |
| tOE | OE# Low to Data Valid | | 35 | | 50 | ns |
| tLZOE[24] | OE# Low to I/O Low-Z | 3 | | 5 | | ns |
| tHZOE | OE# High to I/O High-Z | | 15 | | 25 | |
| tHZCS | CS# High to I/O High-Z | | 15 | | 25 | ns |
| tDBE | UB#/LB# Low to I/O Valid | | 35 | | 50 | |
| tLZBE | UB#/LB# Low to I/O Low-Z | 3 | | 5 | | |

**Notes**
23. All timing parameters are measured with Load 2 specified in the AC Test Loads section.
24. This parameter is guaranteed by not tested.

## Switching Characteristics for $V_{CC}$ = 1.8V Over the Operating Range [23] (continued)

| Parameter | Description | CYDMX256A16 CYDMX128A16 CYDMX064A16 | | CYDMX256A16 CYDMX128A16 CYDMX064A16 | | Unit |
|---|---|---|---|---|---|---|
| | | –65 | | –90 | | |
| | | Min. | Max. | Min. | Max. | |
| tHZBE | UB#/LB# High to I/O High-Z | | 15 | | 25 | |
| tAVOE | ADV# High to OE# Low | 0 | | 0 | | ns |
| **AD Mux Port Write Cycle**[25] | | | | | | |
| tWC | Write Cycle Time | 65 | | 90 | | ns |
| tSCS | CS# Low to Write End | 65 | | 90 | | ns |
| tAVD | ADV# Low Pulse | 15 | | 20 | | ns |
| tAVDS | Address Set-up to ADV# rising edge | 15 | | 20 | | ns |
| tAVDH | Address Hold from ADV# rising edge | 3 | | 5 | | ns |
| tCSS | CS# Set-up to ADV# rising edge | 7 | | 10 | | ns |
| tWRL | WE# Pulse Width | 28 | | 45 | | ns |
| tBW | UB#/LB# Low to Write End | 28 | | 45 | | ns |
| tSD | Data Set-up to Write End | 20 | | 30 | | ns |
| tHD | Data Hold from Write End | 0 | | 0 | | ns |
| tLZWE | WE# High to I/O Low-Z | 0 | | 0 | | ns |
| tAVWE | ADV# High to WE# Low | 0 | | 0 | | ns |
| **Standard Port Read Cycle**[26] | | | | | | |
| tRC | Read Cycle Time | 55 | | 60 | | |
| tAA | Address to Data Valid | | 55 | | 60 | |
| tOHA | Output Hold From Address Change | 5 | | 5 | | |
| tACS | CS# to Data Valid | | 55 | | 60 | |
| tDOE | OE# Low to Data Valid | | 30 | | 35 | |
| tLZOE[24] | OE# Low to Data Low-Z | 5 | | 5 | | |
| tHZOE | OE# High to Data High-Z | | 25 | | 30 | |
| tLZCS | CS# Low to Data Low-Z | 5 | | 5 | | |
| tHZCS | CS# High to Data High-Z | | 25 | | 30 | |
| tLZBE | UB#/LB# Low to Data Low-Z | 5 | | 5 | | |
| tHZBE | UB#/LB# High to Data High-Z | | 25 | | 30 | |
| tABE | UB#/LB# Access Time | | 55 | | 60 | |
| **Standard SRAM Port Write Cycle** | | | | | | |
| tWC | Write Cycle Time | 55 | | 60 | | ns |
| tSCS | CS# Low to Write End | 45 | | 50 | | ns |
| tAW | Address Valid to Write End | 45 | | 50 | | ns |
| tHA | Address Hold from Write End | 0 | | 0 | | ns |
| tSA | Address Set-up to Write Start | 0 | | 0 | | ns |

**Notes**
25. AD Mux port timing applies to left AD Mux port and right port configured to AD Mux port.
26. Standard SRAM port timing applies to right port configured to standard SRAM port.

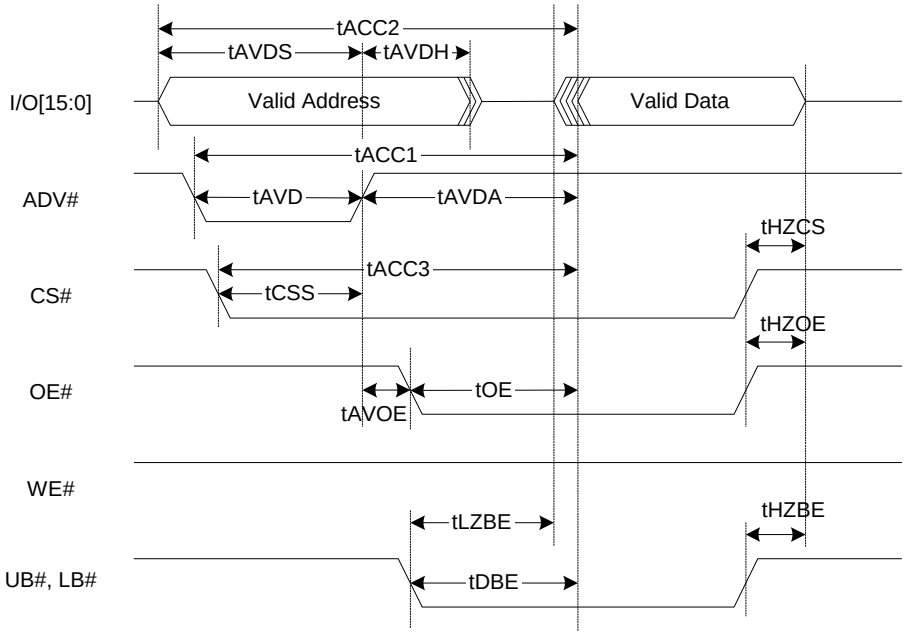
## Switching Characteristics for $V_{CC}$ = 1.8V Over the Operating Range [23] (continued)

| Parameter | Description | CYDMX256A16 CYDMX128A16 CYDMX064A16 | | CYDMX256A16 CYDMX128A16 CYDMX064A16 | | Unit |
|---|---|---|---|---|---|---|
| | | –65 | | –90 | | |
| | | Min. | Max. | Min. | Max. | |
| tWRL | Write Pulse Width | 40 | | 45 | | ns |
| tSD | Data Set-up to Write End | 30 | | 30 | | ns |
| tHD | Data Hold from Write End | 0 | | 0 | | ns |
| tHZWE | WE# Low to Data High-Z | | 25 | | 25 | ns |
| tLZWE | WE# High to Data Low-Z | 0 | | 0 | | ns |
| **Arbitration Timing** | | | | | | |
| tBLA | BUSY# Low from Address Match | | 45 | | 50 | ns |
| tBHA | BUSY# High from Address Mismatch | | 45 | | 50 | ns |
| tBLC | BUSY# Low from CS# Low | | 45 | | 50 | ns |
| tBHC | BUSY# High from CS# High | | 45 | | 50 | ns |
| tPS[27] | Port Set-Up fro Priority | 0 | | 5 | | |
| tBDD | BUSY# High to Data Valid | | 45 | | 50 | |
| tWDD | Write Pulse to Data Delay | | 80 | | 85 | |
| tDDD | Write Data Valid to Read Data Valid | | 65 | | 70 | |
| **Interrupt Timing** | | | | | | |
| tINS | INT# Set Time | | 45 | | 55 | ns |
| tINR | INT# Reset Time | | 45 | | 55 | ns |

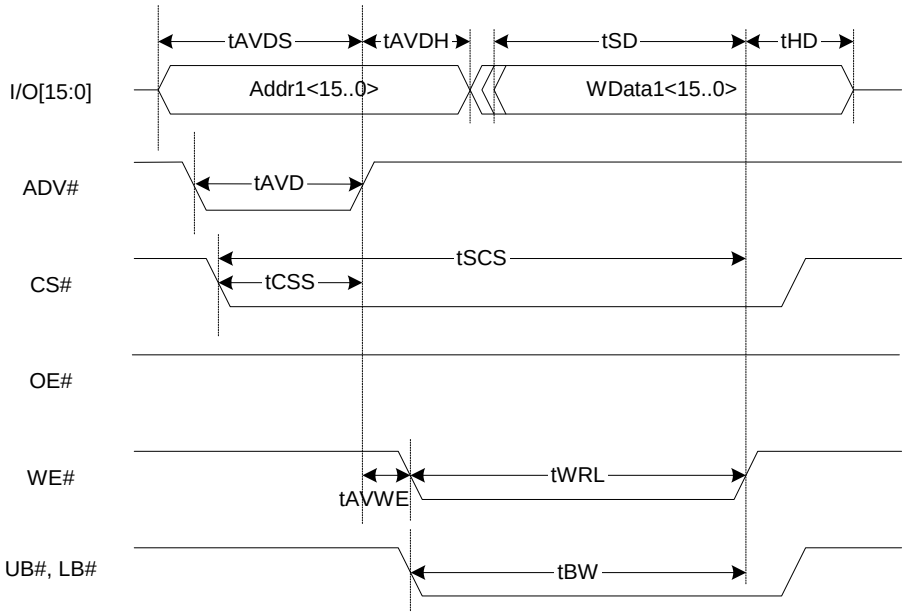
**Notes**
27. Add 2ns to this parameter if VCC and VDDIOR are <1.8V, and VDDIOL is >2.5V at temperature <0°C.

## Switching Waveforms

### ADM Port Read Cycle (Either Port Access, WE# High)

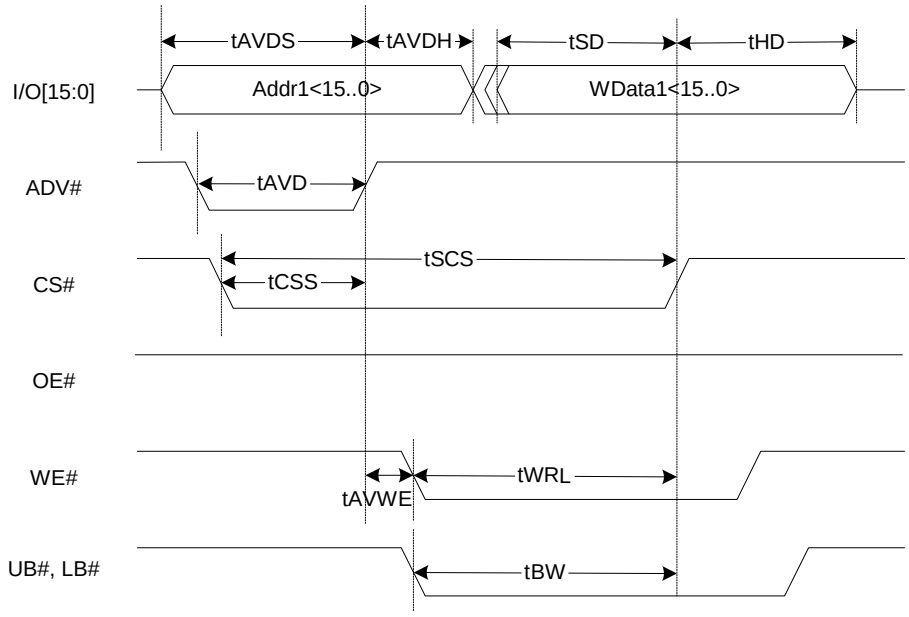



### ADM Port Write Cycle (Either Port Access, WE# Controlled, OE# High)

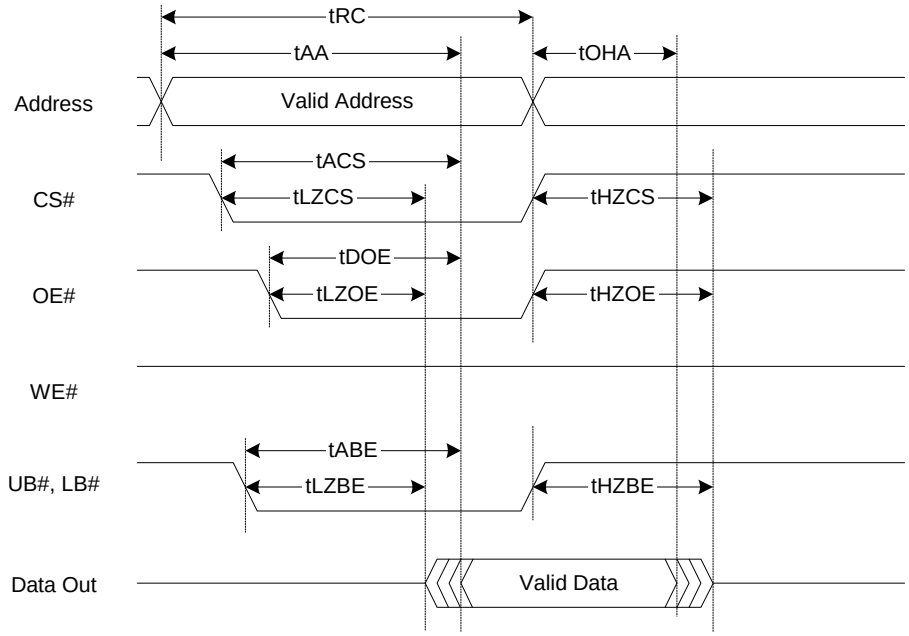


## Switching Waveforms (continued)

### ADM Port Write Cycle (Either Port Access, CS# Controlled, OE# High)

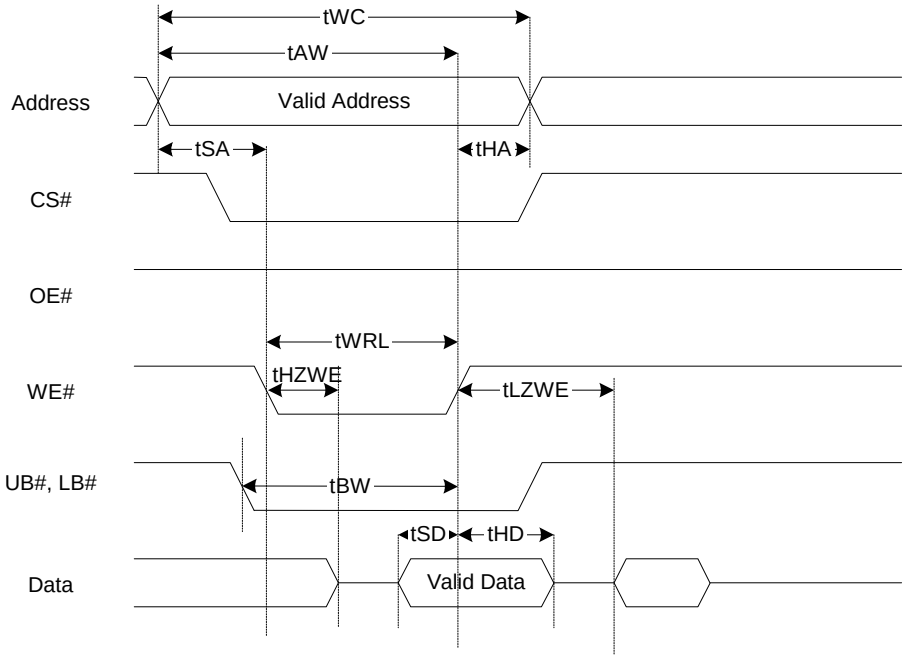



### Standard Port Read Cycle (Right Port Access, WE# High)

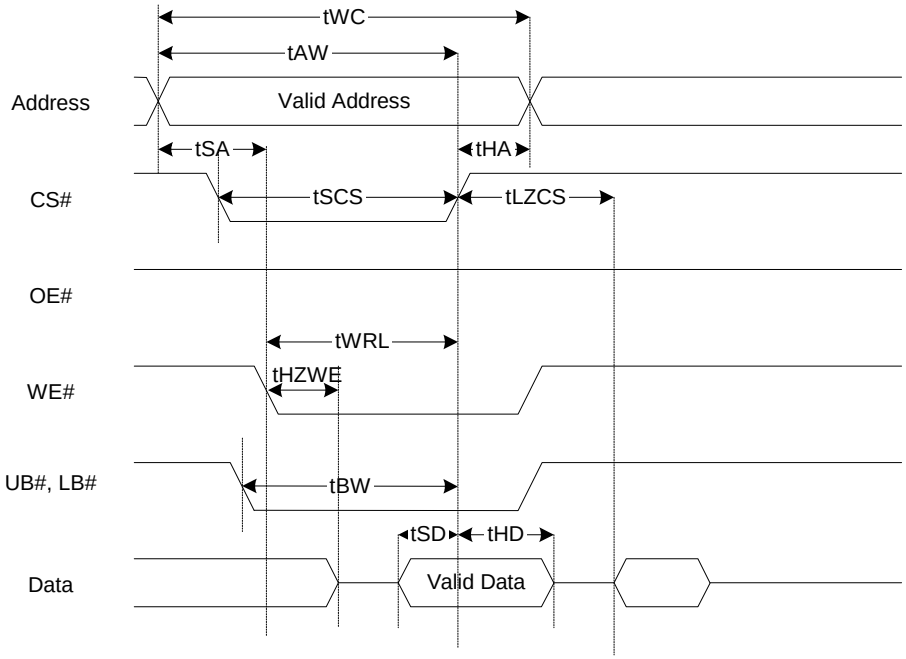


## Switching Waveforms (continued)

### Standard Port Write Cycle (Right Port Access, WE# Controlled)

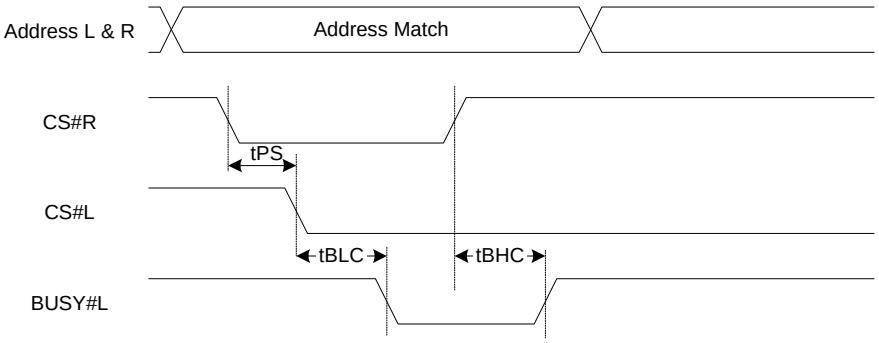



### Standard Port Write Cycle (Right Port Access, CS# Controlled)

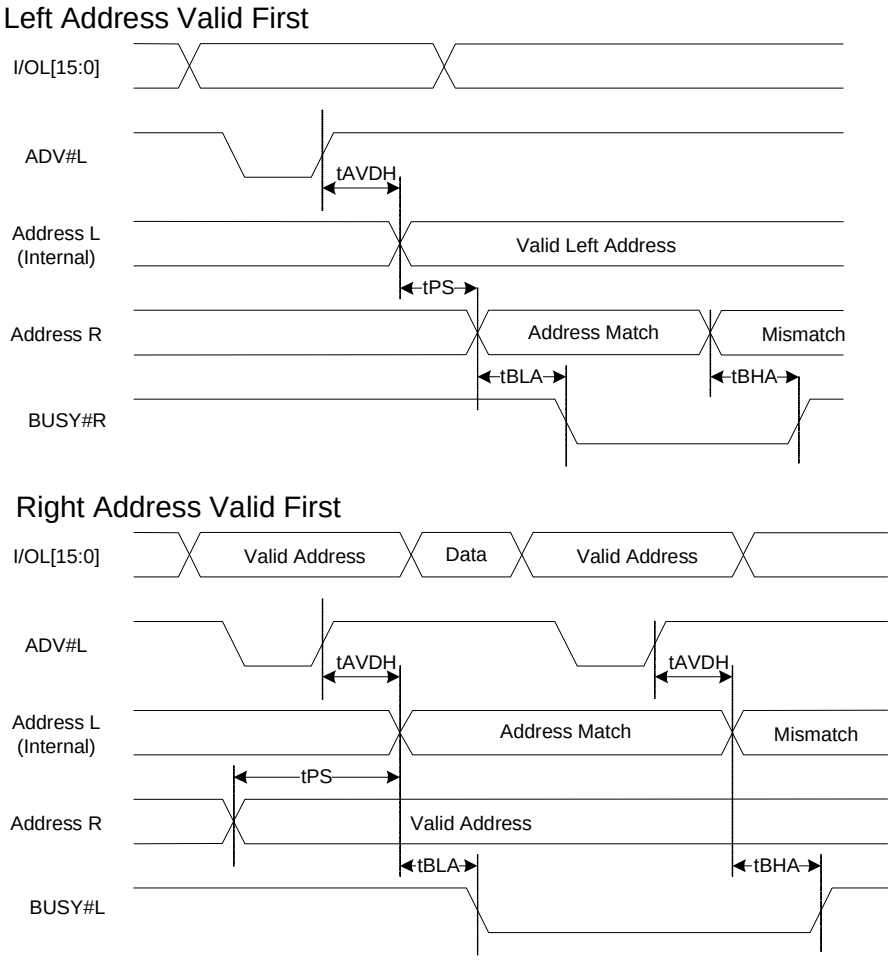


## Switching Waveforms (continued)

### Arbitration Timing

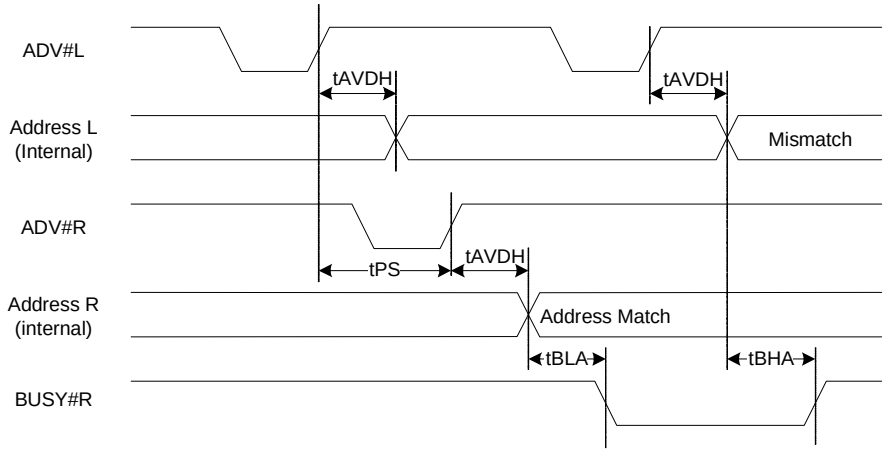



### Arbitration Timing (Address Controlled with Left ADM and Right Std Configuration

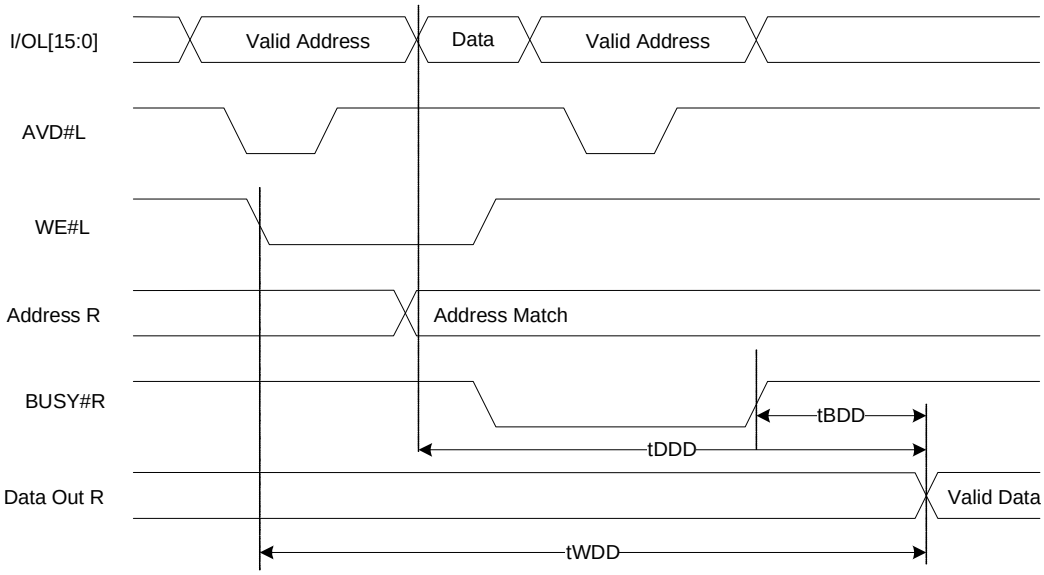


## Switching Waveforms (continued)

### Arbitration Timing (Address Controlled with Left ADM and Right ADM Configuration)

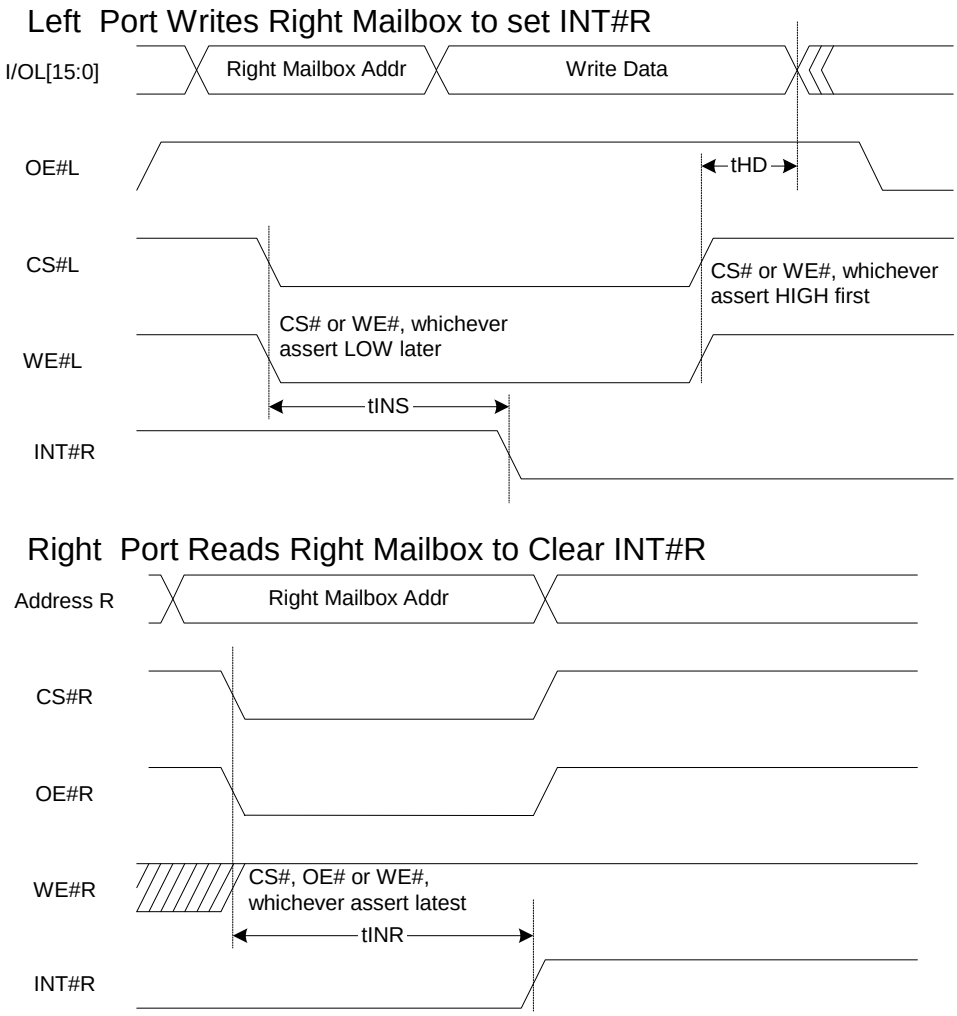



### Read with BUSY# Timing



## Switching Waveforms (continued)

### Interrupt Timing



## Part List

**16k x16 MoBL ADM Asynchronous Dual-Port SRAM**

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 65 | CYDMX256A16-65BVXI | BZ100 | 100-ball Lead-free 0.5-mm Pitch BGA | Industrial |
| 90 | CYDMX256A16-90BVXI | BZ100 | 100-ball Lead-free 0.5-mm Pitch BGA | Industrial |

**8k x16 MoBL ADM Asynchronous Dual-Port SRAM**

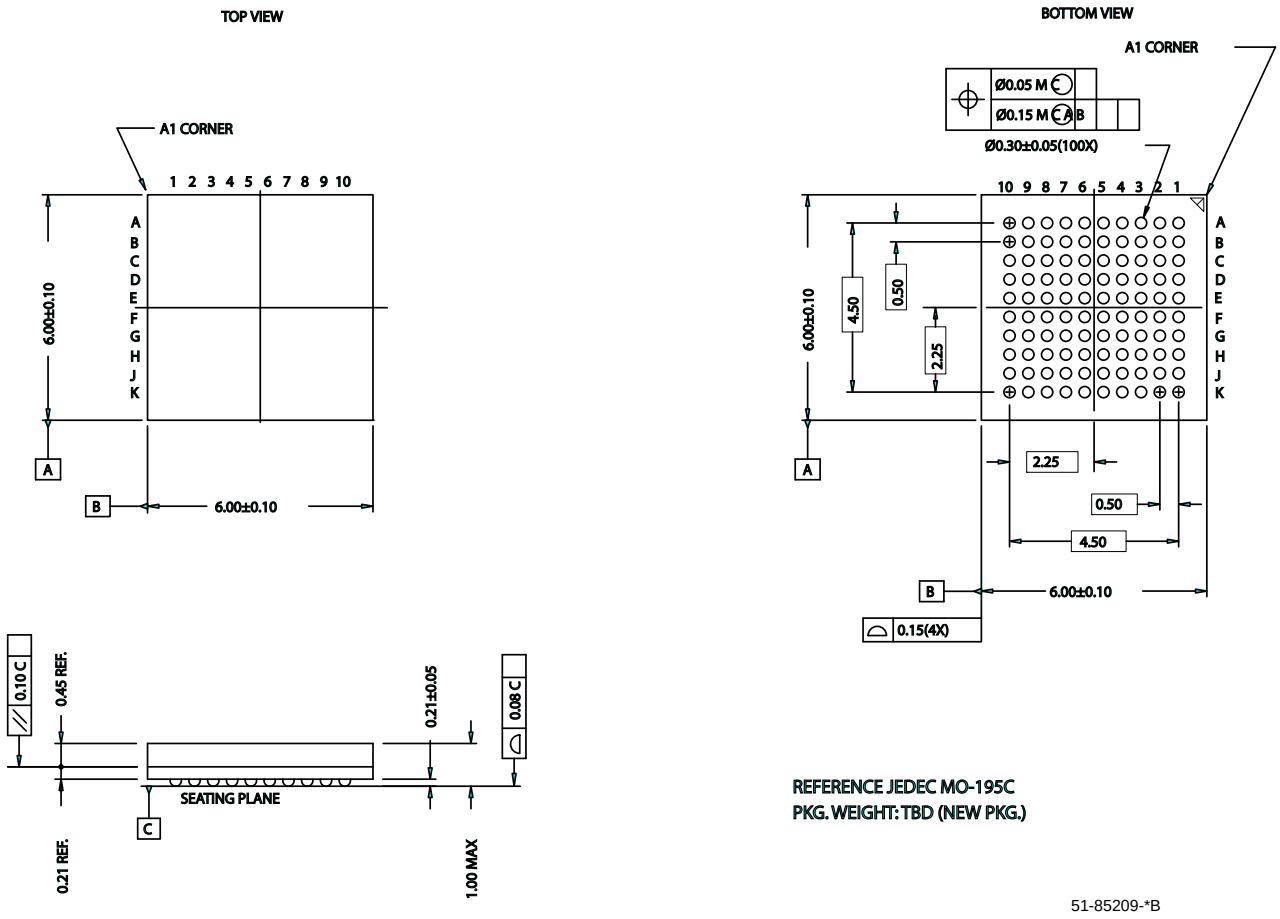
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 65 | CYDMX128A16-65BVXI | BZ100 | 100-ball Lead-free 0.5-mm Pitch BGA | Industrial |
| 90 | CYDMX128A16-90BVXI | BZ100 | 100-ball Lead-free 0.5-mm Pitch BGA | Industrial |

**4k x16 MoBL ADM Asynchronous Dual-Port SRAM**

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 65 | CYDMX064A16-65BVXI | BZ100 | 100-ball Lead-free 0.5-mm Pitch BGA | Industrial |
| 90 | CYDMX064A16-90BVXI | BZ100 | 100-ball Lead-free 0.5-mm Pitch BGA | Industrial |

## Package Diagram

**Figure 2. 100 VFBGA (6 x 6 x 1.0 mm) BZ100A**



## Document History Page

| Document Title: CYDMX256A16/CYDMX128A16/CYDMX064A16 16k/8k/4k x 16 MoBL® ADM Asynchronous Dual-Port Static RAM Final Data sheet<br>Document Number: 001-08090 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 462234 | SEE ECN | HKH | New data sheet |
| *A | 491702 | SEE ECN | HKH | Removed none applicable timing tBW<br>Revised standard port timing numbers<br>Corrected typo |
| *B | 500425 | SEE ECN | HKH | Updated tWC, tSCS to reflect bin spec<br>Added note for special condition of tPS<br>Updated DC data that are previously TBD<br>Added note for tLZOE that is garanteed by design by not tested |
| *C | 2142766 | SEE ECN | YDT | Relaxed -65 Standard port timing to match the standard port timing of -90 |

| | | Current Timing | | | New Timing | |
|---|---|---|---|---|---|---|
| **Standard SRAM Port Read Cycle** | | | | | | |
| **Parameter** | **Description** | **Min** | **Max** | | **Min** | **Max** |
| tRC | Read Cycle Time | 40 | | | 55 | |
| tAA | Address to Data Valid | | 40 | | | 55 |
| tOHA | Output Hold from Address Change | 5 | | | 5 | |
| tACS | CS# to Data Valid | | 40 | | | 55 |
| tDOE | OE# Low to Data Valid | | 25 | | | 30 |
| tLZOE[24] | OE# Low to Data Low-Z | 5 | | | 5 | |
| tHZOE | OE# High to Data High-Z | | 10 | | | 25 |
| tLZCS | CS# Low to Data Low-Z | 5 | | | 5 | |
| tHZCS | CS# High to Data High-Z | | 10 | | | 25 |
| tLZBE | UB#/LB# Low to Data Low-Z | 5 | | | 5 | |
| tHZBE | UB#/LB# High to Data High-Z | | 10 | | | 25 |
| tABE | UB#/LB# Access Time | | 40 | | | 55 |
| | | | | | | |
| **Standard SRAM Port Write Cycle** | | | | | | |
| **Parameter** | **Description** | **Min** | **Max** | | **Min** | **Max** |
| tWC | Write Cycle Time | 40 | | | 55 | |
| tSCS | CS# Low to Write End | 30 | | | 45 | |
| tAW | Address Valid to Write End | 30 | | | 45 | |
| tHA | Address Hold from Write End | 0 | | | 0 | |
| tSA | Address Set-Up to Write Start | 0 | | | 0 | |
| tWRL | Write Pulse Width | 25 | | | 40 | |
| tSD | Data Set-Up to Write End | 20 | | | 30 | |
| tHD | Data Hold from Write End | 0 | | | 0 | |
| tHZWE | WE# Low to Data High-Z | | 15 | | | 25 |
| tLZWE | WE# High to Data Low-Z | 0 | | | 0 | |
| **Arbitration Timing** | | | | | | |
| **Parameter** | **Description** | **Min** | **Max** | | **Min** | **Max** |
| tBLA | BUSY# Low from Address Match | | 30 | | | 45 |
| tBHA | BUSY# High from Address Match | | 30 | | | 45 |
| tBLC | BUSY# Low from CS# Low | | 30 | | | 45 |
| tBHC | BUSY# High from CS# High | | 30 | | | 45 |
| tPS[27] | Port Set-Up for Priority | 5 | | | 5 | |
| tBDD | BUSY# High to Data Valid | | 30 | | | 45 |
| tWDD | Write Pulse to Data Delay | | 55 | | | 80 |
| tDDD | Write Data Valid to Read Data Valid | | 45 | | | 65 |
| **Interrupt Timing** | | | | | | |
| **Parameter** | **Description** | **Min** | **Max** | | **Min** | **Max** |
| tINS | INT# Set Time | | 35 | | | 45 |
| tINR | INT# Reset Time | | 35 | | | 45 |