

3. PSoC Functional Overview

The PSoC family consists of many *Programmable System-on-Chip Controller* devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture allows the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated on the left, is comprised of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows all the device resources to be combined into a complete custom system. The PSoC CY8C29x66 family can have up to five IO ports that connect to the global digital and analog interconnects, providing access to 8 digital blocks and 12 analog blocks.

3.1 PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 17 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 16K of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2K of EEPROM emulated using the Flash. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

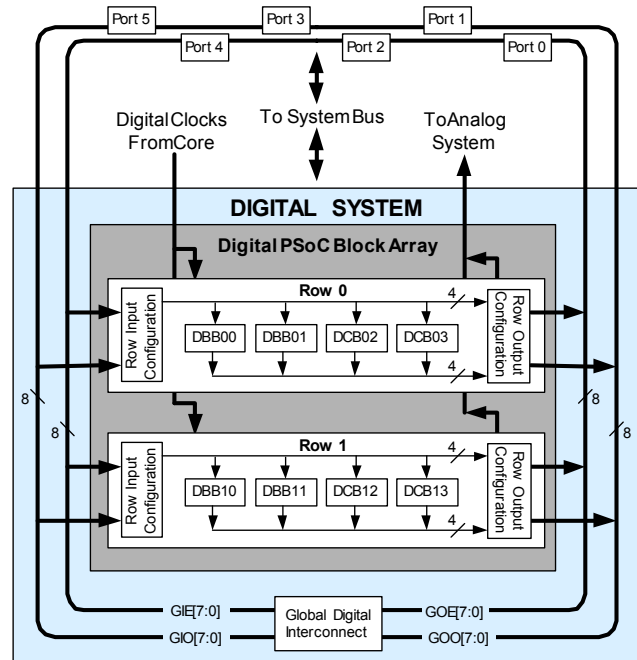
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

3.2 Digital System

The Digital System is composed of 8 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 3-1. Digital System Block Diagram



Digital peripheral configurations include those listed below.

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to 2)
- SPI slave and master (up to 2)
- I2C slave and multi-master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to 2)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled "[PSoC Device Characteristics](#)" on page 4.

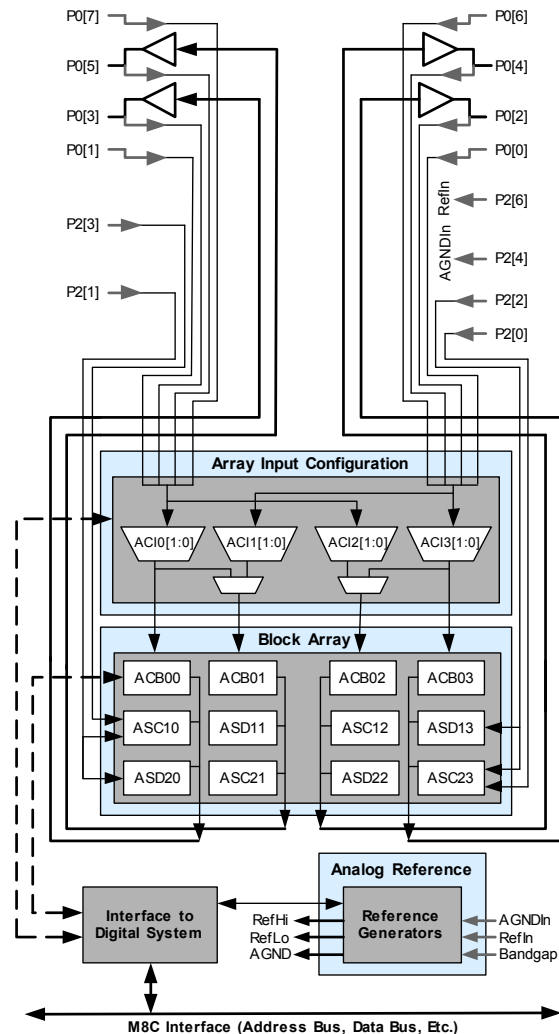
3.3 Analog System

The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, and 8 pole band-pass, low-pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (four with 30 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in the figure below.

Figure 3-2. Analog System Block Diagram



3.4 Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Statements describing the merits of each system resource are below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.

- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

3.5 PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is highlighted below.

Table 3-1. PSoC Device Characteristics

PSoC Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	12	4	4	12	2K	32K
CY8C27x43	up to 44	2	8	12	4	4	12	256 Bytes	16K
CY8C24x94	49	1	4	48	2	2	6	1K	16K
CY8C24x23	up to 24	1	4	12	2	2	6	256 Bytes	4K
CY8C24x23A	up to 24	1	4	12	2	2	6	256 Bytes	4K
CY8C21x34	up to 28	1	4	28	0	2	4 ^[1]	512 Bytes	8K
CY8C21x23	16	1	4	8	0	2	4 ^[1]	256 Bytes	4K
CY8C20x34	up to 28	0	0	28	0	0	3 ^[2]	512 Bytes	8K

Notes

1. Limited analog functionality.
2. Two analog blocks and one CapSense.

4. Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PSoC[®] Programmable System-on-Chip[™] Technical Reference Manual for CY8C28xxx PSoC devices.

For up to date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

4.1 Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

4.2 Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

4.3 Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

4.4 CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

4.5 Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

4.6 Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

5. Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built in support for third party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

5.1 PSoC Designer Software Subsystems

5.1.1 System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Programmable System-on-Chip Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

5.1.2 Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

5.1.3 Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

5.1.4 Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

5.1.5 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

5.1.6 Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

5.2 In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

6. Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select Components
2. Configure Components
3. Organize and Connect
4. Generate, Verify, and Debug

6.1 Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I²C-bus, for example), and the logic to control how they interact with one another (called valuator).

In the chip-level view, the components are called “user modules”. User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and programmable system-on-chip varieties.

6.2 Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in the PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

6.3 Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the IO pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuator to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer’s output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

6.4 Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed. The system-level design also generates a `C main()` program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

7. Document Conventions

7.1 Acronyms Used

This table lists the acronyms used in this data sheet.

Table 7-1. Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
ICE	in-circuit emulator
IDE	integrated development environment
IO	input/output
ISSP	in-system serial programming
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PGA	programmable gain amplifier
POR	power on reset
PPOR	precision power on reset
PSoC [®]	Programmable System-on-Chip [™]
PWM	pulse width modulator
ROM	read only memory
SC	switched capacitor
SMP	switch mode pump
SRAM	static random access memory

7.2 Units of Measure

A units of measure table is located in the section [Electrical Specifications](#) on page 19. [Table 11-1](#) on page 19 lists all the abbreviations used to measure the PSoC devices.

7.3 Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

8. Pinouts

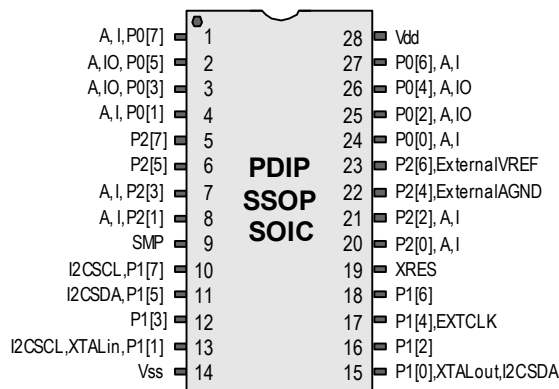
The CY8C29x66 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of Digital IO. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

8.1 28-Pin Part Pinout

Table 8-1. 28-Pin Part Pinout (PDIP, SSOP, SOIC)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog column mux input.
2	IO	IO	P0[5]	Analog column mux input and column output.
3	IO	IO	P0[3]	Analog column mux input and column output.
4	IO	I	P0[1]	Analog column mux input.
5	IO		P2[7]	
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input.
8	IO	I	P2[1]	Direct switched capacitor block input.
9	Power		SMP	Switch Mode Pump (SMP) connection to external components required.
10	IO		P1[7]	I2C Serial Clock (SCL).
11	IO		P1[5]	I2C Serial Data (SDA).
12	IO		P1[3]	
13	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*.
14	Power		Vss	Ground connection.
15	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA), ISSP-SDATA*.
16	IO		P1[2]	
17	IO		P1[4]	Optional External Clock Input (EXTCLK).
18	IO		P1[6]	
19	Input		XRES	Active high external reset with internal pull down.
20	IO	I	P2[0]	Direct switched capacitor block input.
21	IO	I	P2[2]	Direct switched capacitor block input.
22	IO		P2[4]	External Analog Ground (AGND).
23	IO		P2[6]	External Voltage Reference (VREF).
24	IO	I	P0[0]	Analog column mux input.
25	IO	IO	P0[2]	Analog column mux input and column output.
26	IO	IO	P0[4]	Analog column mux input and column output.
27	IO	I	P0[6]	Analog column mux input.
28	Power		Vdd	Supply voltage.

Figure 8-1. CY8C29466 28-Pin PSoC Device



LEGEND: A = Analog, I = Input, and O = Output.

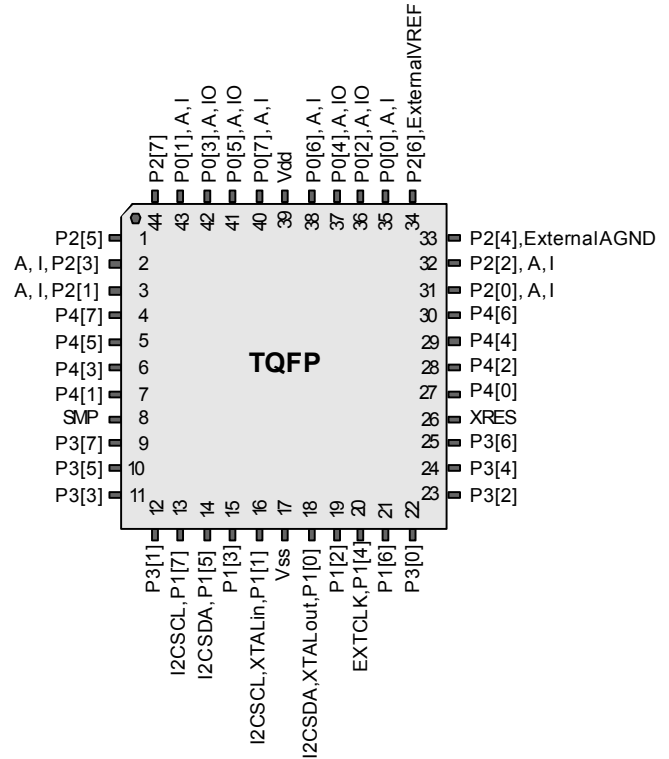
* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

8.2 44-Pin Part Pinout

Table 8-2. 44-Pin Part Pinout (TQFP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO		P2[5]	
2	IO	I	P2[3]	Direct switched capacitor block input.
3	IO	I	P2[1]	Direct switched capacitor block input.
4	IO		P4[7]	
5	IO		P4[5]	
6	IO		P4[3]	
7	IO		P4[1]	
8	Power		SMP	Switch Mode Pump (SMP) connection to external components required.
9	IO		P3[7]	
10	IO		P3[5]	
11	IO		P3[3]	
12	IO		P3[1]	
13	IO		P1[7]	I2C Serial Clock (SCL).
14	IO		P1[5]	I2C Serial Data (SDA).
15	IO		P1[3]	
16	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*.
17	Power		Vss	Ground connection.
18	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA), ISSP-SDATA*.
19	IO		P1[2]	
20	IO		P1[4]	Optional External Clock Input (EXTCLK).
21	IO		P1[6]	
22	IO		P3[0]	
23	IO		P3[2]	
24	IO		P3[4]	
25	IO		P3[6]	
26	Input		XRES	Active high external reset with internal pull down.
27	IO		P4[0]	
28	IO		P4[2]	
29	IO		P4[4]	
30	IO		P4[6]	
31	IO	I	P2[0]	Direct switched capacitor block input.
32	IO	I	P2[2]	Direct switched capacitor block input.
33	IO		P2[4]	External Analog Ground (AGND).
34	IO		P2[6]	External Voltage Reference (VREF).
35	IO	I	P0[0]	Analog column mux input.
36	IO	IO	P0[2]	Analog column mux input and column output.
37	IO	IO	P0[4]	Analog column mux input and column output.
38	IO	I	P0[6]	Analog column mux input.
39	Power		Vdd	Supply voltage.
40	IO	I	P0[7]	Analog column mux input.
41	IO	IO	P0[5]	Analog column mux input and column output.
42	IO	IO	P0[3]	Analog column mux input and column output.
43	IO	I	P0[1]	Analog column mux input.
44	IO		P2[7]	

Figure 8-2. CY8C29566 44-Pin PSoC Device



LEGEND: A = Analog, I = Input, and O = Output.

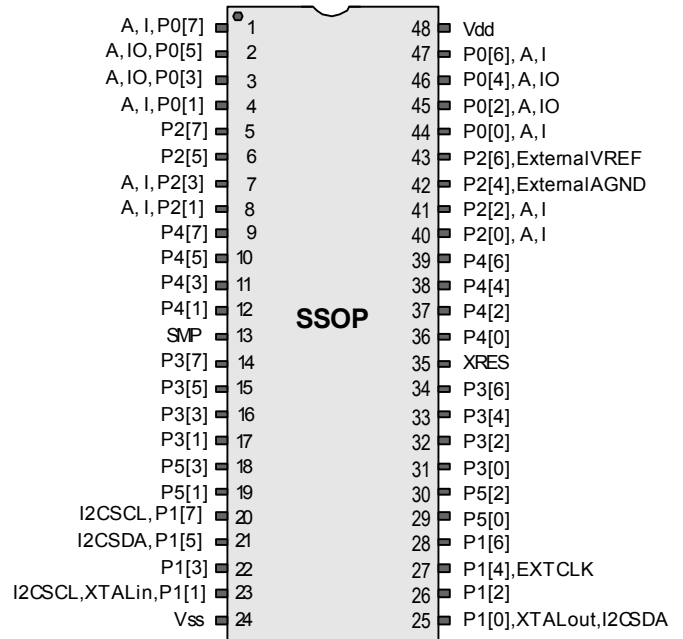
* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

8.3 48-Pin Part Pinouts

Table 8-3. 48-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog column mux input.
2	IO	IO	P0[5]	Analog column mux input and column output.
3	IO	IO	P0[3]	Analog column mux input and column output.
4	IO	I	P0[1]	Analog column mux input.
5	IO		P2[7]	
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input.
8	IO	I	P2[1]	Direct switched capacitor block input.
9	IO		P4[7]	
10	IO		P4[5]	
11	IO		P4[3]	
12	IO		P4[1]	
13	Power		SMP	Switch Mode Pump (SMP) connection to external components required.
14	IO		P3[7]	
15	IO		P3[5]	
16	IO		P3[3]	
17	IO		P3[1]	
18	IO		P5[3]	
19	IO		P5[1]	
20	IO		P1[7]	I2C Serial Clock (SCL).
21	IO		P1[5]	I2C Serial Data (SDA).
22	IO		P1[3]	
23	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*.
24	Power		Vss	Ground connection.
25	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA), ISSP-SDATA*.
26	IO		P1[2]	
27	IO		P1[4]	Optional External Clock Input (EXTCLK).
28	IO		P1[6]	
29	IO		P5[0]	
30	IO		P5[2]	
31	IO		P3[0]	
32	IO		P3[2]	
33	IO		P3[4]	
34	IO		P3[6]	
35	Input		XRES	Active high external reset with internal pull down.
36	IO		P4[0]	
37	IO		P4[2]	
38	IO		P4[4]	
39	IO		P4[6]	
40	IO	I	P2[0]	Direct switched capacitor block input.
41	IO	I	P2[2]	Direct switched capacitor block input.
42	IO		P2[4]	External Analog Ground (AGND).
43	IO		P2[6]	External Voltage Reference (VREF).
44	IO	I	P0[0]	Analog column mux input.
45	IO	IO	P0[2]	Analog column mux input and column output.
46	IO	IO	P0[4]	Analog column mux input and column output.
47	IO	I	P0[6]	Analog column mux input.
48	Power		Vdd	Supply voltage.

Figure 8-3. CY8C29666 48-Pin PSoC Device



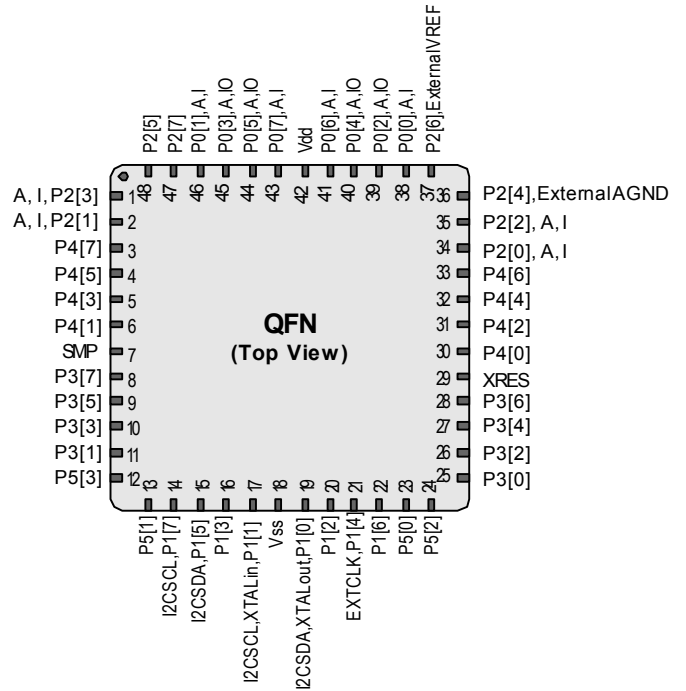
LEGEND: A = Analog, I = Input, and O = Output.

* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

Table 8-4. 48-Pin Part Pinout (QFN)**

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P2[3]	Direct switched capacitor block input.
2	IO	I	P2[1]	Direct switched capacitor block input.
3	IO		P4[7]	
4	IO		P4[5]	
5	IO		P4[3]	
6	IO		P4[1]	
7	Power		SMP	Switch Mode Pump (SMP) connection to external components required.
8	IO		P3[7]	
9	IO		P3[5]	
10	IO		P3[3]	
11	IO		P3[1]	
12	IO		P5[3]	
13	IO		P5[1]	
14	IO		P1[7]	I2C Serial Clock (SCL).
15	IO		P1[5]	I2C Serial Data (SDA).
16	IO		P1[3]	
17	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*.
18	Power		Vss	Ground connection.
19	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA), ISSP-SDATA*.
20	IO		P1[2]	
21	IO		P1[4]	Optional External Clock Input (EXTCLK).
22	IO		P1[6]	
23	IO		P5[0]	
24	IO		P5[2]	
25	IO		P3[0]	
26	IO		P3[2]	
27	IO		P3[4]	
28	IO		P3[6]	
29	Input		XRES	Active high external reset with internal pull down.
30	IO		P4[0]	
31	IO		P4[2]	
32	IO		P4[4]	
33	IO		P4[6]	
34	IO	I	P2[0]	Direct switched capacitor block input.
35	IO	I	P2[2]	Direct switched capacitor block input.
36	IO		P2[4]	External Analog Ground (AGND).
37	IO		P2[6]	External Voltage Reference (VREF).
38	IO	I	P0[0]	Analog column mux input.
39	IO	IO	P0[2]	Analog column mux input and column output.
40	IO	IO	P0[4]	Analog column mux input and column output.
41	IO	I	P0[6]	Analog column mux input.
42	Power		Vdd	Supply voltage.
43	IO	I	P0[7]	Analog column mux input.
44	IO	IO	P0[5]	Analog column mux input and column output.
45	IO	IO	P0[3]	Analog column mux input and column output.
46	IO	I	P0[1]	Analog column mux input.
47	IO		P2[7]	
48	IO		P2[5]	

Figure 8-4. CY8C29666 48-Pin PSoC Device



LEGEND: A = Analog, I = Input, and O = Output.

* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

** The QFN package has a center pad that must be connected to ground (Vss).

8.4 100-Pin Part Pinout

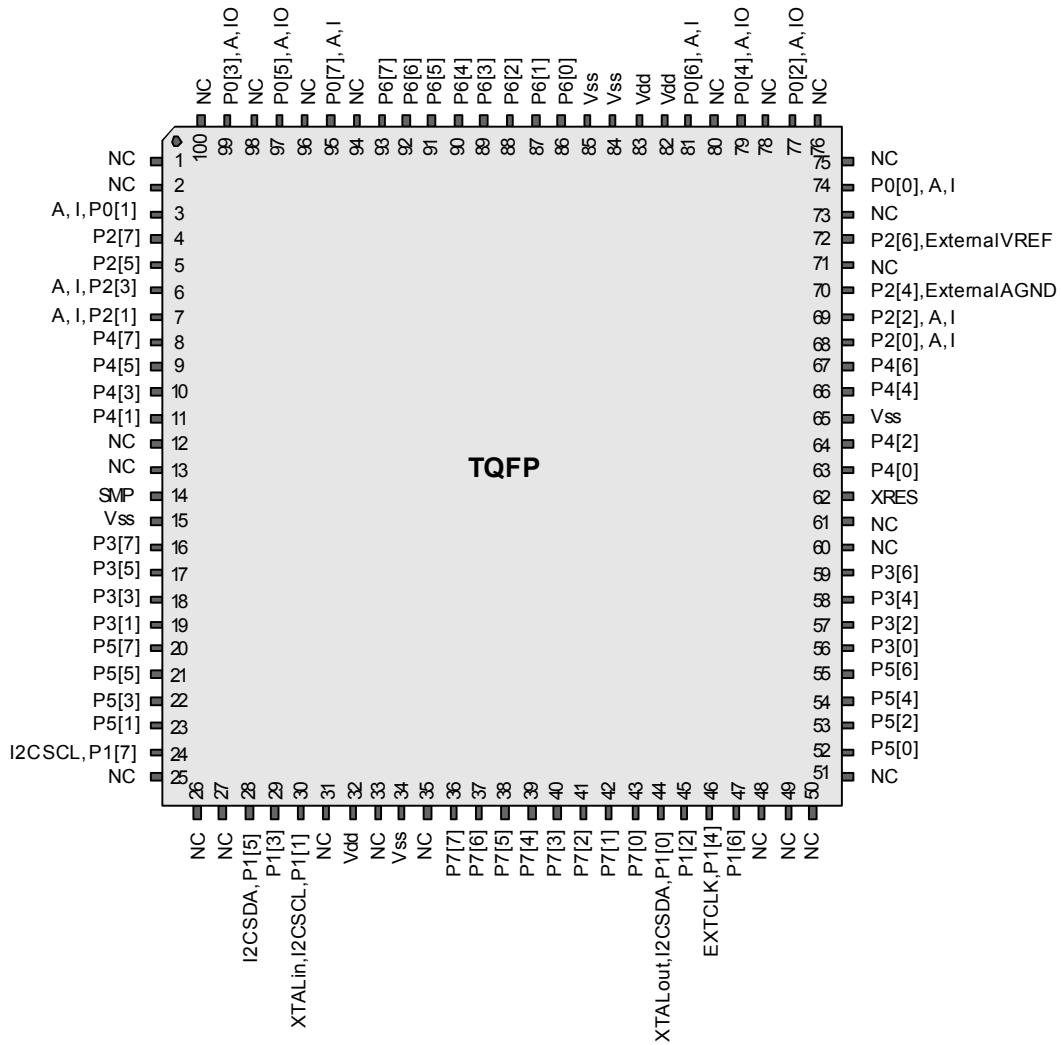
Table 8-5. 100-Pin Part Pinout (TQFP)

Pin No.	Type		Name	Description	Pin No.	Type		Name	Description
	Digital	Analog				Digital	Analog		
1			NC	No connection.	51			NC	No connection.
2			NC	No connection.	52	IO		P5[0]	
3	IO	I	P0[1]	Analog column mux input.	53	IO		P5[2]	
4	IO		P2[7]		54	IO		P5[4]	
5	IO		P2[5]		55	IO		P5[6]	
6	IO	I	P2[3]	Direct switched capacitor block input.	56	IO		P3[0]	
7	IO	I	P2[1]	Direct switched capacitor block input.	57	IO		P3[2]	
8	IO		P4[7]		58	IO		P3[4]	
9	IO		P4[5]		59	IO		P3[6]	
10	IO		P4[3]		60			NC	No connection.
11	IO		P4[1]		61			NC	No connection.
12			NC	No connection.	62		Input	XRES	Active high external reset with internal pull down.
13			NC	No connection.	63	IO		P4[0]	
14		Power	SMP	Switch Mode Pump (SMP) connection to external components required.	64	IO		P4[2]	
15		Power	Vss	Ground connection.	65		Power	Vss	Ground connection.
16	IO		P3[7]		66	IO		P4[4]	
17	IO		P3[5]		67	IO		P4[6]	
18	IO		P3[3]		68	IO	I	P2[0]	Direct switched capacitor block input.
19	IO		P3[1]		69	IO	I	P2[2]	Direct switched capacitor block input.
20	IO		P5[7]		70	IO		P2[4]	External Analog Ground (AGND).
21	IO		P5[5]		71			NC	No connection.
22	IO		P5[3]		72	IO		P2[6]	External Voltage Reference (VREF).
23	IO		P5[1]		73			NC	No connection.
24	IO		P1[7]	I2C Serial Clock (SCL).	74	IO	I	P0[0]	Analog column mux input.
25			NC	No connection.	75			NC	No connection.
26			NC	No connection.	76			NC	No connection.
27			NC	No connection.	77	IO	IO	P0[2]	Analog column mux input and column output.
28	IO		P1[5]	I2C Serial Data (SDA).	78			NC	No connection.
29	IO		P1[3]		79	IO	IO	P0[4]	Analog column mux input and column output.
30	IO		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*.	80			NC	No connection.
31			NC	No connection.	81	IO	I	P0[6]	Analog column mux input.
32		Power	Vdd	Supply voltage.	82		Power	Vdd	Supply voltage.
33			NC	No connection.	83		Power	Vdd	Supply voltage.
34		Power	Vss	Ground connection.	84		Power	Vss	Ground connection.
35			NC	No connection.	85		Power	Vss	Ground connection.
36	IO		P7[7]		86	IO		P6[0]	
37	IO		P7[6]		87	IO		P6[1]	
38	IO		P7[5]		88	IO		P6[2]	
39	IO		P7[4]		89	IO		P6[3]	
40	IO		P7[3]		90	IO		P6[4]	
41	IO		P7[2]		91	IO		P6[5]	
42	IO		P7[1]		92	IO		P6[6]	
43	IO		P7[0]		93	IO		P6[7]	
44	IO		P1[0]	Crystal (XTALout), I2C Serial Data (SDA), ISSP-SDATA*.	94			NC	No connection.
45	IO		P1[2]		95	IO	I	P0[7]	Analog column mux input.
46	IO		P1[4]	Optional External Clock Input (EXTCLK).	96			NC	No connection.
47	IO		P1[6]		97	IO	IO	P0[5]	Analog column mux input and column output.
48			NC	No connection.	98			NC	No connection.
49			NC	No connection.	99	IO	IO	P0[3]	Analog column mux input and column output.
50			NC	No connection.	100			NC	No connection.

LEGEND: A = Analog, I = Input, and O = Output.

* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

Figure 8-5. CY8C29866 100-Pin PSoC Device



8.5 100-Pin Part Pinout (On-Chip Debug)

The 100-pin TQFP part is for the CY8C29000 On-Chip Debug (OCD) PSoC device.

Note OCD parts are only used for in-circuit debugging. OCD parts are NOT available for production

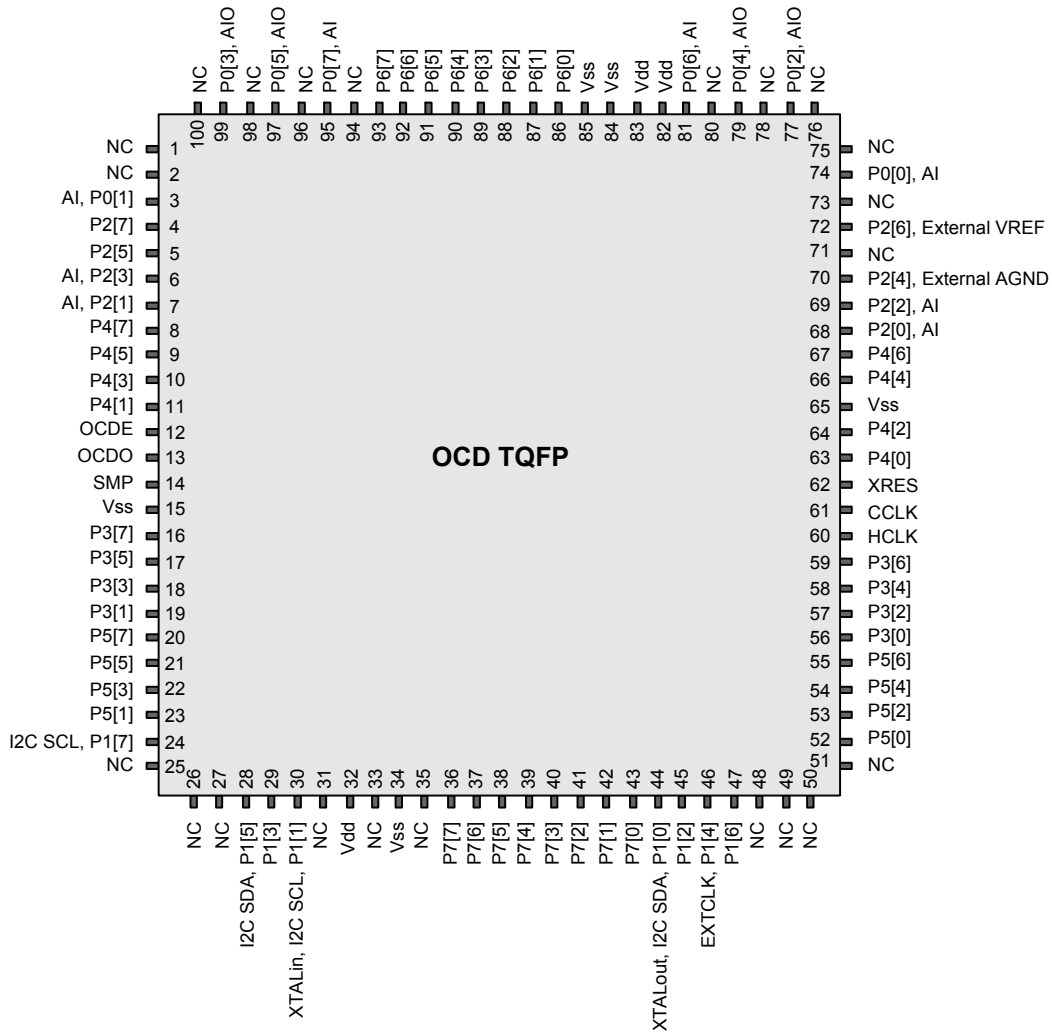
Table 8-6. 100-Pin OCD Part Pinout (TQFP)

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1			NC	No internal connection.	51			NC	No internal connection.
2			NC	No internal connection.	52	IO		P5[0]	
3	IO	I	P0[1]	Analog column mux input.	53	IO		P5[2]	
4	IO		P2[7]		54	IO		P5[4]	
5	IO		P2[5]		55	IO		P5[6]	
6	IO	I	P2[3]	Direct switched capacitor block input.	56	IO		P3[0]	
7	IO	I	P2[1]	Direct switched capacitor block input.	57	IO		P3[2]	
8	IO		P4[7]		58	IO		P3[4]	
9	IO		P4[5]		59	IO		P3[6]	
10	IO		P4[3]		60			HCLK	OCD high speed clock output
11	IO		P4[1]		61			CCLK	OCD CPU clock output
12			OCDE	OCD even data IO	62	Input		XRES	Active high pin reset with internal pull down.
13			OCDO	OCD odd data output	63	IO		P4[0]	
14	Power		SMP	Switch Mode Pump (SMP) connection to required external components.	64	IO		P4[2]	
15	Power		Vss	Ground connection.	65	Power		Vss	Ground connection.
16	IO		P3[7]		66	IO		P4[4]	
17	IO		P3[5]		67	IO		P4[6]	
18	IO		P3[3]		68	IO	I	P2[0]	Direct switched capacitor block input.
19	IO		P3[1]		69	IO	I	P2[2]	Direct switched capacitor block input.
20	IO		P5[7]		70	IO		P2[4]	External Analog Ground (AGND) input.
21	IO		P5[5]		71			NC	No internal connection.
22	IO		P5[3]		72	IO		P2[6]	External Voltage Reference (VREF) input.
23	IO		P5[1]		73			NC	No internal connection.
24	IO		P1[7]	I2C Serial Clock (SCL)	74	IO	I	P0[0]	Analog column mux input.
25			NC	No internal connection.	75			NC	No internal connection.
26			NC	No internal connection.	76			NC	No internal connection.
27			NC	No internal connection.	77	IO	IO	P0[2]	Analog column mux input and column output.
28	IO		P1[5]	I2C Serial Data (SDA).	78			NC	No internal connection.
29	IO		P1[3]	IFMTEST	79	IO	IO	P0[4]	Analog column mux input and column output, VREF.
30	IO		P1[1]*	Crystal (XTALin), I2C Serial Clock (SCL), TC SCLK.	80			NC	No internal connection.
31			NC	No internal connection.	81	IO	I	P0[6]	Analog column mux input.
32	Power		Vdd	Supply voltage.	82	Power		Vdd	Supply voltage.
33			NC	No internal connection.	83	Power		Vdd	Supply voltage.
34	Power		Vss	Ground connection.	84	Power		Vss	Ground connection.
35			NC	No internal connection.	85	Power		Vss	Ground connection.
36	IO		P7[7]		86	IO		P6[0]	
37	IO		P7[6]		87	IO		P6[1]	
38	IO		P7[5]		88	IO		P6[2]	
39	IO		P7[4]		89	IO		P6[3]	
40	IO		P7[3]		90	IO		P6[4]	
41	IO		P7[2]		91	IO		P6[5]	
42	IO		P7[1]		92	IO		P6[6]	
43	IO		P7[0]		93	IO		P6[7]	
44	IO		P1[0]*	Crystal (XTALout), I2C Serial Data (SDA), TC SDATA	94			NC	No internal connection.
45	IO		P1[2]	VFTEST	95	IO	I	P0[7]	Analog column mux input.
46	IO		P1[4]	Optional External Clock Input (EXTCLK)	96			NC	No internal connection.
47	IO		P1[6]		97	IO	IO	P0[5]	Analog column mux input and column output.
48			NC	No internal connection.	98			NC	No internal connection.
49			NC	No internal connection.	99	IO	IO	P0[3]	Analog column mux input and column output.
50			NC	No internal connection.	100			NC	No internal connection.

LEGEND A = Analog, I = Input, O = Output, NC = No Connection, TC/TM: Test.

* ISSP pin which is not HiZ at POR.

Figure 8-6. CY8C29000 OCD (Not for Production)



This section lists the registers of the CY8C29x66 PSoC device. For detailed register information, reference the *PSoC Programmable System-on-Chip Technical Reference Manual*.

9. Register Conventions

9.1 Abbreviations Used

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

10. Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XO \bar{I} bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XO \bar{I} bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 10-1. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBB20DR0	40	#	ASC10CR0	80	RW	RD12RI	C0	RW
PRT0IE	01	RW	DBB20DR1	41	W	ASC10CR1	81	RW	RD12SYN	C1	RW
PRT0GS	02	RW	DBB20DR2	42	RW	ASC10CR2	82	RW	RD12IS	C2	RW
PRT0DM2	03	RW	DBB20CR0	43	#	ASC10CR3	83	RW	RD12LT0	C3	RW
PRT1DR	04	RW	DBB21DR0	44	#	ASD11CR0	84	RW	RD12LT1	C4	RW
PRT1IE	05	RW	DBB21DR1	45	W	ASD11CR1	85	RW	RD12RO0	C5	RW
PRT1GS	06	RW	DBB21DR2	46	RW	ASD11CR2	86	RW	RD12RO1	C6	RW
PRT1DM2	07	RW	DBB21CR0	47	#	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	DCB22DR0	48	#	ASC12CR0	88	RW	RD13RI	C8	RW
PRT2IE	09	RW	DCB22DR1	49	W	ASC12CR1	89	RW	RD13SYN	C9	RW
PRT2GS	0A	RW	DCB22DR2	4A	RW	ASC12CR2	8A	RW	RD13IS	CA	RW
PRT2DM2	0B	RW	DCB22CR0	4B	#	ASC12CR3	8B	RW	RD13LT0	CB	RW
PRT3DR	0C	RW	DCB23DR0	4C	#	ASD13CR0	8C	RW	RD13LT1	CC	RW
PRT3IE	0D	RW	DCB23DR1	4D	W	ASD13CR1	8D	RW	RD13RO0	CD	RW
PRT3GS	0E	RW	DCB23DR2	4E	RW	ASD13CR2	8E	RW	RD13RO1	CE	RW
PRT3DM2	0F	RW	DCB23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW	DBB30DR0	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	DBB30DR1	51	W	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	DBB30DR2	52	RW	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	DBB30CR0	53	#	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	DBB31DR0	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	DBB31DR1	55	W	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	DBB31DR2	56	RW	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	DBB31CR0	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
PRT6DR	18	RW	DCB32DR0	58	#	ASD22CR0	98	RW	I2C_DR	D8	RW
PRT6IE	19	RW	DCB32DR1	59	W	ASD22CR1	99	RW	I2C_MSCR	D9	#
PRT6GS	1A	RW	DCB32DR2	5A	RW	ASD22CR2	9A	RW	INT_CLR0	DA	RW
PRT6DM2	1B	RW	DCB32CR0	5B	#	ASD22CR3	9B	RW	INT_CLR1	DB	RW
PRT7DR	1C	RW	DCB33DR0	5C	#	ASC23CR0	9C	RW	INT_CLR2	DC	RW
PRT7IE	1D	RW	DCB33DR1	5D	W	ASC23CR1	9D	RW	INT_CLR3	DD	RW
PRT7GS	1E	RW	DCB33DR2	5E	RW	ASC23CR2	9E	RW	INT_MSK3	DE	RW
PRT7DM2	1F	RW	DCB33CR0	5F	#	ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MULO_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MULO_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MULO_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MULO_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RD10RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RD10SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RD10IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RD10LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RD10LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RD10RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RD10RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RD11RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RD11SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RD11IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RD11LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RD11LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RD11RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

Table 10-2. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBB20FN	40	RW	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBB20IN	41	RW	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBB20OU	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBB21FN	44	RW	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBB21IN	45	RW	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBB21OU	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW	DCB22FN	48	RW	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2DM1	09	RW	DCB22IN	49	RW	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2IC0	0A	RW	DCB22OU	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DM0	0C	RW	DCB23FN	4C	RW	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3DM1	0D	RW	DCB23IN	4D	RW	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3IC0	0E	RW	DCB23OU	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW	DBB30FN	50	RW	ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	DBB30IN	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	DBB30OU	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	DBB31FN	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	DBB31IN	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	DBB31OU	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
PRT6DM0	18	RW	DCB32FN	58	RW	ASD22CR0	98	RW		D8	
PRT6DM1	19	RW	DCB32IN	59	RW	ASD22CR1	99	RW		D9	
PRT6IC0	1A	RW	DCB32OU	5A	RW	ASD22CR2	9A	RW		DA	
PRT6IC1	1B	RW		5B		ASD22CR3	9B	RW		DB	
PRT7DM0	1C	RW	DCB33FN	5C	RW	ASC23CR0	9C	RW		DC	
PRT7DM1	1D	RW	DCB33IN	5D	RW	ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
PRT7IC0	1E	RW	DCB33OU	5E	RW	ASC23CR2	9E	RW	OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7		DEC_CR2	E7	RW
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

11. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C29x66 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at <http://www.cypress.com/psoc>.

Specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $T_J \leq 100^{\circ}\text{C}$, except where noted. Refer to Table 11-17 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 11-1. Voltage versus CPU Frequency

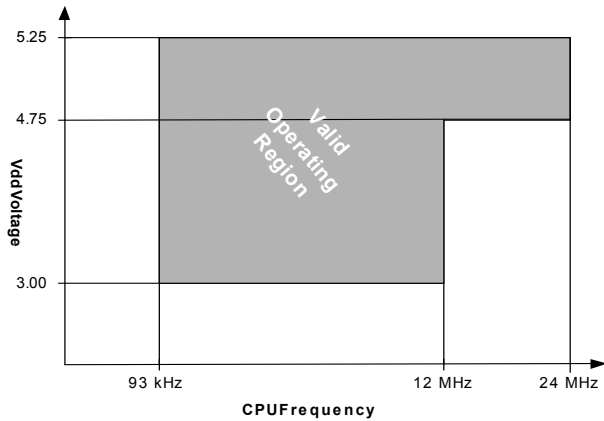
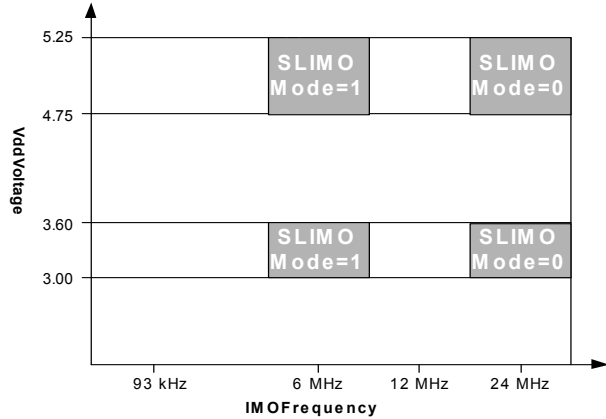


Figure 11-2. IMO Frequency Options



The following table lists the units of measure that are used in this chapter.

Table 11-1. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
$^{\circ}\text{C}$	degree Celsius	μW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
k Ω	kilohm	W	ohm
MHz	megahertz	μA	picoampere
M Ω	megaohm	pF	picofarad
μA	microampere	pp	peak-to-peak
μF	microfarad	ppm	parts per million
μH	microhenry	ps	picosecond
μs	microsecond	sps	samples per second
μV	microvolts	s	sigma: one standard deviation
μVrms	microvolts root-mean-square	V	volts

11.1 Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11-2. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit	Notes
T _{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
T _A	Ambient Temperature with Power Applied	-40	–	+85	°C	
V _{dd}	Supply Voltage on V _{dd} Relative to V _{ss}	-0.5	–	+6.0	V	
V _{IO}	DC Input Voltage	V _{ss} - 0.5	–	V _{dd} + 0.5	V	
V _{IOZ}	DC Voltage Applied to Tri-state	V _{ss} - 0.5	–	V _{dd} + 0.5	V	
I _{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I _{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up Current	–	–	200	mA	

11.2 Operating Temperature

Table 11-3. Operating Temperature

Symbol	Description	Min	Typ	Max	Unit	Notes
T _A	Ambient Temperature	-40	–	+85	°C	
T _J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See “ Thermal Impedances ” on page 41. The user must limit the power consumption to comply with this requirement.

11.3 DC Electrical Characteristics

11.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-4. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{DD}	Supply Voltage	3.00	–	5.25	V	See DC POR and LVD specifications, Table 3-15 on page 27.
I _{DD}	Supply Current	–	8	14	mA	Conditions are 5.0V, T _A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
I _{DD3}	Supply Current	–	5	9	mA	Conditions are V _{DD} = 3.3V, T _A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
I _{DDP}	Supply current when IMO = 6 MHz using SLIMO mode.	–	2	3	mA	Conditions are V _{DD} = 3.3V, T _A = 25 °C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz.
I _{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	–	3	10	μA	Conditions are with internal slow speed oscillator, V _{DD} = 3.3V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$.
I _{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	–	4	25	μA	Conditions are with internal slow speed oscillator, V _{DD} = 3.3V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$.
I _{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, internal slow oscillator, and 32 kHz crystal oscillator active.	–	4	12	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V _{DD} = 3.3V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$.
I _{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and 32 kHz crystal oscillator active.	–	5	27	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V _{DD} = 3.3V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$.
V _{REF}	Reference Voltage (Bandgap)	1.28	1.3	1.32	V	Trimmed for appropriate V _{DD} .

11.3.2 DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-5. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
R _{PU}	Pull up Resistor	4	5.6	8	kΩ	
R _{PD}	Pull down Resistor	4	5.6	8	kΩ	
V _{OH}	High Output Level	V _{DD} - 1.0	–	–	V	I _{OH} = 10 mA, V _{DD} = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I _{OH} budget.
V _{OL}	Low Output Level	–	–	0.75	V	I _{OL} = 25 mA, V _{DD} = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I _{OL} budget.
I _{OH}	High Level Source Current	10	–	–	mA	V _{OH} = V _{DD} -1.0V, see the limitations of the total current in the note for V _{OH}
I _{OL}	Low Level Sink Current	25	–	–	mA	V _{OL} = 0.75V, see the limitations of the total current in the note for V _{OL}
V _{IL}	Input Low Level	–	–	0.8	V	V _{DD} = 3.0 to 5.25.
V _{IH}	Input High Level	2.1	–	–	V	V _{DD} = 3.0 to 5.25.
V _H	Input Hysteresis	–	60	–	mV	
I _{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C _{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C _{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

11.3.3 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 11-6. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V _{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High	–	1.6	10	mV	
	Power = Medium, Opamp Bias = High	–	1.3	8	mV	
	Power = High, Opamp Bias = High	–	1.2	7.5	mV	
TCV _{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	μV/°C	
I _{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 μA.
C _{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V _{CMOA}	Common Mode Voltage Range. All Cases, except highest. Power = High, Opamp Bias = High	0.0	–	V _{dd}	V	
		0.5	–	V _{dd} - 0.5	V	
CMRR _{OA}	Common Mode Rejection Ratio	60	–	–	dB	
G _{OLOA}	Open Loop Gain	80	–	–	dB	
V _{OHIGHOA}	High Output Voltage Swing (internal signals)	V _{dd} - .01	–	–	V	
V _{OLOWOA}	Low Output Voltage Swing (internal signals)	–	–	0.1	V	
I _{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low	–	150	200	μA	
	Power = Low, Opamp Bias = High	–	300	400	μA	
	Power = Medium, Opamp Bias = Low	–	600	800	μA	
	Power = Medium, Opamp Bias = High	–	1200	1600	μA	
	Power = High, Opamp Bias = Low	–	2400	3200	μA	
	Power = High, Opamp Bias = High	–	4600	6400	μA	
PSRR _{OA}	Supply Voltage Rejection Ratio	67	80	–	dB	V _{ss} ≤ VIN ≤ (V _{dd} - 2.25) or (V _{dd} - 1.25V) ≤ VIN ≤ V _{dd} .

Table 11-7. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V _{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High	–	1.65	10	mV	
	Power = Medium, Opamp Bias = High	–	1.32	8	mV	
	High Power is 5 Volts Only					
TCV _{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	μV/°C	
I _{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 μA.
C _{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V _{CMOA}	Common Mode Voltage Range	0	–	V _{dd}	V	
CMRR _{OA}	Common Mode Rejection Ratio	60	–	–	dB	
G _{OLOA}	Open Loop Gain	80	–	–	dB	
V _{OHIGHOA}	High Output Voltage Swing (internal signals)	V _{dd} - .01	–	–	V	
V _{OLOWOA}	Low Output Voltage Swing (internal signals)	–	–	.01	V	
I _{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low	–	150	200	μA	Not Allowed
	Power = Low, Opamp Bias = High	–	300	400	μA	
	Power = Medium, Opamp Bias = Low	–	600	800	μA	
	Power = Medium, Opamp Bias = High	–	1200	1600	μA	
	Power = High, Opamp Bias = Low	–	2400	3200	μA	
	Power = High, Opamp Bias = High	–	–	–	–	
PSRR _{OA}	Supply Voltage Rejection Ratio	54	80	–	dB	V _{ss} ≤ VIN ≤ (V _{dd} - 2.25) or (V _{dd} - 1.25V) ≤ VIN ≤ V _{dd}

11.3.4 DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 2.4V to 3.0V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 11-8. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Unit
V _{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V _{dd} - 1	V
I _{SLPC}	LPC supply current	–	10	40	μA
V _{OSLPC}	LPC voltage offset	–	2.5	30	mV

11.3.5 DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-9. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit
V _{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV
TCV _{OSOB}	Average Input Offset Voltage Drift	–	+6	–	μV/°C
V _{CMOB}	Common-Mode Input Voltage Range	0.5	–	V _{dd} - 1.0	V
R _{OUTOB}	Output Resistance Power = Low Power = High	– –	– –	1 1	W W
V _{OHIGHOB}	High Output Voltage Swing (Load = 32 ohms to V _{dd} /2) Power = Low Power = High	0.5 x V _{dd} + 1.3 0.5 x V _{dd} + 1.3	– –	– –	V V
V _{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to V _{dd} /2) Power = Low Power = High	– –	– –	0.5 x V _{dd} - 1.3 0.5 x V _{dd} - 1.3	V V
I _{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	– –	1.1 2.6	2 5	mA mA
PSRR _{OB}	Supply Voltage Rejection Ratio	40	64	–	dB

Table 11-10. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
V _{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV
TCV _{OSOB}	Average Input Offset Voltage Drift	–	+6	–	μV/°C
V _{CMOB}	Common-Mode Input Voltage Range	0.5	–	V _{dd} - 1.0	V
R _{OUTOB}	Output Resistance Power = Low Power = High	– –	– –	10 10	W W
V _{OHIGHOB}	High Output Voltage Swing (Load = 1k ohms to V _{dd} /2) Power = Low Power = High	0.5 x V _{dd} + 1.0 0.5 x V _{dd} + 1.0	– –	– –	V V
V _{OLOWOB}	Low Output Voltage Swing (Load = 1k ohms to V _{dd} /2) Power = Low Power = High	– –	– –	0.5 x V _{dd} - 1.0 0.5 x V _{dd} - 1.0	V V
I _{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	– –	0.8 2.0	1 5	mA mA
PSRR _{OB}	Supply Voltage Rejection Ratio	60	64	–	dB

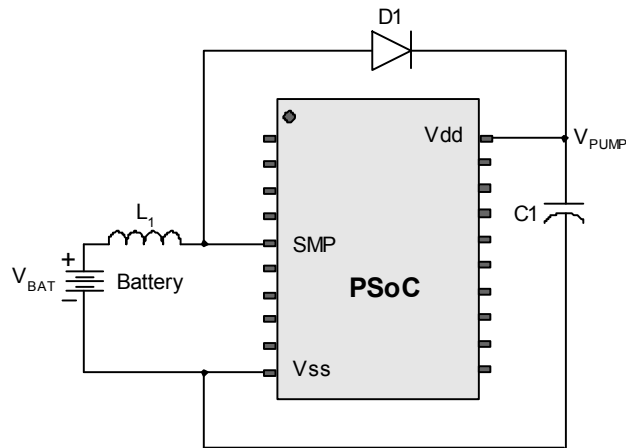
11.3.6 DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-11. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
$V_{PUMP\ 5V}$	5V Output Voltage at Vdd from Pump	4.75	5.0	5.25	V	Configuration of footnote. ^[3] Average, neglecting ripple. SMP trip voltage is set to 5.0V.
$V_{PUMP\ 3V}$	3V Output Voltage at Vdd from Pump	3.00	3.25	3.60	V	Configuration of footnote. ^[3] Average, neglecting ripple. SMP trip voltage is set to 3.25V.
I_{PUMP}	Available Output Current $V_{BAT} = 1.5V, V_{PUMP} = 3.25V$ $V_{BAT} = 1.8V, V_{PUMP} = 5.0V$	8 5	– –	– –	mA mA	Configuration of footnote. ^[3] SMP trip voltage is set to 3.25V. SMP trip voltage is set to 5.0V.
$V_{BAT\ 5V}$	Input Voltage Range from Battery	1.8	–	5.0	V	Configuration of footnote. ^[3] SMP trip voltage is set to 5.0V.
$V_{BAT\ 3V}$	Input Voltage Range from Battery	1.0	–	3.3	V	Configuration of footnote. ^[3] SMP trip voltage is set to 3.25V.
$V_{BAT\ START}$	Minimum Input Voltage from Battery to Start Pump	1.2	–	–	V	Configuration of footnote. ^[3] $0^{\circ}\text{C} \leq T_A \leq 100$. 1.25V at $T_A = -40^{\circ}\text{C}$.
ΔV_{PUMP_Line}	Line Regulation (over V_{BAT} range)	–	5	–	% V_O	Configuration of footnote. ^[3] V_O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 3-15 on page 27.
ΔV_{PUMP_Load}	Load Regulation	–	5	–	% V_O	Configuration of footnote. ^[3] V_O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 3-15 on page 27.
ΔV_{PUMP_Ripple}	Output Voltage Ripple (depends on capacitor/load)	–	100	–	mVp p	Configuration of footnote. ^[3] Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configuration of footnote. ^[3] Load is 5 mA. SMP trip voltage is set to 3.25V.
F_{PUMP}	Switching Frequency	–	1.4	–	MHz	
DC_{PUMP}	Switching Duty Cycle	–	50	–	%	

Figure 11-3. Basic Switch Mode Pump Circuit



Note

3. $L_1 = 2\ \mu\text{H}$ inductor, $C_1 = 10\ \mu\text{F}$ capacitor, $D_1 =$ Schottky diode. See [Figure 11-3.](#)

11.3.7 DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 11-12. 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Unit
V _{BG5}	Bandgap Voltage Reference 5V	1.28	1.30	1.32	V
–	AGND = Vdd/2 ^[4]	Vdd/2 - 0.02	Vdd/2	Vdd/2 + 0.02	V
–	AGND = 2 x BandGap ^[4]	2.52	2.60	2.72	V
–	AGND = P2[4] (P2[4] = Vdd/2) ^[4]	P2[4] - 0.013	P2[4]	P2[4] + 0.013	V
–	AGND = BandGap ^[4]	1.27	1.3	1.34	V
–	AGND = 1.6 x BandGap ^[4]	2.03	2.08	2.13	V
–	AGND Block to Block Variation (AGND = Vdd/2) ^[4]	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + 1.21	Vdd/2 + 1.3	Vdd/2 + 1.382	V
–	RefHi = 3 x BandGap	3.75	3.9	4.05	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	P2[6] + 2.478	P2[6] + 2.6	P2[6] + 2.722	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + 1.218	P2[4] + 1.3	P2[4] + 1.382	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.058	P2[4] + P2[6]	P2[4] + P2[6] + 0.058	V
–	RefHi = 2 x BandGap	2.50	2.60	2.70	V
–	RefHi = 3.2 x BandGap	4.02	4.16	4.29	V
–	RefLo = BandGap	BG - 0.082	BG + 0.023	BG + 0.129	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] - BandGap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

Table 11-13. 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Unit
V _{BG33}	Bandgap Voltage Reference 3.3V	1.28	1.30	1.32	V
–	AGND = Vdd/2 ^[4]	Vdd/2 - 0.02	Vdd/2	Vdd/2 + 0.02	V
–	AGND = 2 x BandGap ^[4]	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.009	P2[4]	P2[4] + 0.009	V
–	AGND = BandGap ^[4]	1.27	1.30	1.34	V
–	AGND = 1.6 x BandGap ^[4]	2.03	2.08	2.13	V
–	AGND Block to Block Variation (AGND = Vdd/2) ^[4]	-0.034	0.000	0.034	mV
–	RefHi = Vdd/2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.042	P2[4] + P2[6]	P2[4] + P2[6] + 0.042	V
–	RefHi = 2 x BandGap	2.50	2.60	2.70	V
–	RefHi = 3.2 x BandGap	Not Allowed			

Note

4. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V.

Table 11-13. 3.3V DC Analog Reference Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit
–	RefLo = Vdd/2 - BandGap		Not Allowed		
–	RefLo = BandGap		Not Allowed		
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)		Not Allowed		
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)		Not Allowed		

11.3.8 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-14. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
R _{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C _{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

11.3.9 DC POR, SMP, and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-15. DC POR, SMP, and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{PPOR0R} V _{PPOR1R} V _{PPOR2R}	Vdd Value for PPOR Trip (positive ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	2.91 4.39 4.55	–	V V V	
V _{PPOR0} V _{PPOR1} V _{PPOR2}	Vdd Value for PPOR Trip (negative ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	2.82 4.39 4.55	–	V V V	
V _{PH0} V _{PH1} V _{PH2}	PPOR Hysteresis PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	92 0 0	–	mV mV mV	
V _{LVD0} V _{LVD1} V _{LVD2} V _{LVD3} V _{LVD4} V _{LVD5} V _{LVD6} V _{LVD7}	Vdd Value for LVD Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.86 2.96 3.07 3.92 4.39 4.55 4.63 4.72	2.92 3.02 3.13 4.00 4.48 4.64 4.73 4.81	2.98 ^[5] 3.08 3.20 4.08 4.57 4.74 ^[6] 4.82 4.91	V V V V V V V V	
V _{PUMP0} V _{PUMP1} V _{PUMP2} V _{PUMP3} V _{PUMP4} V _{PUMP5} V _{PUMP6} V _{PUMP7}	Vdd Value for SMP Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.96 3.03 3.18 4.11 4.55 4.63 4.72 4.90	3.02 3.10 3.25 4.19 4.64 4.73 4.82 5.00	3.08 3.16 3.32 4.28 4.74 4.82 4.91 5.10	V V V V V V V V	

Notes

- Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
- Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

11.3.10 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-16. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I _{DDP}	Supply Current During Programming or Verify	–	10	30	mA	
V _{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V _{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I _{ILP}	Input Current when Applying Vi _{lp} to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I _{IHP}	Input Current when Applying Vi _{hp} to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V _{OLV}	Output Low Voltage During Programming or Verify	–	–	V _{ss} + 0.75	V	
V _{OHV}	Output High Voltage During Programming or Verify	V _{dd} - 1.0	–	V _{dd}	V	
Flash _{ENPB}	Flash Endurance (per block)	50,000 ^[7]	–	–	–	Erase/write cycles per block.
Flash _{ENT}	Flash Endurance (total) ^[8]	1,800,000	–	–	–	Erase/write cycles.
Flash _{DR}	Flash Data Retention	10	–	–	Years	

11.4 AC Electrical Characteristics

11.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Note See the individual user module data sheets for information on maximum frequencies for user modules.

Table 11-17. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6 ^[9,10,11]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See the figure on page 19. SLIMO Mode = 0.
F _{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5 ^[9,10,11]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See the figure on page 19. SLIMO Mode = 1.
F _{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6 ^[9,10]	MHz	
F _{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3 ^[10,11]	MHz	
F _{48M}	Digital PSoC Block Frequency	0	48	49.2 ^[9,10,12]	MHz	Refer to the AC Digital Block Specifications below.
F _{24M}	Digital PSoC Block Frequency	0	24	24.6 ^[10,12]	MHz	
F _{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F _{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle

Notes

- The 50,000 cycle flash endurance per block will only be guaranteed if the flash is operating within one voltage range. Voltage ranges are 3.0V to 3.6V and 4.75V to 5.25V.
- A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information.
- 4.75V < V_{dd} < 5.25V.
- Accuracy derived from Internal Main Oscillator with appropriate trim for V_{dd} range.
- 3.0V < V_{dd} < 3.6V. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.
- See the individual user module data sheets for information on maximum frequencies for user modules

Table 11-17. AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
F _{32K_U}	Internal Low Speed Oscillator (ILO) Untrimmed Frequency	5	–	–	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this
F _{PLL}	PLL Frequency	–	23.986	–	MHz	A multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	
T _{PLLSLEW}	PLL Lock Time	0.5	–	10	ms	
T _{PLLSLEWLOW}	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T _{OS}	External Crystal Oscillator Startup to 1%	–	250	500	ms	
T _{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	300	600	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T _{OSACC} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V ≤ Vdd ≤ 5.5V, -40 °C ≤ T _A ≤ 85 °C.
Jitter32k	32 kHz Period Jitter	–	100	–	ns	
T _{XRST}	External Reset Pulse Width	10	–	–	μs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
DC _{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
F _{out48M}	48 MHz Output Frequency	46.8	48.0	49.2 ^[9, 11]	MHz	Trimmed. Using factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	–	600	–	ps	
F _{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T _{RAMP}	Supply Ramp Time	0	–	–	μs	
T _{POWERUP}	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0V. See the System Resets section of the PSoC Technical Reference Manual.

Figure 11-4. PLL Lock Timing Diagram

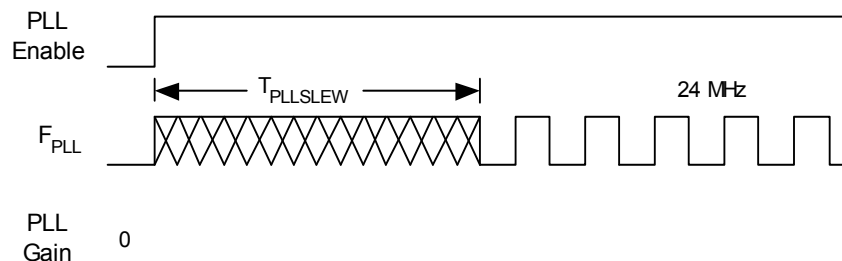
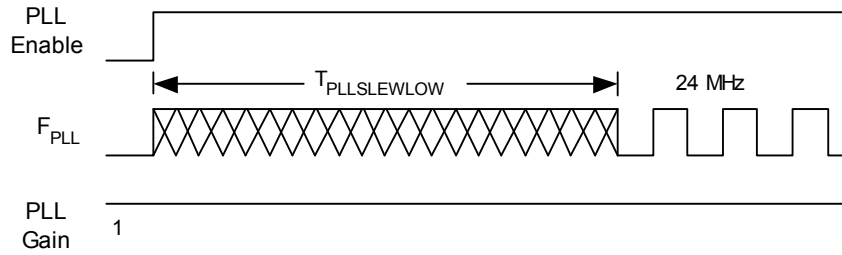
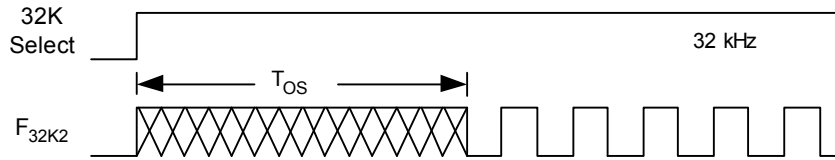
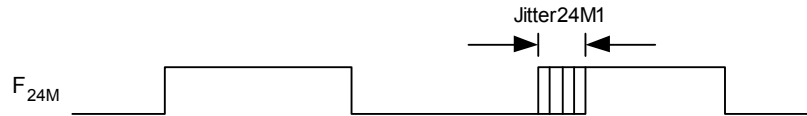


Figure 11-5. PLL Lock for Low Gain Setting Timing Diagram

Figure 11-6. External Crystal Oscillator Startup Timing Diagram

Figure 11-7. 24 MHz Period Jitter (IMO) Timing Diagram

Figure 11-8. 32 kHz Period Jitter (ECO) Timing Diagram

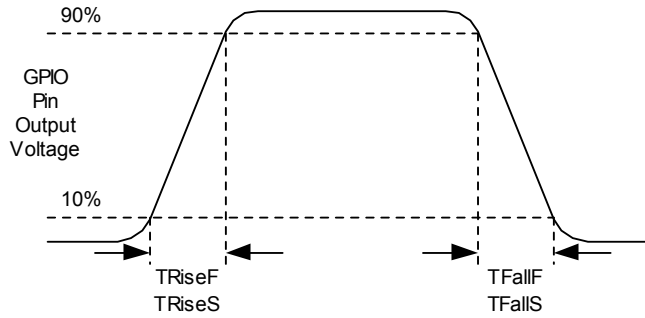

11.4.2 AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-18. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12.3	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cloud = 50 pF	3	–	18	ns	Vdd = 4.75 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cloud = 50 pF	2	–	18	ns	Vdd = 4.75 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cloud = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cloud = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Figure 11-9. GPIO Timing Diagram



11.4.3 AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 11-19. 5V AC Operational Amplifier Specifications

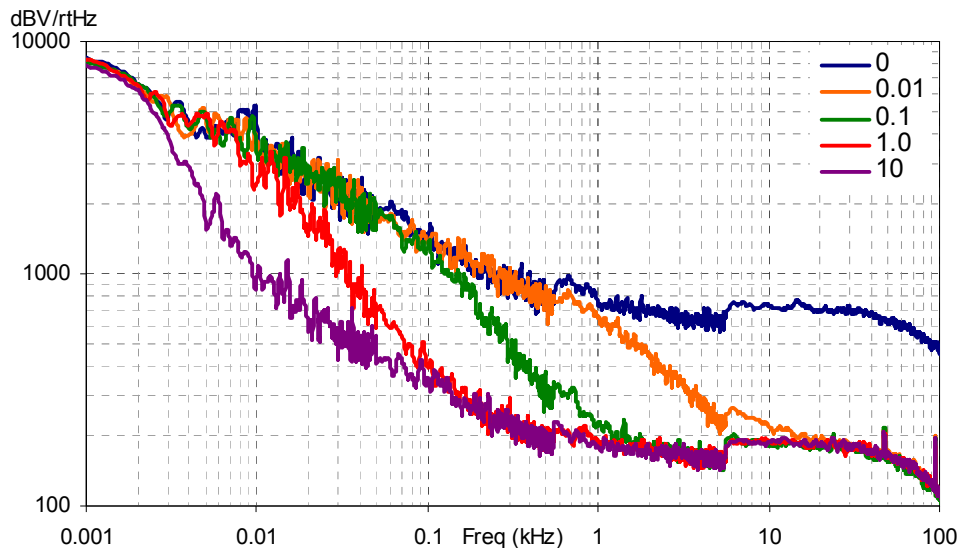
Symbol	Description	Min	Typ	Max	Unit
T_{ROA}	Rising Settling Time to 0.1% for a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	– – –	– – –	3.9 0.72 0.62	μs μs μs
T_{SOA}	Falling Settling Time to 0.1% for a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	– – –	– – –	5.9 0.92 0.72	μs μs μs
SR_{ROA}	Rising Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	0.15 1.7 6.5	– – –	– – –	$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$
SR_{FOA}	Falling Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	0.01 0.5 4.0	– – –	– – –	$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	0.75 3.1 5.4	– – –	– – –	MHz MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

Table 11-20. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T _{ROA}	Rising Settling Time to 0.1% of a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	– –	– –	3.92 0.72	μs μs
T _{SOA}	Falling Settling Time to 0.1% of a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	– –	– –	5.41 0.72	μs μs
SR _{ROA}	Rising Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	0.31 2.7	– –	– –	V/μs V/μs
SR _{FOA}	Falling Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	0.24 1.8	– –	– –	V/μs V/μs
BW _{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	0.67 2.8	– –	– –	MHz MHz
E _{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

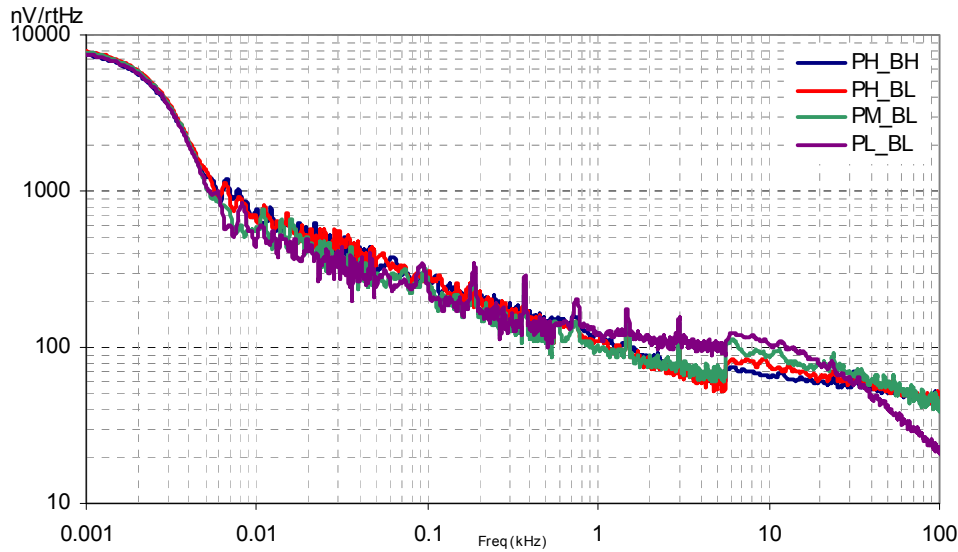
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 11-10. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to $1/f$, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 11-11. Typical Opamp Noise



11.4.4 AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 2.4V to 3.0V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 11-21. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
T_{RLPC}	LPC response time	–	–	50	μs	≥ 50 mV overdrive comparator reference set within V_{REFLPC} .

11.4.5 AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-22. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All Functions	Maximum Block Clocking Frequency (> 4.75V)			49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Block Clocking Frequency (< 4.75V)			24.6	MHz	3.0V < Vdd < 4.75V.
Timer	Capture Pulse Width	50 ^[13]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50 ^[13]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50 ^[13]	–	–	ns	
	Disable Mode	50 ^[13]	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.

Note

13. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 11-22. AC Digital Block Specifications (continued)

Function	Description	Min	Typ	Max	Unit	Notes
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V < V _{dd} < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50 ^[13]	–	–	MHz	
Transmitter	Maximum Input Clock Frequency V _{dd} ≥ 4.75V, 2 Stop Bits	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking. Maximum data rate at 6.15 MHz due to 8 x over clocking.
		–	–	49.2	MHz	
Receiver	Maximum Input Clock Frequency V _{dd} ≥ 4.75V, 2 Stop Bits	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking. Maximum data rate at 6.15 MHz due to 8 x over clocking.
		–	–	49.2	MHz	

11.4.6 AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-23. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit
T _{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	–	–	4	μs
		–	–	4	μs
T _{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	–	–	3.4	μs
		–	–	3.4	μs
SR _{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load Power = Low Power = High	0.5	–	–	V/μs
		0.5	–	–	V/μs
SR _{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load Power = Low Power = High	0.55	–	–	V/μs
		0.55	–	–	V/μs
BW _{OB}	Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100pF Load Power = Low Power = High	0.8	–	–	MHz
		0.8	–	–	MHz
BW _{OB}	Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100pF Load Power = Low Power = High	300	–	–	kHz
		300	–	–	kHz

Table 11-24. 3.3V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Unit
T _{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	–	–	4.7	μs
		–	–	4.7	μs
T _{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	–	–	4	μs
		–	–	4	μs
SR _{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load Power = Low Power = High	.36	–	–	V/μs
		.36	–	–	V/μs
SR _{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load Power = Low Power = High	.4	–	–	V/μs
		.4	–	–	V/μs
BW _{OB}	Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100pF Load Power = Low Power = High	0.7	–	–	MHz
		0.7	–	–	MHz
BW _{OB}	Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100pF Load Power = Low Power = High	200	–	–	kHz
		200	–	–	kHz

11.4.7 AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-25. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Unit
F _{OSCEXT}	Frequency	0.093	–	24.6	MHz
–	High Period	20.6	–	5300	ns
–	Low Period	20.6	–	–	ns
–	Power Up IMO to Switch	150	–	–	ms

Table 11-26. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Unit
F _{OSCEXT}	Frequency with CPU Clock divide by 1	0.093	–	12.3	MHz
F _{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.186	–	24.6	MHz
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns
–	Power Up IMO to Switch	150	–	–	μs

11.4.8 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-27. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
T _{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T _{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T _{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T _{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F _{SCLK}	Frequency of SCLK	0	–	8	MHz	
T _{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T _{WRITE}	Flash Block Write Time	–	40	–	ms	
T _{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	V _{dd} > 3.6
T _{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ V _{dd} ≤ 3.6
T _{ERASEALL}	Flash Erase Time (Bulk)	–	80	–	ms	Erase all Blocks and protection fields at once
T _{PROGRAM_HOT}	Flash Block Erase + Flash Block Write Time	–	–	100 ^[14]	ms	0°C ≤ T _j ≤ 100°C
T _{PROGRAM_COLD}	Flash Block Erase + Flash Block Write Time	–	–	200 ^[14]	ms	-40°C ≤ T _j ≤ 0°C

Note

14. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information

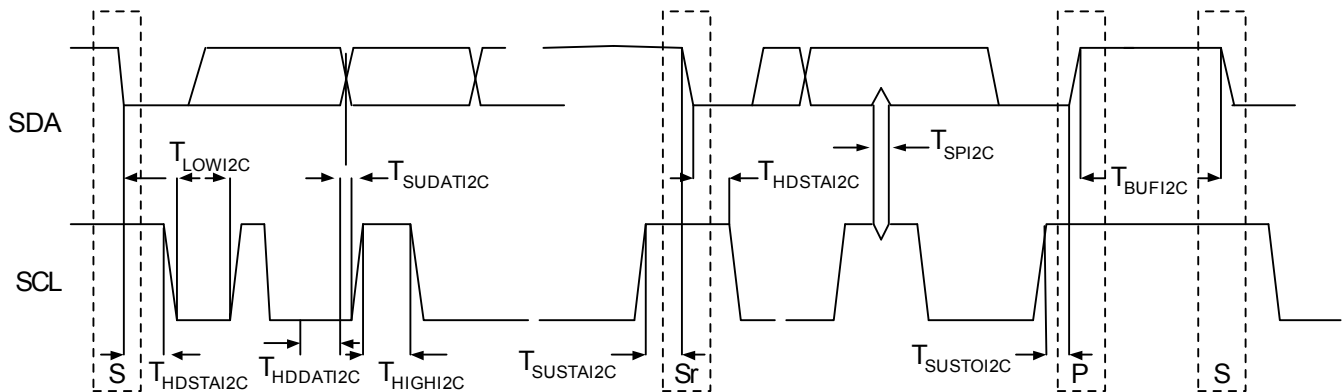
11.4.9 AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11-28. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
F _{SCL I2C}	SCL Clock Frequency	0	100	0	400	kHz
T _{HDSTAI2C}	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	μs
T _{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	μs
T _{HIGHI2C}	HIGH Period of the SCL Clock	4.0	–	0.6	–	μs
T _{SUSTA I2C}	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	μs
T _{HDDAT I2C}	Data Hold Time	0	–	0	–	μs
T _{SUDAT I2C}	Data Set-up Time	250	–	100 ^[15]	–	ns
T _{SUSTO I2C}	Set-up Time for STOP Condition	4.0	–	0.6	–	μs
T _{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	μs
T _{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns

Figure 11-12. Definition for Timing for Fast/Standard Mode on the I2C Bus



Note

15. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{\text{SU;DAT}} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{\text{rmax}} + t_{\text{SU;DAT}} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

12. Packaging Information

This section illustrates the packaging specifications for the CY8C27x43 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at <http://www.cypress.com/design/MR10161>.

12.1 Packaging Dimensions

Figure 12-1. 28-Pin (300 mil) Molded DIP

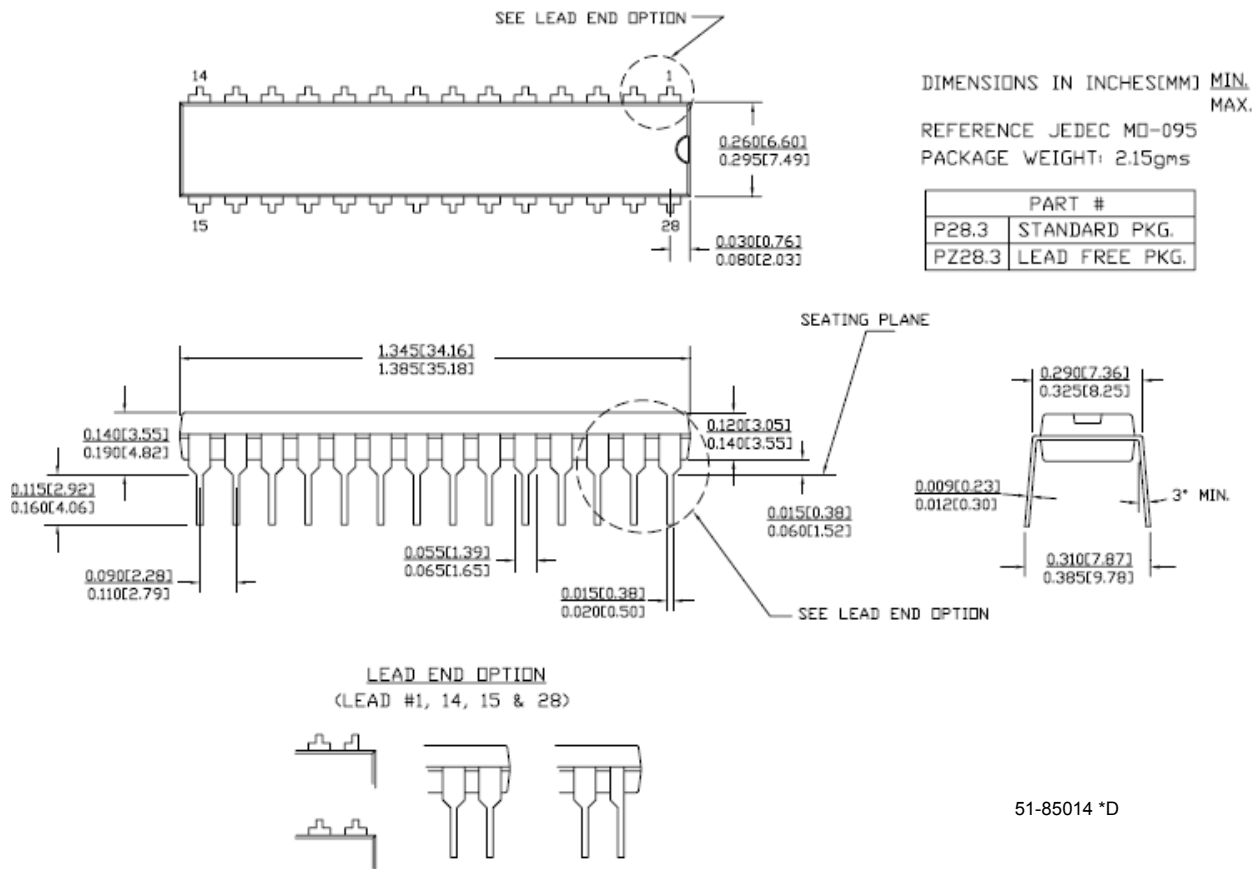


Figure 12-2. 28-Pin (210-Mil) SSOP

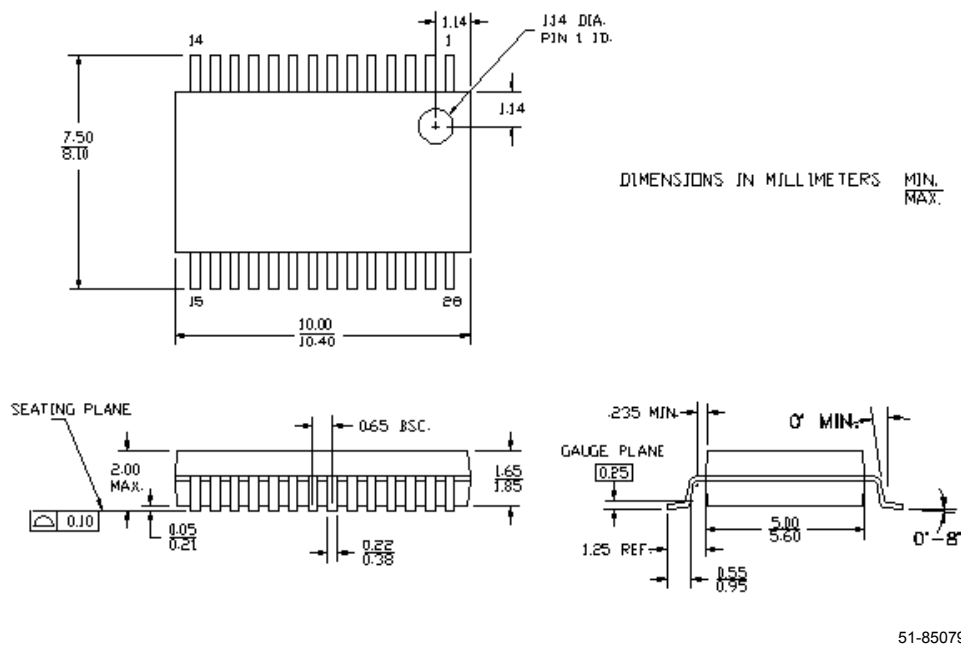


Figure 12-3. 28-Pin (300-Mil) SOIC

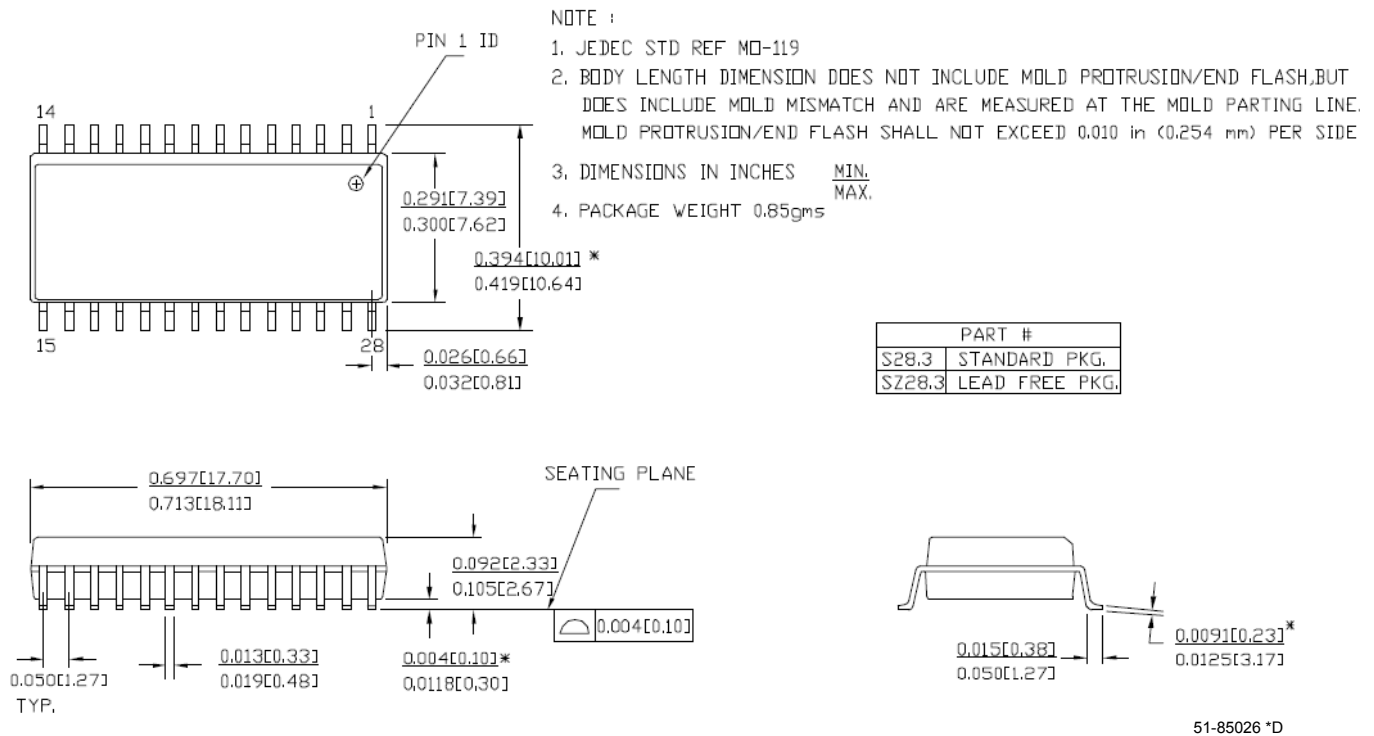


Figure 12-4. 44-Pin TQFP

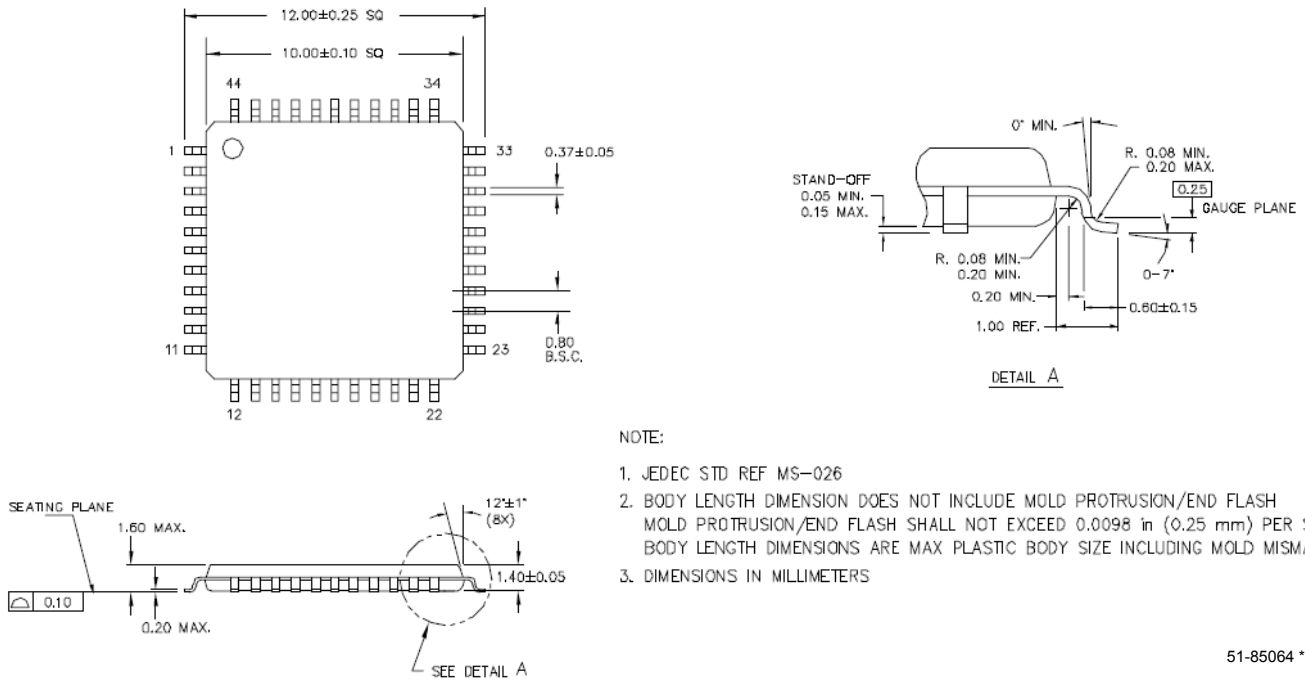


Figure 12-5. 48-Pin (300-Mil) SSOP

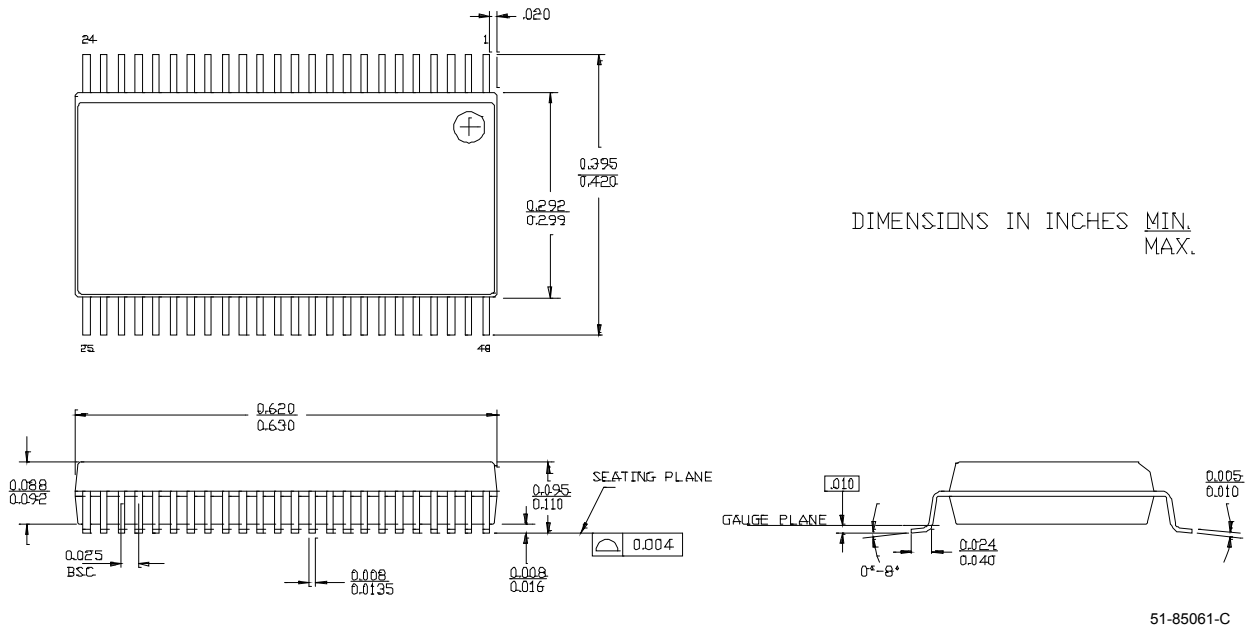
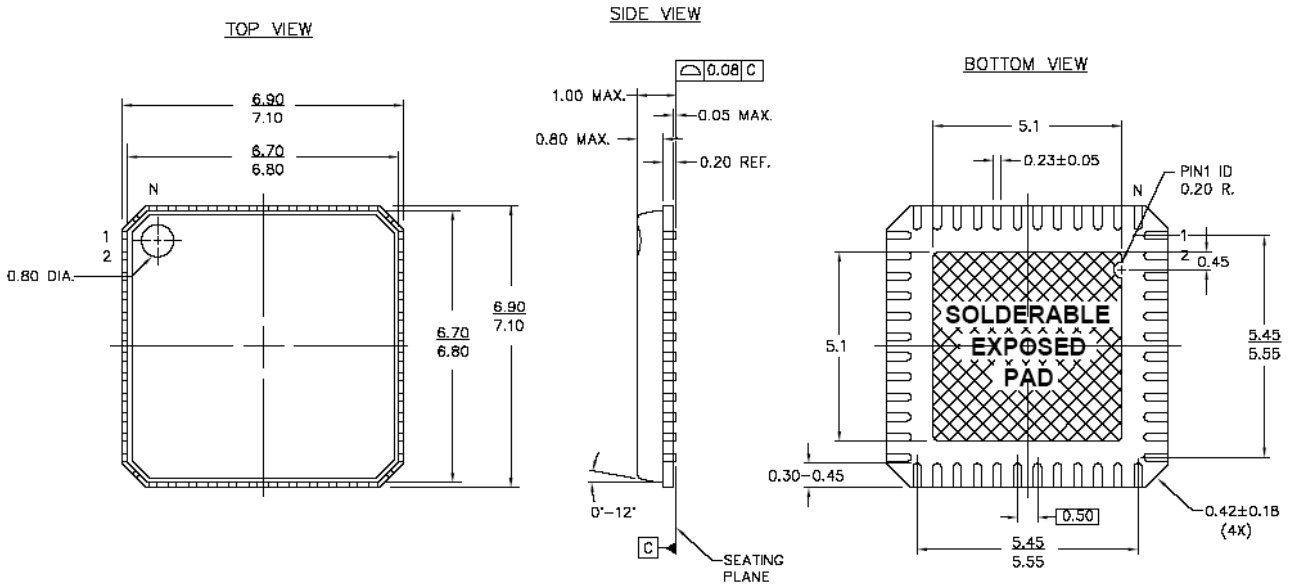



Figure 12-6. 48-Pin (7x7 mm) QFN



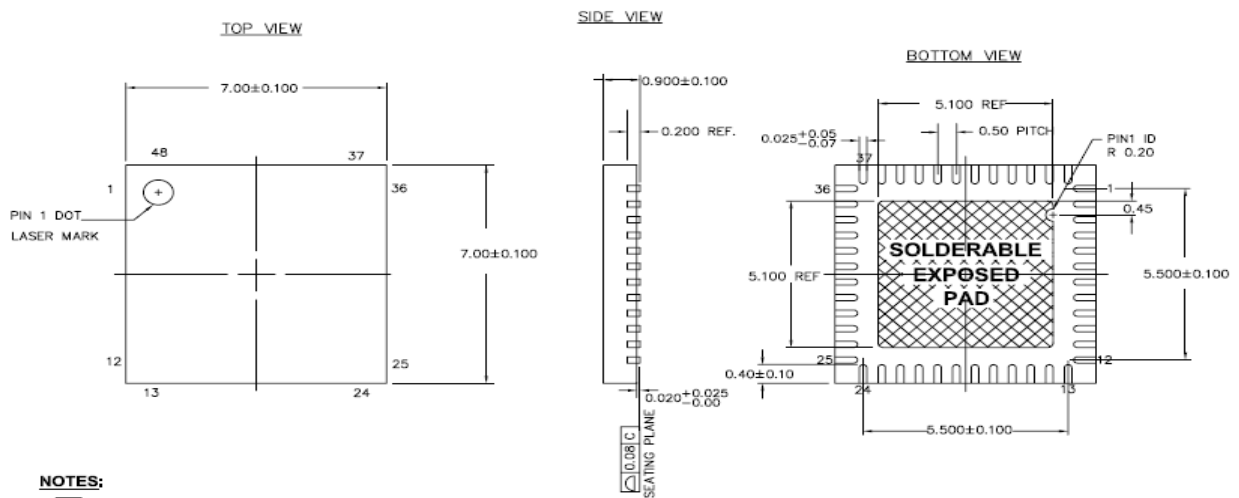
NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE


PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919 *A

Figure 12-7. 48-Pin QFN 7x7x 0.90 MM (Sawn Type)

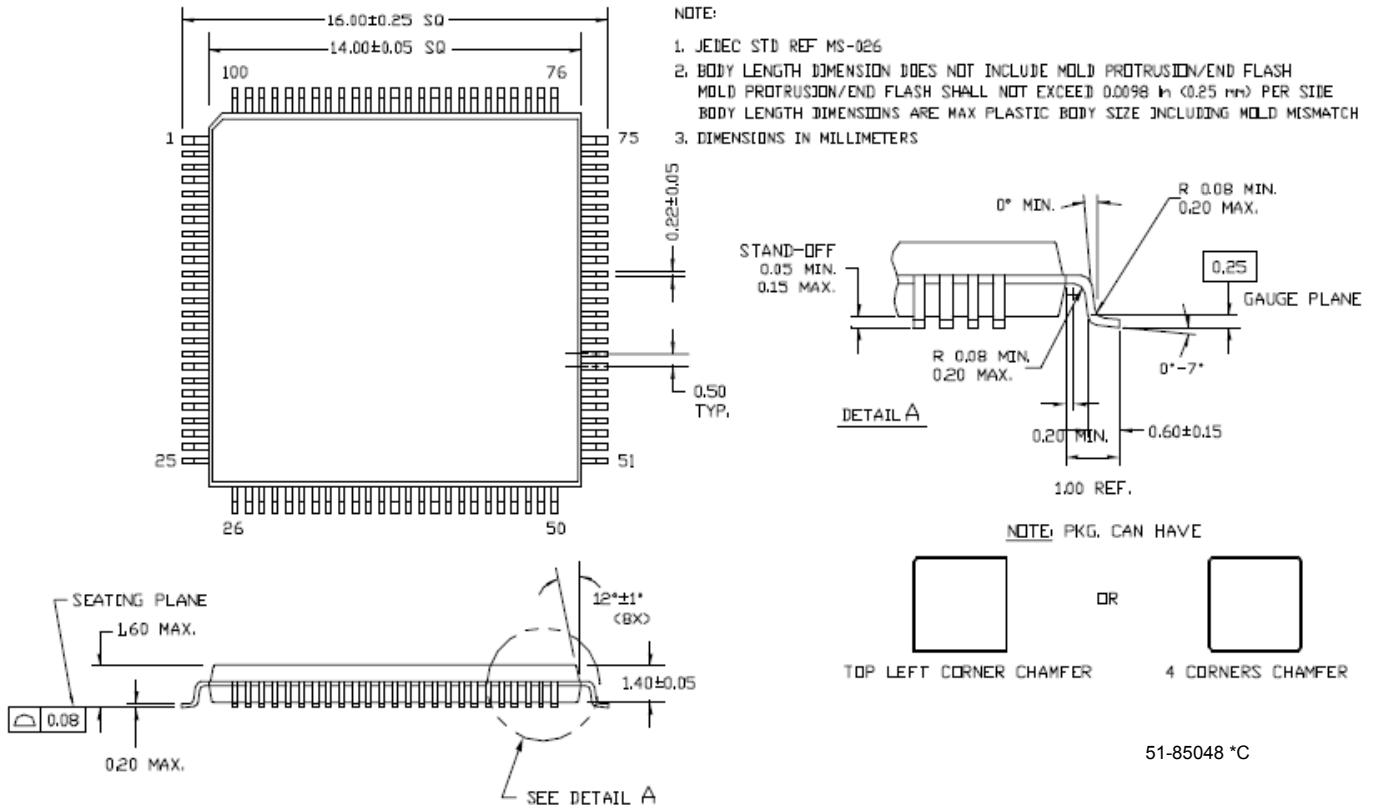


NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *C

Figure 12-8. 100-Pin TQFP



Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Important Note Pinned vias for thermal conduction are not required for the low-power PSoC device.

12.1 Thermal Impedances

Table 12-1. Thermal Impedances per Package

Package	Typical θ_{JA} *
28 PDIP	69 °C/W
28 SSOP	94 °C/W
28 SOIC	67 °C/W
44 TQFP	60 °C/W
48 SSOP	69 °C/W
48 QFN**	28 °C/W
100 TQFP	50 °C/W

* $T_J = T_A + \text{POWER} \times \theta_{JA}$

** To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.

12.2 Capacitance on Crystal Pins

Table 12-2. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28 PDIP	3.5 pF
28 SSOP	2.8 pF
28 SOIC	2.7 pF
44 TQFP	2.6 pF
48 SSOP	3.3 pF
48 QFN	1.8 pF
100 TQFP	3.1 pF

12.3 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 12-3. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature*	Maximum Peak Temperature
28 PDIP	220°C	260°C
28 SSOP	240°C	260°C
28 SOIC	220°C	260°C
44 TQFP	220°C	260°C
48 SSOP	220°C	260°C
48 QFN	220°C	260°C
100 TQFP	220°C	260°C

*Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

13. Development Tool Selection

This chapter presents the development tools available for all current PSoC device families including the CY8C27x43 family.

13.1 Software

13.1.1 PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at <http://www.cypress.com/psocdesigner> and includes a free C compiler.

13.1.2 PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at <http://www.cypress.com/psocprogrammer>.

13.2 Development Kits

All development kits can be purchased from the Cypress Online Store.

13.2.1 CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

13.2.2 CY3210-ExpressDK PSoC Express Development Kit

The CY3210-ExpressDK is for advanced prototyping and development with PSoC Express (may be used with ICE-Cube In-Circuit Emulator). It provides access to I²C buses, voltage reference, switches, upgradeable modules and more. The kit includes:

- PSoC Express Software CD
- Express Development Board
- 4 Fan Modules
- 2 Proto Modules
- MiniProg In-System Serial Programmer
- MiniEval PCB Evaluation Board
- Jumper Wire Kit
- USB 2.0 Cable
- Serial Cable (DB9)
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- 2 CY8C24423A-24PXI 28-PDIP Chip Samples
- 2 CY8C27443-24PXI 28-PDIP Chip Samples
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

13.3 Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

13.3.1 CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

13.3.2 CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

13.3.3 CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MiniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

13.4 Device Programmers

All device programmers can be purchased from the Cypress Online Store.

13.4.1 CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular

programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

13.4.2 CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

14. Accessories (Emulation and Programming)

Table 14-1. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit ^[16]	Foot Kit ^[17]	Adapter ^[18]
CY8C29466-24PXI	28 PDIP	CY3250-29XXX	CY3250-28PDIP-FK	Adapters can be found at http://www.emulation.com .
CY8C29466-24PVXI	28 SSOP	CY3250-29XXX	CY3250-28SSOP-FK	
CY8C29466-24SXI	28 SOIC	CY3250-29XXX	CY3250-28SOIC-FK	
CY8C29566-24AXI	44 TQFP	CY3250-29XXX	CY3250-44TQFP-FK	
CY8C29666-24PVXI	48 SSOP	CY3250-29XXX	CY3250-48SSOP-FK	
CY8C29666-24LFXI	48 QFN	CY3250-29XXXQFN	CY3250-48QFN-FK	
CY8C29866-24AXI	100 TQFP	CY3250-29XXX	CY3250-100TQFP-FK	
CY8C29466-24PXI	28 PDIP	CY3250-29XXX	CY3250-28PDIP-FK	Adapters can be found at http://www.emulation.com .

14.1 Third Party Tools

Several tools have been specially designed by the following 3rd-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at <http://www.cypress.com> under DESIGN RESOURCES >> Evaluation Boards.

14.2 Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note “[Debugging - Build a PSoC Emulator into Your Board - AN2323](#)”.

Notes

16. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.

17. Foot kit includes surface mount feet that can be soldered to the target PCB.

18. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at <http://www.emulation.com>

15. Ordering Information

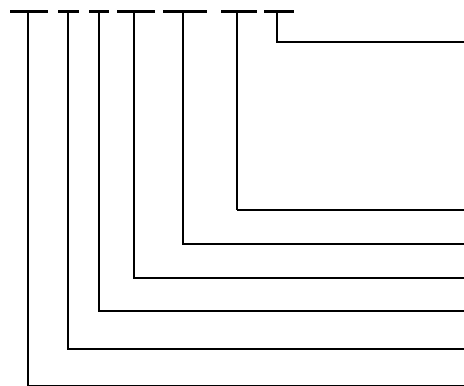
The following table lists the CY8C27x43 PSoC device's key package features and ordering codes.

Package	Ordering Code	Flash (Bytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital PSoC Blocks	Analog PSoC Blocks	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
28 Pin (300 Mil) DIP	CY8C29466-24PXI	32K	2K	Yes	-40C to +85C	16	12	24	12	4	Yes
28 Pin (210 Mil) SSOP	CY8C29466-24PVXI	32K	2K	Yes	-40C to +85C	16	12	24	12	4	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C29466-24PVXIT	32K	2K	Yes	-40C to +85C	16	12	24	12	4	Yes
28 Pin (300 Mil) SOIC	CY8C29466-24SXI	32K	2K	Yes	-40C to +85C	16	12	24	12	4	Yes
28 Pin (300 Mil) SOIC (Tape and Reel)	CY8C29466-24SXIT	32K	2K	Yes	-40C to +85C	16	12	24	12	4	Yes
44 Pin TQFP	CY8C29566-24AXI	32K	2K	Yes	-40C to +85C	16	12	40	12	4	Yes
44 Pin TQFP (Tape and Reel)	CY8C29566-24AXIT	32K	2K	Yes	-40C to +85C	16	12	40	12	4	Yes
48 Pin (300 Mil) SSOP	CY8C29666-24PVXI	32K	2K	Yes	-40C to +85C	16	12	44	12	4	Yes
48 Pin (300 Mil) SSOP (Tape and Reel)	CY8C29666-24PVXIT	32K	2K	Yes	-40C to +85C	16	12	44	12	4	Yes
48 Pin QFN	CY8C29666-24LFXI	32K	2K	Yes	-40C to +85C	16	12	44	12	4	Yes
100 Pin TQFP	CY8C29866-24AXI	32K	2K	Yes	-40C to +85C	16	12	64	12	4	Yes
100 Pin OCD TQFP ^{19]}	CY8C29000-24AXI	32K	2K	Yes	-40C to +85C	16	12	64	12	4	Yes
48-Pin (7X7X 1.0 MM) QFN (Sawn)	CY8C29666-24LTXI	32K	2K	Yes	-40C to +85C	16	12	44	12	4	Yes
48-Pin (7X7X 1.0 MM) QFN (Sawn)	CY8C29666-24LTXIT	32K	2K	Yes	-40C to +85C	16	12	44	12	4	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

16. Ordering Code Definitions

CY 8 C 29 xxx-SPxx



Package Type:
 PX = PDIP Pb-Free
 SX = SOIC Pb-Free
 PVX = SSOP Pb-Free
 LFX/LKX = QFN Pb-Free
 AX = TQFP Pb-Free

Thermal Rating:
 C = Commercial
 I = Industrial
 E = Extended

Speed: 24 MHz

Part Number

Family Code

Technology Code: C = CMOS

Marketing Code: 8 = Cypress PSoC

Company ID: CY = Cypress

Note

¹⁹. This part may be used for in-circuit debugging. It is NOT available for production.

17. Document History Page

Document Title: CY8C29466, CY8C29566, CY8C29666, and CY8C29866 PSoC® Programmable System-on-Chip™ Document Number: 38-12013				
Revision	ECN No.	Submission Date	Origin of Change	Description of Change
**	131151	11/13/2003	New Silicon	New document (Revision **).
*A	132848	01/21/2004	NWJ	New information. First edition of preliminary data sheet.
*B	133205	01/27/2004	NWJ	Changed part numbers, increased SRAM data storage to 2K bytes.
*C	133656	02/09/2004	SFV	Changed part numbers and removed a 28-pin SOIC.
*D	227240	06/01/2004	SFV	Changes to Overview section, 48-pin MLF pinout, and significant changes to the Electrical Specs.
*E	240108	See ECN	SFV	Added a 28-lead (300 mil) SOIC part.
*F	247492	See ECN	SFV	New information added to the Electrical Specifications chapter.
*G	288849	See ECN	HMT	Add DS standards, update device table, fine-tune pinouts, add Reflow Peak Temp. table. Finalize.
*H	722736	See ECN	HMT	Add QFN package clarifications. Add new QFN diagram. Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add CY8C20x34 to PSoC Device Characteristics table. Update emulation pod/feet kit part numbers. Add OCD non-production pinouts and package diagrams. Add ISSP note to pinout tables. Update package diagram revisions. Update typical and recommended Storage Temperature per industrial specs. Update CY branding and QFN convention. Add new Dev. Tool section. Update copyright and trademarks.
*I	2503350	See ECN	DFK/PYRS	Pinout for CY8C29000 OCD wrongly included details of CY8C24X94. The correct pinout for CY8C29000 is included in this version. Added note on digital signaling in "DC Analog Reference Specifications" section.
*J	2545030	07/29/08	YARA	Added note to Ordering Information
*K	2708295	04/22/2009	JVY	<p>Changed title from "CY8C29466, CY8C29566, CY8C29666, and CY8C29866 PSoC Mixed Signal Array Final Data Sheet" to "CY8C29466, CY8C29566, CY8C29666, and CY8C29866 PSoC® Programmable System-on-Chip™"</p> <p>Updated to data sheet template</p> <p>Added 48-Pin QFN (Sawn) package diagram and CY8C29666-24LTXI and CY8C29666-24LTXIT part details in the Ordering Information table</p> <p>Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows:</p> <p>Modified F_{IMO6} (page 27), T_{WRITE} specifications (page 34)</p> <p>Added I_{OH} (page 21), I_{OL} (page 21), DC_{ILO} (page 28), F_{32K_U} (page 27), T_{POWERUP} (page 28), T_{ERASEALL} (page 34), T_{PROGRAM_HOT} (page 34), and T_{PROGRAM_COLD} (page 34) specifications</p>

18. Sales, Solutions, and Legal Information

18.1 Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

18.2 Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com

18.3 PSoC Solutions

General	psoc.cypress.com/solutions
Low Power/Low Voltage	psoc.cypress.com/low-power
Precision Analog	psoc.cypress.com/precision-analog
LCD Drive	psoc.cypress.com/lcd-drive
CAN 2.0b	psoc.cypress.com/can
USB	psoc.cypress.com/usb

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