



**CY8C28243, CY8C28403, CY8C28413
 CY8C28433, CY8C28445, CY8C28452
 CY8C28513, CY8C28533, CY8C28545
 CY8C28623, CY8C28643, CY8C28645**

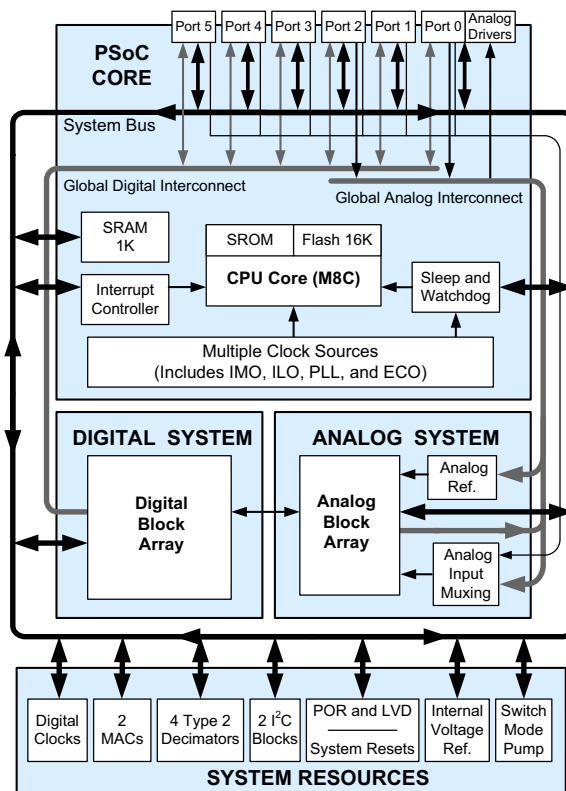
PSoC[®] Programmable System-on-Chip

Features

- Varied Resource Options Within One PSoC[®] Device Group
- Powerful Harvard Architecture Processor
 - M8C Processor Speeds up to 24 MHz
 - 8x8 Multiply, 32-Bit Accumulate
 - Low Power at High Speed
 - 3.0V to 5.25V Operating Voltage
 - Operating Voltages Down to 1.5V Using On-Chip Switched Mode Pump (SMP)
 - Industrial Temperature Range: -40°C to +85°C
- Advanced Reconfigurable Peripherals (PSoC Blocks)
 - Up to 12 Rail-to-Rail Analog PSoC Blocks Provide:
 - Up to 14-Bit ADCs
 - Up to 9-Bit DACs
 - Programmable Gain Amplifiers
 - Programmable Filters and Comparators
 - Multiple ADC configurations
 - Dedicated SAR ADC, up to 142 ksp/s with Sample and Hold
 - Up to 4 Synchronized or Independent Delta-Sigma ADCs for Advanced Applications
 - Up to 4 Limited Type E Analog Blocks Provide:
 - Dual Channel Capacitive Sensing Capability
 - Comparators with Programmable DAC Reference
 - Up to 10-bit Single-Slope ADCs
 - Up to 12 Digital PSoC Blocks Provide:
 - 8 to 32-Bit Timers, Counters, and PWMs
 - Shift Register, CRC, and PRS Modules
 - Up to 3 Full-Duplex UARTs
 - Up to 6 Half-Duplex UARTs
 - Multiple Variable Data Length SPI[™] Masters or Slaves
 - Connectable to All GPIO
 - Complex Peripherals by Combining Blocks
- Precision, Programmable Clocking
 - Internal ±2.5% 24/48 MHz Main Oscillator
 - Optional 32.768 kHz Crystal for Precise On-Chip Clocks
 - Optional External Oscillator, up to 24 MHz
 - Internal Low Speed, Low Power Oscillator for Watchdog and Sleep Functionality
- Flexible On-Chip Memory
 - 16K Bytes Flash Program Storage 50,000 Erase/Write Cycles
 - 1K Bytes SRAM Data Storage
 - In-System Serial Programming (ISSP[™])
 - Partial Flash Updates
 - Flexible Protection Modes
 - EEPROM Emulation in Flash
- Programmable Pin Configurations
 - 25 mA Sink, 10 mA Drive on All GPIO

- Pull Up, Pull Down, High Z, Strong, or Open Drain Drive Modes on All GPIO
- Analog Input on All GPIO
- 30 mA Analog Outputs on GPIO
- Configurable Interrupt on All GPIO
- Additional System Resources
 - Up to 2 Hardware I²C Resources
 - Each Resource Implements Slave, Master, or Multi-Master Modes
 - Operation Between 0 and 400 kHz
 - Watchdog and Sleep Timers
 - User-Configurable Low Voltage Detection
 - Flexible Internal Voltage References
 - Integrated Supervisory Circuit
 - On-Chip Precision Voltage Reference
- Complete Development Tools
 - Free Development Software (PSoC Designer[™])
 - Full Featured In-Circuit Emulator, and Programmer
 - Full Speed Emulation
 - Flexible and Functional Breakpoint Structure
 - 128K Trace Memory

System Block Diagram



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PSoC Functional Overview

The PSoC family consists of many devices with On-Chip Controllers. These devices are designed to replace multiple traditional MCU based system components with one low cost single chip programmable component. A PSoC device includes configurable analog blocks, digital blocks, and interconnections. This architecture enables the user to create customized peripheral configurations to match the requirements of each individual application. In addition, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The CY8C28xxx group of PSoC devices described in this data sheet have multiple resource configuration options available. Therefore, not every resource mentioned in this data sheet is available for each CY8C28xxx subgroup. The CY8C28x45 subgroup has a full feature set of all resources described. There are six more segmented subgroups that allow designers to use a device with only the resources and functionality necessary for a specific application. See [Table 2](#) on page 7 to determine the resources available for each CY8C28xxx subgroup. The same information is also presented in more detail in the [Ordering Information](#) section.

The architecture for this specific PSoC device family, as shown in the [System Block Diagram](#) on page 1, consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. The configurable global bus system allows all the device resources to be combined into a complete custom system. PSoC CY8C28xxx family devices have up to six I/O ports that connect to the global digital and analog interconnects, providing access to up to 12 digital blocks and up to 16 analog blocks.

The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general Purpose I/O (GPIO). The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microcontroller.

Memory encompasses 16K bytes of Flash for program storage, 1K bytes of SRAM for data storage. The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 2.5% over temperature and voltage. A low power 32 kHz internal low speed oscillator (ILO) is provided for the sleep timer and watch dog timer (WDT). The 32.768 kHz external crystal oscillator (ECO) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL.

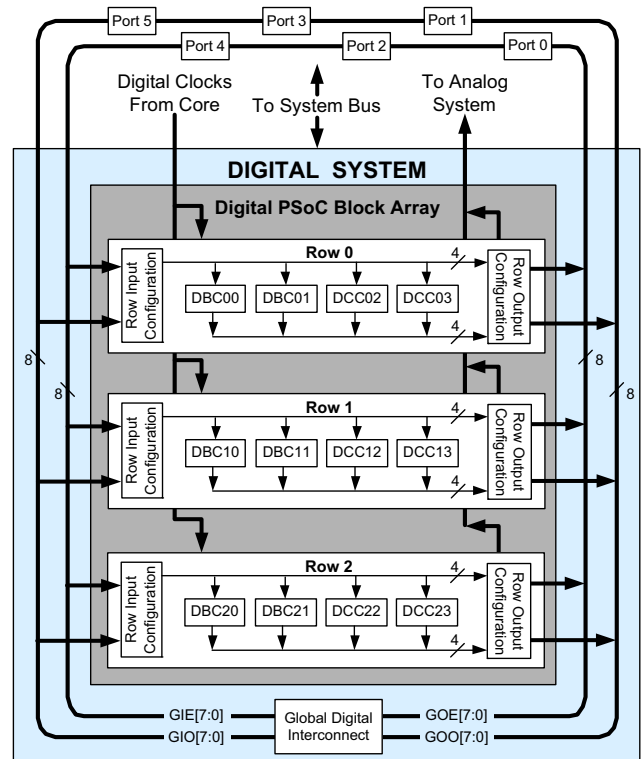
PSoC GPIOs provide connections to the CPU, and digital and analog resources. Each pin's drive mode may be selected from 8 options, which allows great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of up to 12 configurable digital PSoC blocks. Each block is an 8-bit resource that can be used

alone or combined with other blocks to create 8, 16, 24, and 32-bit peripherals, which are called user modules. The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin.

Figure 1. Digital System Block Diagram^[1]



Digital peripheral configurations include:

- PWMs (8 to 16 bit, One-shot and Multi-shot capability)
- PWMs with Dead band/Kill (8 to 16 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- Full-duplex 8-bit UARTs (up to 3) with selectable parity
- Half-duplex 8-bit UARTs (up to 6) with selectable parity
- Variable length SPI slave and master
 - Up to 6 total slaves and masters (8-bit)
 - Supports 8 to 16 bit operation
- I²C slave, master, or multi-master (up to 2 available as System Resources)
- IrDA (up to 3)
- Pseudo Random Sequence Generators (8 to 32 bit)
- Cyclical Redundancy Checker/Generator (16 bit)
- Shift Register (2 to 32 bit)

Note

1. CY8C28x52 devices do not have digital block row 2. They have two digital rows with eight total digital blocks.

The Analog System

The Analog System is composed of up to 16 configurable analog blocks, each containing an opamp circuit that allows the creation of complex analog signal flows. Some devices in this PSoC family have an analog multiplex bus that can connect to every GPIO pin. This bus can also connect to the analog system for analysis with comparators and analog-to-digital converters. It can be split into two sections for simultaneous dual-channel processing.

Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (6 to 14-bit resolution, up to 4, selectable as Incremental or Delta Sigma)
- Dedicated 10-bit SAR ADC with sample rates up to 142 ksp/s
- Synchronized, simultaneous Delta Sigma ADCs (up to 4)
- Filters (2 to 8 pole band-pass, low pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 6, with 16 selectable thresholds)
- DACs (up to 4, with 6 to 9-bit resolution)
- Multiplying DACs (up to 4, with 6 to 9-bit resolution)
- High current output drivers (up to 4 with 30 mA drive)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Figure 2. Analog System Block Diagram for CY8C28x45 and CY8C28x52 Devices

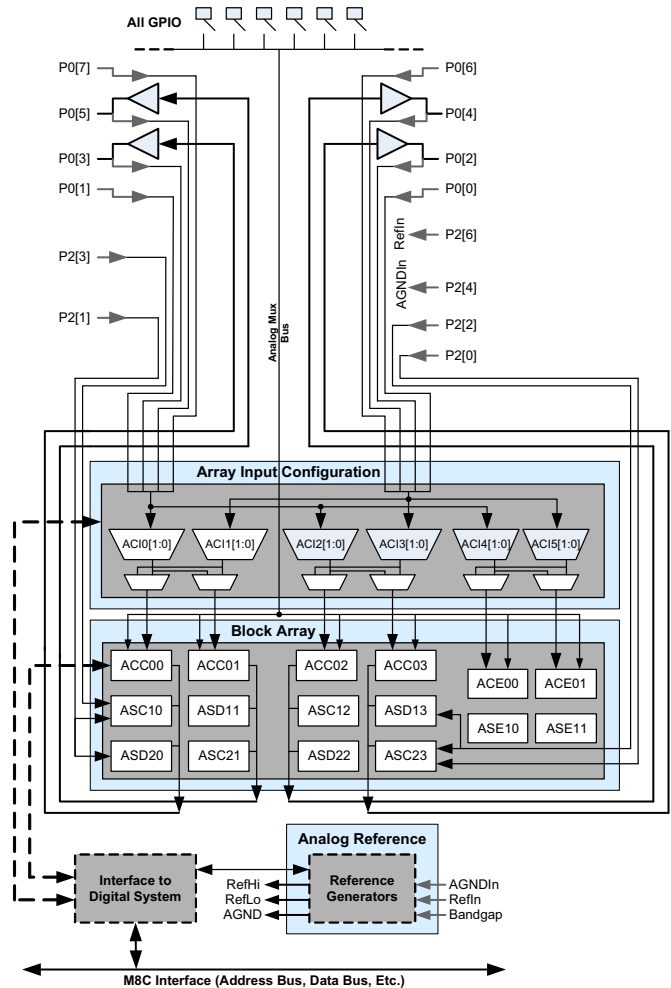


Figure 3. Analog System Block Diagram for CY8C28x43 Devices

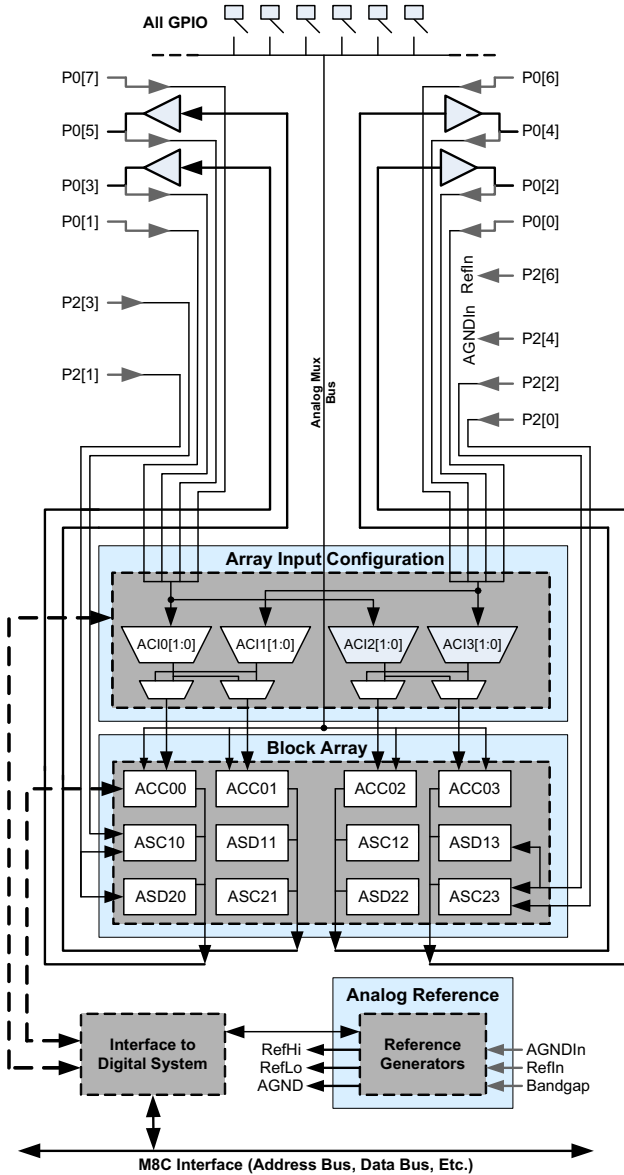


Figure 4. Analog System Block Diagram for CY8C28x33 Devices

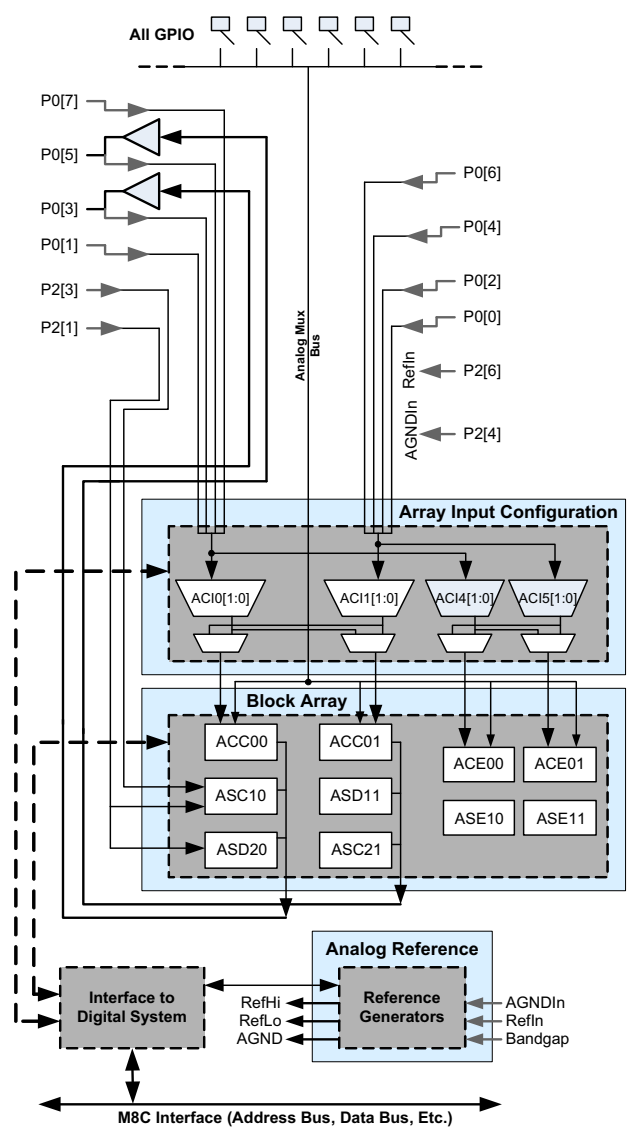


Figure 5. Analog System Block Diagram for CY8C28x23 Devices

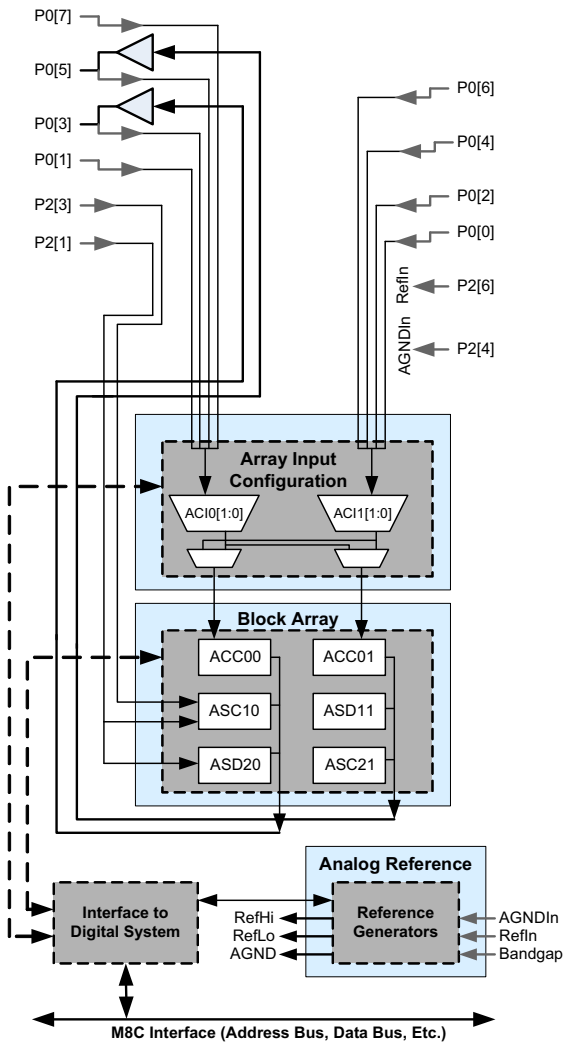
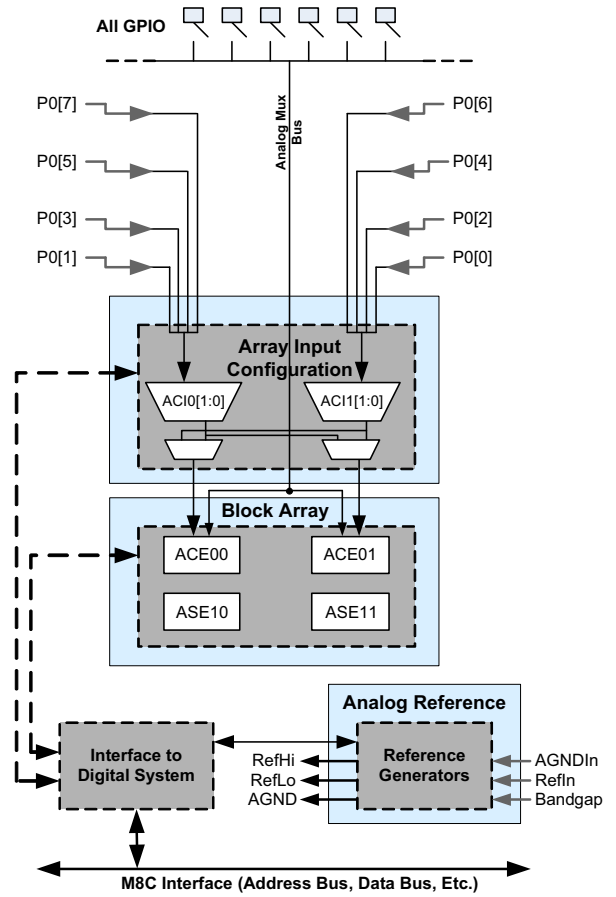


Figure 6. Analog System Block Diagram for CY8C28x13 Devices



System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a multiplier, multiple decimators, switch mode pump, low voltage detection, and power on reset. Statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- Up to four decimators provide custom hardware filters for digital signal processing applications such as Delta-Sigma ADCs and CapSense capacitive sensor measurement.
- Up to two I²C resources provide 0 to 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported. I²C resources have hardware address detection capability.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.5V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

There are other PSoC device groups in addition to the one described in this data sheet. These other PSoC device groups offer even more resource options. The following table lists the resources available for specific PSoC device groups. The PSoC device group covered by this data sheet is highlighted.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	12	4	4	12	2K	32K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12/4 ^[2]	1K	16K
CY8C27x43	up to 44	2	8	12	4	4	12	256 Bytes	16K
CY8C24x94	64	1	4	48	2	2	6	1K	16K
CY8C24x23A	up to 24	1	4	12	2	2	6	256 Bytes	4K
CY8C23x33	up to	1	4	12	2	2	4	256 Bytes	8K
CY8C21x34	up to 28	1	4	28	0	2	4 ^[3]	512 Bytes	8K
CY8C21x23	16	1	4	8	0	2	4 ^[3]	256 Bytes	4K
CY8C20x34	up to 28	0	0	28	0	0	3 ^[4]	512 Bytes	8K

The devices covered by this data sheet all have the same architecture, specifications, and ratings. However, the amount of some hardware resources varies from device to device within the group. The following table lists resources available for the specific device subgroups covered by this data sheet.

Table 2. CY8C28xxx Device Characteristics

PSoC Part Number	CapSense	Digital Blocks	Regular Analog Blocks	Limited Analog Blocks	HW I ² C	Decimators	Digital I/O	Analog Inputs	Analog Outputs
CY8C28x03	N	12	0	0	2	0	up to 24	up to 8	0
CY8C28x13	Y	12	0	4	1	2	up to 40	up to 40	0
CY8C28x23	N	12	6	0	2	2	up to 44	up to 10	2
CY8C28x33	Y	12	6	4	1	4	up to 40	up to 40	2
CY8C28x43	N	12	12	0	2	4	up to 44	up to 44	4
CY8C28x45	Y	12	12	4	2	4	up to 44	up to 44	4
CY8C28x52	Y	8	12	4	1	4	up to 24	up to 24	4

Notes

2. Has 12 regular analog blocks and four limited Type-E analog blocks.
3. Limited analog functionality.
4. Two analog blocks and one CapSense.

Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

PSoC Designer Software Subsystems

System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC On-Chip Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device.

Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I²C-bus, for example), and the logic to control how they interact with one another (called valuator).

In the chip-level view, the components are called “user modules”. User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse

Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in the PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuator to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer’s output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose I/O
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC	Programmable System-on-Chip
PWM	pulse width modulator
SAR	successive approximation register
SC	switched capacitor
SLIMO	slow IMO
SMP	switch mode pump
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. [Table 22](#) on page 32 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.

Pinouts

This section describes, lists, and illustrates the CY8C28xxx PSoC device pins and pinout configurations.

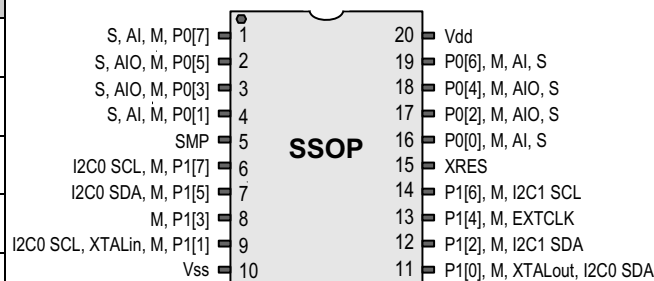
The CY8C28xxx PSoC devices are available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, SMP, and XRES are not capable of Digital I/O.

20-Pin Part Pinout

Table 3. 20-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input. ^[6]
2	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output. ^[6, 7]
3	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output. ^[6, 7]
4	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input. ^[6]
5	Output		SMP	Switch Mode Pump (SMP) connection to external components.
6	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
7	I/O	M	P1[5]	I2C0 Serial Data (SDA).
8	I/O	M	P1[3]	
9	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK ^[5] .
10	Power		Vss	Ground connection.
11	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA ^[5] .
12	I/O	M	P1[2]	I2C1 Serial Data (SDA). ^[8]
13	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
14	I/O	M	P1[6]	I2C1 Serial Clock (SCL). ^[8]
15	Input		XRES	Active high external reset with internal pull down.
16	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input. ^[6]
17	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output. ^[6, 9]
18	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output. ^[6, 9]
19	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input. ^[6]
20	Power		Vdd	Supply voltage.

CY8C28243 20-Pin PSoC Device



LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

Notes

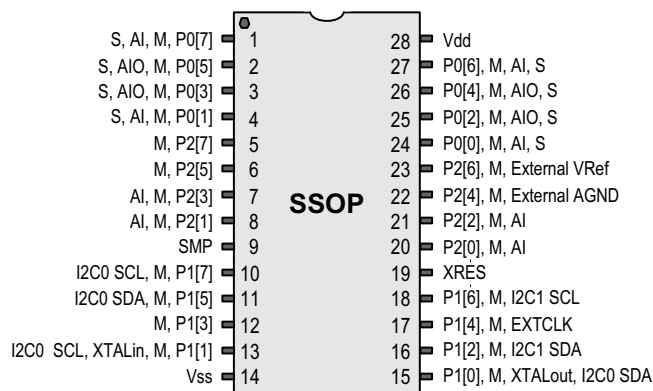
- These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices for details.
- CY8C28x52 and CY8C28x23 devices do not have a SAR ADC. Therefore, this pin does not function as a SAR ADC input for these devices.
- CY8C28x13 and CY8C28x03 devices do not have any analog output buffers. Therefore, this pin does not function as an analog column output for these devices.
- CY8C28x52, CY8C28x13, and CY8C28x33 devices only have one I2C block. Therefore, this GPIO does not function as an I2C pin for these devices.
- CY8C28x33, CY8C28x23, CY8C28x13, and CY8C28x03 devices do not have an analog output buffer for this pin. Therefore, this pin does not function as an analog column output for these devices.

28-Pin Part Pinout

Table 4. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input. ^[6]
2	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output. ^[6, 7]
3	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output. ^[6, 7]
4	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input. ^[6]
5	I/O	M	P2[7]	
6	I/O	M	P2[5]	
7	I/O	I, M	P2[3]	Direct switched capacitor block input. ^[10]
8	I/O	I, M	P2[1]	Direct switched capacitor block input. ^[10]
9	Output		SMP	Switch Mode Pump (SMP) connection to external components.
10	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
11	I/O	M	P1[5]	I2C0 Serial Data (SDA).
12	I/O	M	P1[3]	
13	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK ^[5] .
14	Power		Vss	Ground connection.
15	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA ^[5] .
16	I/O	M	P1[2]	I2C1 Serial Data (SDA). ^[8]
17	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
18	I/O	M	P1[6]	I2C1 Serial Clock (SCL). ^[8]
19	Input		XRES	Active high external reset with internal pull down.
20	I/O	I, M	P2[0]	Direct switched capacitor block input. ^[11]
21	I/O	I, M	P2[2]	Direct switched capacitor block input. ^[11]
22	I/O	M	P2[4]	External Analog Ground (AGND).
23	I/O	M	P2[6]	External Voltage Reference (VRef).
24	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input. ^[6]
25	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output. ^[6, 9]
26	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output. ^[6, 9]
27	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input. ^[6]
28	Power		Vdd	Supply voltage.

CY8C28403, CY8C28413, CY8C28433, CY8C28445, and CY8C28452 28-Pin PSoC Devices



LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input

Notes

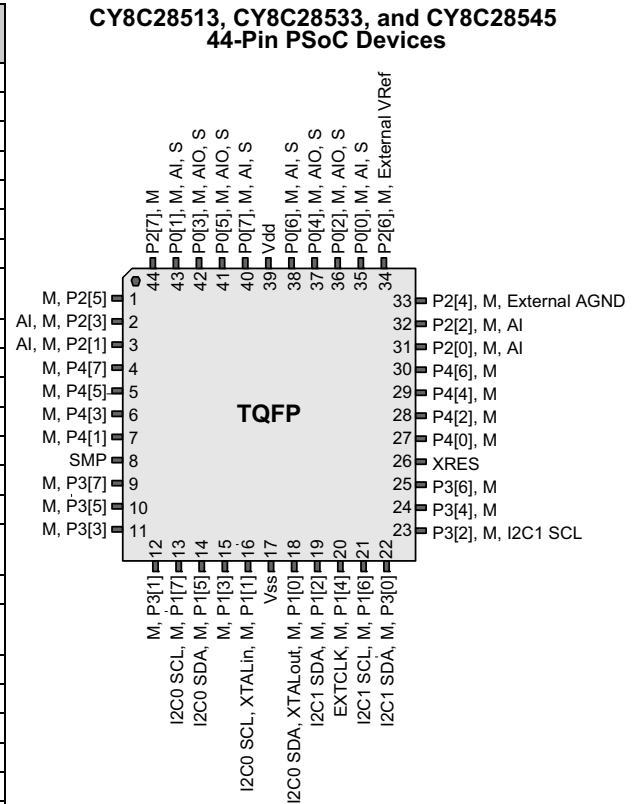
- 10. This pin is not a direct switched capacitor block analog input for CY8C28x03 and CY8C28x13 devices.
- 11. This pin is not a direct switched capacitor block analog input for CY8C28x03, CY8C28x13, CY8C28x23, and CY8C28x33 devices.

44-Pin Part Pinout

Table 5. 44-Pin Part Pinout (TQFP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	M	P2[5]	
2	I/O	I, M	P2[3]	Direct switched capacitor block input. ^[10]
3	I/O	I, M	P2[1]	Direct switched capacitor block input. ^[10]
4	I/O	M	P4[7]	
5	I/O	M	P4[5]	
6	I/O	M	P4[3]	
7	I/O	M	P4[1]	
8	Output		SMP	Switch Mode Pump (SMP) connection to external components.
9	I/O	M	P3[7]	
10	I/O	M	P3[5]	
11	I/O	M	P3[3]	
12	I/O	M	P3[1]	
13	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
14	I/O	M	P1[5]	I2C0 Serial Data (SDA).
15	I/O	M	P1[3]	
16	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK ^[5] .
17	Output		Vss	Ground connection.
18	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA ^[5] .
19	I/O	M	P1[2]	I2C1 Serial Data (SDA). ^[8]
20	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
21	I/O	M	P1[6]	I2C1 Serial Clock (SCL). ^[8]
22	I/O	M	P3[0]	I2C1 Serial Data (SDA). ^[8]
23	I/O	M	P3[2]	I2C1 Serial Clock (SCL). ^[8]
24	I/O	M	P3[4]	
25	I/O	M	P3[6]	
26	Input		XRES	Active high external reset with internal pull down.
27	I/O	M	P4[0]	
28	I/O	M	P4[2]	
29	I/O	M	P4[4]	
30	I/O	M	P4[6]	
31	I/O	I, M	P2[0]	Direct switched capacitor block input. ^[11]
32	I/O	I, M	P2[2]	Direct switched capacitor block input. ^[11]
33	I/O	M	P2[4]	External Analog Ground (AGND).
34	I/O	M	P2[6]	External Voltage Reference (VRef).
35	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input. ^[6]
36	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output. ^[6, 9]
37	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output. ^[6, 9]
38	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input. ^[6]
39	Power		Vdd	Supply voltage.
40	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input. ^[6]
41	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output. ^[6, 7]
42	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output. ^[6, 7]
43	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input. ^[6]
44	I/O	M	P2[7]	

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

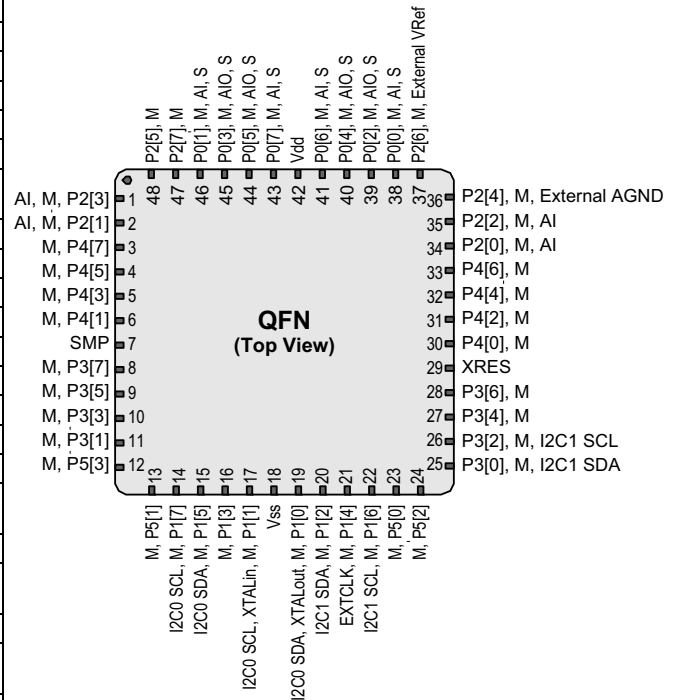


48-Pin Part Pinout

Table 6. 48-Pin Part Pinout (QFN^[12])

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct switched capacitor block input. ^[10]
2	I/O	I, M	P2[1]	Direct switched capacitor block input. ^[10]
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	Output		SMP	Switch Mode Pump (SMP) connection to external components.
8	I/O	M	P3[7]	
9	I/O	M	P3[5]	
10	I/O	M	P3[3]	
11	I/O	M	P3[1]	
12	I/O	M	P5[3]	
13	I/O	M	P5[1]	
14	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
15	I/O	M	P1[5]	I2C0 Serial Data (SDA).
16	I/O	M	P1[3]	
17	I/O	M	P1[1]	Crystal Input (XTALin), I2C0 Serial Clock (SCL), ISSP-SCLK ^[5] .
18	Power		Vss	Ground connection.
19	I/O	M	P1[0]	Crystal Output (XTALout), I2C0 Serial Data (SDA), ISSP-SDATA ^[5] .
20	I/O	M	P1[2]	I2C1 Serial Data (SDA). ^[8]
21	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
22	I/O	M	P1[6]	I2C1 Serial Clock (SCL). ^[8]
23	I/O	M	P5[0]	
24	I/O	M	P5[2]	
25	I/O	M	P3[0]	I2C1 Serial Data (SDA). ^[8]
26	I/O	M	P3[2]	I2C1 Serial Clock (SCL). ^[8]
27	I/O	M	P3[4]	
28	I/O	M	P3[6]	
29	Input		XRES	Active high external reset with internal pull down.
30	I/O	M	P4[0]	
31	I/O	M	P4[2]	
32	I/O	M	P4[4]	
33	I/O	M	P4[6]	
34	I/O	I, M	P2[0]	Direct switched capacitor block input. ^[11]
35	I/O	I, M	P2[2]	Direct switched capacitor block input. ^[11]
36	I/O	M	P2[4]	External Analog Ground (AGND).
37	I/O	M	P2[6]	External Voltage Reference (VRef).
38	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input. ^[6]
39	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output. ^[6, 9]
40	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output. ^[6, 9]

CY8C28623, CY8C28643, and CY8C28645
48-Pin PSoC Devices



Pin No.	Type		Pin Name	Description
	Digital	Analog		
41	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input. ^[6]
42	Power		Vdd	Supply voltage.
43	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input. ^[6]
44	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output. ^[6, 7]
45	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output. ^[6, 7]
46	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input. ^[6]
47	I/O	M	P2[7]	
48	I/O	M	P2[5]	

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, and M = Analog Mux Bus Input.

Note

12. The QFN package has a center pad that must be connected to ground (Vss)

56-Pin Part Pinout

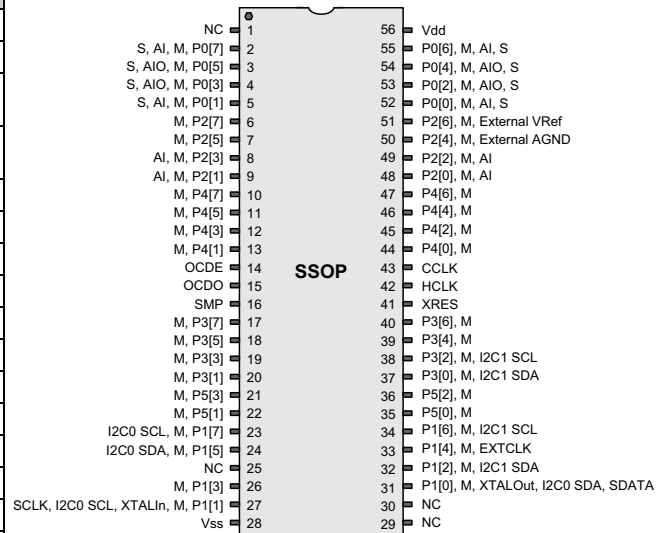
The 56-pin SSOP part is for the CY8C28000 On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 7. 56-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1			NC	No connection.
2	I/O	I, M, S	P0[7]	Analog column mux and SAR ADC input.
3	I/O	I/O, M, S	P0[5]	Analog column mux and SAR ADC input. Analog column output.
4	I/O	I/O, M, S	P0[3]	Analog column mux and SAR ADC input. Analog column output.
5	I/O	I, M, S	P0[1]	Analog column mux and SAR ADC input.
6	I/O	M	P2[7]	
7	I/O	M	P2[5]	
8	I/O	I	P2[3]	Direct switched capacitor block input.
9	I/O	I	P2[1]	Direct switched capacitor block input.
10	I/O	M	P4[7]	
11	I/O	M	P4[5]	
12	I/O	I, M	P4[3]	
13	I/O	I, M	P4[1]	
14	OCD	M	OCDE	OCD even data I/O.
15	OCD	M	OCDO	OCD odd data output.
16	Output		SMP	Switch Mode Pump (SMP) connection to required external components.
17	I/O	M	P3[7]	
18	I/O	M	P3[5]	
19	I/O	M	P3[3]	
20	I/O	M	P3[1]	
21	I/O	M	P5[3]	
22	I/O	M	P5[1]	
23	I/O	M	P1[7]	I2C0 Serial Clock (SCL).
24	I/O	M	P1[5]	I2C0 Serial Data (SDA).
25			NC	No connection.
26	I/O	M	P1[3]	
27	I/O	M	P1[1]	Crystal Input (XTALIn), I2C0 Serial Clock (SCL), ISSP-SCLK ^[5] .
28	Power		Vdd	Ground connection.
29			NC	No connection.
30			NC	No connection.
31	I/O	M	P1[0]	Crystal Output (XTALOut), I2C0 Serial Data (SDA), ISSP-SDATA ^[5] .
32	I/O	M	P1[2]	I2C1 Serial Data (SDA).
33	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
34	I/O	M	P1[6]	I2C1 Serial Clock (SCL).
35	I/O	M	P5[0]	
36	I/O	M	P5[2]	
37	I/O	M	P3[0]	I2C1 Serial Data (SDA).
38	I/O	M	P3[2]	I2C1 Serial Clock (SCL).
39	I/O	M	P3[4]	
40	I/O	M	P3[6]	

CY8C28000 56-Pin PSoC Device



Not for Production

Table 7. 56-Pin Part Pinout (SSOP) (continued)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
41	Input		XRES	Active high external reset with internal pull down.
42	OCD	M	HCLK	OCD high speed clock output.
43	OCD	M	CCLK	OCD CPU clock output.
44	I/O	M	P4[0]	
45	I/O	M	P4[2]	
46	I/O	M	P4[4]	
47	I/O	M	P4[6]	
48	I/O	I, M	P2[0]	Direct switched capacitor block input.
49	I/O	I, M	P2[2]	Direct switched capacitor block input.
50	I/O	M	P2[4]	External Analog Ground (AGND).
51	I/O	M	P2[6]	External Voltage Reference (VRef).
52	I/O	I, M, S	P0[0]	Analog column mux and SAR ADC input.
53	I/O	I/O, M, S	P0[2]	Analog column mux and SAR ADC input. Analog column output.
54	I/O	I/O, M, S	P0[4]	Analog column mux and SAR ADC input. Analog column output.
55	I/O	I, M, S	P0[6]	Analog column mux and SAR ADC input.
56	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, O = Output, S = SAR ADC Input, M = Analog Mux Bus Input, and OCD = On-Chip Debug.

Register Reference

This section lists the registers of the CY8C28xxx PSoC devices. For detailed register information, reference the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices.

Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

CY8C28xxx PSoC devices have a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank of registers CPU instructions access. When the XIO bit is set the registers in Bank 1 are accessed by CPU instructions. When the XIO bit is cleared the registers in Bank 0 are accessed by CPU instructions.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 8. CY8C28x03 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#		80		RD12RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W		81		RD12SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW		82		RD12IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#		83		RD12LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#		84		RD12LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W		85		RD12RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW		86		RD12RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#		87		RD12DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
PRT4GS	12	RW		52			92			D2	
PRT4DM2	13	RW		53			93		IDX_PP	D3	RW
PRT5DR	14	RW		54			94		MVR_PP	D4	RW
PRT5IE	15	RW		55			95		MVW_PP	D5	RW
PRT5GS	16	RW		56			96		I2C0_CFG	D6	RW
PRT5DM2	17	RW		57			97		I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#		60			A0		INT_MSK0	E0	RW
DBC00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBC00DR2	22	RW		62			A2		INT_VC	E2	RC
DBC00CR0	23	#		63			A3		RES_WDT	E3	W
DBC01DR0	24	#		64			A4		I2C1_SCR	E4	#
DBC01DR1	25	W		65			A5		I2C1_MSCR	E5	#
DBC01DR2	26	RW		66			A6			E6	
DBC01CR0	27	#	I2C1_DR	67	RW		A7			E7	
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#		70		RD10RI	B0	RW		F0	
DBC10DR1	31	W		71		RD10SYN	B1	RW		F1	
DBC10DR2	32	RW		72		RD10IS	B2	RW		F2	
DBC10CR0	33	#		73		RD10LT0	B3	RW		F3	
DBC11DR0	34	#		74		RD10LT1	B4	RW		F4	
DBC11DR1	35	W		75		RD10RO0	B5	RW		F5	
DBC11DR2	36	RW		76		RD10RO1	B6	RW		F6	
DBC11CR0	37	#		77		RD10DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RD11RI	B8	RW		F8	
DCC12DR1	39	W		79		RD11SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RD11IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RD11LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RD11LT1	BC	RW		FC	
DCC13DR1	3D	W		7D		RD11RO0	BD	RW		FD	
DCC13DR2	3E	RW		7E		RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 9. CY8C28x03 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW		83		RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW		85		RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW		86		RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW		87		RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW		89			C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW		8A			CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW		8B			CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW		8D			CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW		8E			CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW		8F			CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51			91		GDI_E_IN	D1	RW
PRT4IC0	12	RW		52			92		GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94			D4	
PRT5DM1	15	RW		55			95			D5	
PRT5IC0	16	RW		56			96			D6	
PRT5IC1	17	RW		57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW		60		GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW		61		GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW		62		GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW		63		GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW		64		RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW		E5	
DBC01OU	26	RW		66		RTC_S	A6	RW		E6	
DBC01CR1	27	RW		67		RTC_CR	A7	RW		E7	
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW		69		SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW		6A		SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW	SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW		EC	
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW		ED	
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW		73		RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW		77		RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW		FD	
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 10. CY8C28x13 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#		80		RD12RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W		81		RD12SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW		82		RD12IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#		83		RD12LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#		84		RD12LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W		85		RD12RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW		86		RD12RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#		87		RD12DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50			90		CUR_PP	D0	RW
PRT4IE	11	RW		51			91		STK_PP	D1	RW
PRT4GS	12	RW		52			92			D2	
PRT4DM2	13	RW		53			93		IDX_PP	D3	RW
PRT5DR	14	RW		54			94		MVR_PP	D4	RW
PRT5IE	15	RW		55			95		MVW_PP	D5	RW
PRT5GS	16	RW		56			96		I2C0_CFG	D6	RW
PRT5DM2	17	RW		57			97		I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#		60		DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW		62		DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#		63		DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#		64			A4			E4	
DBC01DR1	25	W		65			A5			E5	
DBC01DR2	26	RW		66			A6		DEC_CR0*	E6	RW
DBC01CR0	27	#		67			A7		DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#		70		RD10RI	B0	RW		F0	
DBC10DR1	31	W		71		RD10SYN	B1	RW		F1	
DBC10DR2	32	RW		72		RD10IS	B2	RW		F2	
DBC10CR0	33	#		73		RD10LT0	B3	RW		F3	
DBC11DR0	34	#		74		RD10LT1	B4	RW		F4	
DBC11DR1	35	W		75		RD10RO0	B5	RW		F5	
DBC11DR2	36	RW		76		RD10RO1	B6	RW		F6	
DBC11CR0	37	#		77		RD10DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RD11RI	B8	RW		F8	
DCC12DR1	39	W		79		RD11SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RD11IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RD11LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RD11LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W		7D		RD11RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW		7E		RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 11. CY8C28x13 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C	RW		CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56			96			D6	
PRT5IC1	17	RW		57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW		60		GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW		61		GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW		62		GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW		63		GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW		64		RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW		66		RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW		67		RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW		69		SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW		6B		SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RDI1RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 12. CY8C28x23 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RD12RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RD12SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RD12IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RD12LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RD12LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RD12RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RD12RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RD12DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#		A4		I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#		A5		I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW		A7		DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RD10RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RD10SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RD10LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RD10LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RD10RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RD10RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RD11RI	B8	RW		F8	
DCC12DR1	39	W		79		RD11SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RD11IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RD11LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RD11LT1	BC	RW		FC	
DCC13DR1	3D	W		7D		RD11RO0	BD	RW		FD	
DCC13DR2	3E	RW		7E		RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 13. CY8C28x23 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW		81		RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW		82		RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW		83		RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW		85		RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW		86		RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW		87		RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW		89			C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW		8A			CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW		8B			CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW		8D			CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW		8E			CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW		8F			CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94	RW	DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56			96			D6	
PRT5IC1	17	RW		57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A		DEC_CR5	9A	RW		DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VL_T_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VL_T_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW		E5	
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW		E6	
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW		E7	
DCC02FN	28	RW		68			A8		IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	RW
DCC02OU	2A	RW		6A			AA		BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW		AB		ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW		ED	
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW		71		RDI0SYN	B1	RW		F1	
DBC10OU	32	RW		72		RDI0IS	B2	RW		F2	
DBC10CR1	33	RW		73		RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW		77		RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW		FD	
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 14. CY8C28x33 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RD12RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RD12SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RD12IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RD12LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RD12LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RD12RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RD12RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RD12DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#		88			C8	
PRT2IE	09	RW	DCC22DR1	49	W		89			C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW		8A			CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#		8B			CB	
PRT3DR	0C	RW	DCC23DR0	4C	#		8C			CC	
PRT3IE	0D	RW	DCC23DR1	4D	W		8D			CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW		8E			CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#		8F			CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58			98		I2C0_DR	D8	RW
	19			59			99		I2C0_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C		INT_CLR2	DC	RW
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F		INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC		E4	
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC		E5	
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#		67		DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RD10RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RD10SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RD10LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RD10LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RD10RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RD10RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#		78		RD11RI	B8	RW		F8	
DCC12DR1	39	W		79		RD11SYN	B9	RW		F9	
DCC12DR2	3A	RW		7A		RD11IS	BA	RW		FA	
DCC12CR0	3B	#		7B		RD11LT0	BB	RW		FB	
DCC13DR0	3C	#		7C		RD11LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W		7D		RD11RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW		7E		RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#		7F		RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 15. CY8C28x33 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88	RW		C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW		65		RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW		68		SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW		6B		SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RDI1RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 16. CY8C28x43 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RD12RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RD12SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RD12IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RD12LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RD12LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RD12RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RD12RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RD12DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#	ASC12CR0	88	RW		C8	
PRT2IE	09	RW	DCC22DR1	49	W	ASC12CR1	89	RW		C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW	ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#	ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW	DCC23DR0	4C	#	ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW	DCC23DR1	4D	W	ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW	ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC	I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC	I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW	DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RD10RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RD10SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RD10LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RD10LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RD10RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RD10RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RD11RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RD11SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RD11IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RD11LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RD11LT1	BC	RW		FC	
DCC13DR1	3D	W	ACB03CR0	7D	RW	RD11RO0	BD	RW		FD	
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 17. CY8C28x43 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80		RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW		83		RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84		RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW		85		RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW		86		RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW		87		RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88			C8	
PRT2DM1	09	RW	DCC22IN	49	RW		89			C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW		8A			CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW		8B			CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C			CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW		8D			CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW		8E			CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW		8F			CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW		E5	
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW		E6	
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW		E7	
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW	SADC_CR3	AB	RW	OSC_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW		73		RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW		75		RDI0RO0	B5	RW		F5	
DBC11OU	36	RW		76		RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW		77		RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW		79		RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW		7A		RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW		7B		RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW		7D		RDI1RO0	BD	RW		FD	
DCC13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW		7F		RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 18. CY8C28x45 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBC20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBC20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBC20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBC20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBC21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBC21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBC21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBC21CR0	47	#	ASD11CR3	87	RW	RDI2DSM	C7	RW
PRT2DR	08	RW	DCC22DR0	48	#	ASC12CR0	88	RW		C8	
PRT2IE	09	RW	DCC22DR1	49	W	ASC12CR1	89	RW		C9	
PRT2GS	0A	RW	DCC22DR2	4A	RW	ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW	DCC22CR0	4B	#	ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW	DCC23DR0	4C	#	ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW	DCC23DR1	4D	W	ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW	DCC23DR2	4E	RW	ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW	DCC23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC	I2C1_SCR	E4	#
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC	I2C1_MSCR	E5	#
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#	I2C1_DR	67	RW	DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW	SADC_DH	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#	SADC_DL	6B	RW	MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 19. CY8C28x45 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBC20FN	40	RW		80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBC20IN	41	RW	SADC_TSCMPL	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBC20OU	42	RW	SADC_TSCMPH	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW	DBC20CR1	43	RW	ACE_AMD_CR1	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBC21FN	44	RW		84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBC21IN	45	RW	ACE_PWM_CR	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBC21OU	46	RW	ACE_ADC0_CR	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW	DBC21CR1	47	RW	ACE_ADC1_CR	87	RW	RDI2DSM	C7	RW
PRT2DM0	08	RW	DCC22FN	48	RW		88	RW		C8	
PRT2DM1	09	RW	DCC22IN	49	RW	ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW	DCC22OU	4A	RW	ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW	DCC22CR1	4B	RW	ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW	DCC23FN	4C	RW		8C	RW		CC	
PRT3DM1	0D	RW	DCC23IN	4D	RW	ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW	DCC23OU	4E	RW	ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW	DCC23CR1	4F	RW	ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW	SADC_CR0	A8	RW	IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW	SADC_CR1	A9	RW	ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW	SADC_CR2	AA	RW	BDG_TR	EA	RW
DCC02CR1	2B	RW	I2C1_CFG	6B	RW	SADC_CR3	AB	RW	ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW	SADC_CR4	AC	RW	MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW	I2C1_ADDR	AE	RW		EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RDI0RI	B0	RW		F0	
DBC10IN	31	RW	SADC_TSCR0	71	RW	RDI0SYN	B1	RW		F1	
DBC10OU	32	RW	SADC_TSCR1	72	RW	RDI0IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RDI0LT0	B3	RW		F3	
DBC11FN	34	RW		74		RDI0LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RDI0RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RDI0RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RDI0DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RDI1SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RDI1LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RDI1RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RDI1DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 20. CY8C28x52 Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48		ASC12CR0	88	RW		C8	
PRT2IE	09	RW		49		ASC12CR1	89	RW		C9	
PRT2GS	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW		51		ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW		54		ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW		55		ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C0_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C0_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C0_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C0_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW	INT_CLR2	DC	RW
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBC00DR0	20	#	AMX_IN	60	RW	DEC0_DH	A0	RC	INT_MSK0	E0	RW
DBC00DR1	21	W	AMUX_CFG	61	RW	DEC0_DL	A1	RC	INT_MSK1	E1	RW
DBC00DR2	22	RW	CLK_CR3	62	RW	DEC1_DH	A2	RC	INT_VC	E2	RC
DBC00CR0	23	#	ARF_CR	63	RW	DEC1_DL	A3	RC	RES_WDT	E3	W
DBC01DR0	24	#	CMP_CR0	64	#	DEC2_DH	A4	RC		E4	
DBC01DR1	25	W	ASY_CR	65	#	DEC2_DL	A5	RC		E5	
DBC01DR2	26	RW	CMP_CR1	66	RW	DEC3_DH	A6	RC	DEC_CR0*	E6	RW
DBC01CR0	27	#		67		DEC3_DL	A7	RC	DEC_CR1*	E7	RW
DCC02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCC02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCC02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCC02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCC03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCC03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCC03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCC03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBC10DR0	30	#	ACB00CR3	70	RW	RD10RI	B0	RW		F0	
DBC10DR1	31	W	ACB00CR0	71	RW	RD10SYN	B1	RW		F1	
DBC10DR2	32	RW	ACB00CR1	72	RW	RD10IS	B2	RW		F2	
DBC10CR0	33	#	ACB00CR2	73	RW	RD10LT0	B3	RW		F3	
DBC11DR0	34	#	ACB01CR3	74	RW	RD10LT1	B4	RW		F4	
DBC11DR1	35	W	ACB01CR0	75	RW	RD10RO0	B5	RW		F5	
DBC11DR2	36	RW	ACB01CR1	76	RW	RD10RO1	B6	RW		F6	
DBC11CR0	37	#	ACB01CR2	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12DR0	38	#	ACB02CR3	78	RW	RD11RI	B8	RW		F8	
DCC12DR1	39	W	ACB02CR0	79	RW	RD11SYN	B9	RW		F9	
DCC12DR2	3A	RW	ACB02CR1	7A	RW	RD11IS	BA	RW		FA	
DCC12CR0	3B	#	ACB02CR2	7B	RW	RD11LT0	BB	RW		FB	
DCC13DR0	3C	#	ACB03CR3	7C	RW	RD11LT1	BC	RW	DAC1_D	FC	RW
DCC13DR1	3D	W	ACB03CR0	7D	RW	RD11RO0	BD	RW	DAC0_D	FD	RW
DCC13DR2	3E	RW	ACB03CR1	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR0	3F	#	ACB03CR2	7F	RW	RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

*Address has a dual purpose, see "Mapping Exceptions" on page 251

Table 21. CY8C28x52 Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43		ACE_AMD_CR1	83	RW		C3	
PRT1DM0	04	RW		44			84			C4	
PRT1DM1	05	RW		45		ACE_PWM_CR	85	RW		C5	
PRT1IC0	06	RW		46		ACE_ADC0_CR	86	RW		C6	
PRT1IC1	07	RW		47		ACE_ADC1_CR	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49		ACE_CLK_CR0	89	RW		C9	
PRT2IC0	0A	RW		4A		ACE_CLK_CR1	8A	RW		CA	
PRT2IC1	0B	RW		4B		ACE_CLK_CR3	8B	RW		CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D		ACE01CR1	8D	RW		CD	
PRT3IC0	0E	RW		4E		ACE01CR2	8E	RW		CE	
PRT3IC1	0F	RW		4F		ASE11CR0	8F	RW		CF	
PRT4DM0	10	RW		50			90		GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		DEC0_CR0	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		DEC_CR3	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53			93		GDI_E_OU	D3	RW
PRT5DM0	14	RW		54			94		DEC0_CR	D4	RW
PRT5DM1	15	RW		55		DEC1_CR0	95	RW	DEC1_CR	D5	RW
PRT5IC0	16	RW		56		DEC_CR4	96	RW	DEC2_CR	D6	RW
PRT5IC1	17	RW		57			97		DEC3_CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59		DEC2_CR0	99	RW	MUX_CR1	D9	RW
	1A			5A		DEC_CR5	9A	RW	MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C		IDAC_CR1	DC	RW
	1D			5D		DEC3_CR0	9D	RW	OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBC00FN	20	RW	CLK_CR0	60	RW	GDI_O_IN_CR	A0	RW	OSC_CR0	E0	RW
DBC00IN	21	RW	CLK_CR1	61	RW	GDI_E_IN_CR	A1	RW	OSC_CR1	E1	RW
DBC00OU	22	RW	ABF_CR0	62	RW	GDI_O_OU_CR	A2	RW	OSC_CR2	E2	RW
DBC00CR1	23	RW	AMD_CR0	63	RW	GDI_E_OU_CR	A3	RW	VLT_CR	E3	RW
DBC01FN	24	RW	CMP_GO_EN	64	RW	RTC_H	A4	RW	VLT_CMP	E4	RW
DBC01IN	25	RW	CMP_GO_EN1	65	RW	RTC_M	A5	RW	ADC0_TR	E5	RW
DBC01OU	26	RW	AMD_CR1	66	RW	RTC_S	A6	RW	ADC1_TR	E6	RW
DBC01CR1	27	RW	ALT_CR0	67	RW	RTC_CR	A7	RW	IDAC_CR2	E7	RW
DCC02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	RW
DCC02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	RW
DCC02OU	2A	RW	AMUX_CFG1	6A	RW		AA		BDG_TR	EA	RW
DCC02CR1	2B	RW		6B			AB		ECO_TR	EB	RW
DCC03FN	2C	RW	TMP_DR0	6C	RW		AC		MUX_CR4	EC	RW
DCC03IN	2D	RW	TMP_DR1	6D	RW	I2C0_ADDR	AD	RW	MUX_CR5	ED	RW
DCC03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCC03CR1	2F	RW	TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBC10FN	30	RW		70		RD10RI	B0	RW		F0	
DBC10IN	31	RW		71		RD10SYN	B1	RW		F1	
DBC10OU	32	RW		72		RD10IS	B2	RW		F2	
DBC10CR1	33	RW	ACE_AMD_CR0	73	RW	RD10LT0	B3	RW		F3	
DBC11FN	34	RW		74		RD10LT1	B4	RW		F4	
DBC11IN	35	RW	ACE_AMX_IN	75	RW	RD10RO0	B5	RW		F5	
DBC11OU	36	RW	ACE_CMP_CR0	76	RW	RD10RO1	B6	RW		F6	
DBC11CR1	37	RW	ACE_CMP_CR1	77	RW	RD10DSM	B7	RW	CPU_F	F7	RL
DCC12FN	38	RW		78		RD11RI	B8	RW		F8	
DCC12IN	39	RW	ACE_CMP_GI_EN	79	RW	RD11SYN	B9	RW		F9	
DCC12OU	3A	RW	ACE_ALT_CR0	7A	RW	RD11IS	BA	RW	FLS_PR1	FA	RW
DCC12CR1	3B	RW	ACE_ABF_CR0	7B	RW	RD11LT0	BB	RW		FB	
DCC13FN	3C	RW		7C		RD11LT1	BC	RW		FC	
DCC13IN	3D	RW	ACE0_CR1	7D	RW	RD11RO0	BD	RW	IDAC_CR0	FD	RW
DCC13OU	3E	RW	ACE0_CR2	7E	RW	RD11RO1	BE	RW	CPU_SCR1	FE	#
DCC13CR1	3F	RW	ACE0_CR3	7F	RW	RD11DSM	BF	RW	CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

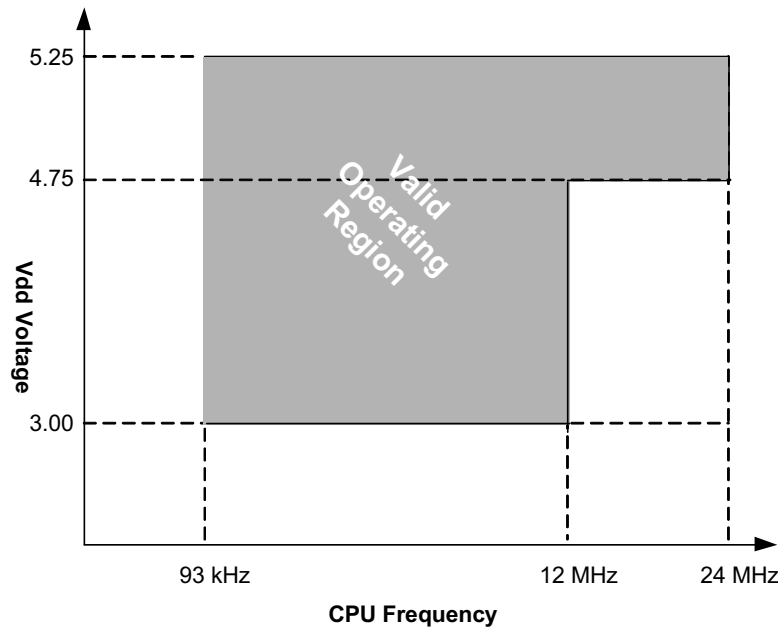
*Address has a dual purpose, see "Mapping Exceptions" on page 251

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C28xxx PSoC devices. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at <http://www.cypress.com/psoc>.

Specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $T_J \leq 100^{\circ}\text{C}$, except where noted. Specifications for devices running at greater than 12 MHz are valid for $-40^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ and $T_J \leq 82^{\circ}\text{C}$.

Figure 7. Voltage versus CPU Frequency



The following table lists the units of measure that are used in this section.

Table 22. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	μW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
μA	microampere	pp	peak-to-peak
μF	microfarad	ppm	parts per million
μH	microhenry	ps	picosecond
μs	microsecond	ksps	kilo-samples per second
μV	microvolts	Σ	sigma: one standard deviation
μVrms	microvolts root-mean-square	V	volts

Absolute Maximum Ratings
Table 23. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T _{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
T _A	Ambient Temperature with Power Applied	-40	–	+85	°C	
V _{dd}	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V _{IO}	DC Input Voltage	V _{ss} - 0.5	–	V _{dd} + 0.5	V	
V _{IOZ}	DC Voltage Applied to Tri-state	V _{ss} - 0.5	–	V _{dd} + 0.5	V	
I _{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I _{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

Operating Temperature
Table 24. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T _A	Ambient Temperature	-40	–	+85	°C	
T _J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 62. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics
DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 25. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{DD}	Supply Voltage	3.00	–	5.25	V	
I _{DD}	Supply Current	–	8	14	mA	Conditions are V _{DD} = 5.0V, T _A = 25°C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I _{DD3}	Supply Current	–	5	9	mA	Conditions are V _{DD} = 3.3V, T _A = 25°C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I _{DDP}	Supply current when IMO = 6 MHz using SLIMO mode=1	–	2	3	mA	Conditions are V _{DD} = 3.3V, T _A = 25°C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz.
I _{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT. ^[13]	–	3	10	μA	Conditions are with internal slow speed oscillator, V _{DD} = 3.3V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$.
I _{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature. ^[13]	–	4	25	μA	Conditions are with internal slow speed oscillator, V _{DD} = 3.3V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$.
I _{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal. ^[13]	–	4	13	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V _{DD} = 3.3V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$.
I _{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature. ^[13]	–	5	26	μA	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V _{DD} = 3.3V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$.
I _{SBRTC}	Current Consumed by RTC during Sleep	–	0.5	1	μA	Extra current consumed by the RTC during sleep. This number is typical at 25°C and 5V.
V _{REF}	Reference Voltage (Bandgap)	1.280	1.300	1.320	V	Trimmed for appropriate V _{DD} .
I _{SXRES}	Supply Current with XRES Asserted 5V	–	0.65	3	mA	Max is peak current after XRES;
	Supply Current with XRES Asserted 3.3V	–	0.4	1.5	mA	Typical value is the steady state current value. T _A =25°C.

Note

13. Standby (sleep) current includes all functions (POR, LVD, WDT, Sleep Timer) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

DC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 26. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R _{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R _{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V _{OH}	High Output Level	V _{DD} - 1.0	–	–	V	I _{OH} = 10 mA, V _{DD} = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I _{OH} budget.
V _{OL}	Low Output Level	–	–	0.75	V	I _{OL} = 25 mA, V _{DD} = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I _{OL} budget.
I _{OH}	High Level Source Current	10	–	–	mA	V _{OH} = V _{DD} -1.0V, see the limitations of the total current in the note for V _{OH} .
I _{OL}	Low Level Sink Current	25	–	–	mA	V _{OL} = 0.75V, see the limitations of the total current in the note for V _{OL} .
V _{IL}	Input Low Level	–	–	0.8	V	V _{DD} = 3.0 to 5.25.
V _{IH}	Input High Level	2.1	–	–	V	V _{DD} = 3.0 to 5.25.
V _H	Input Hysteresis	–	60	–	mV	
I _{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C _{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C _{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 27. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOACT}	Input Offset Voltage CT Block (absolute value) Power = Low, Opamp Bias = High	–	1.6	8	mV	
	Power = Medium, Opamp Bias = High	–	1.3	8	mV	
	Power = High, Opamp Bias = High	–	1.2	8	mV	
V_{OSOA}	Input Offset Voltage SC and AGND Opamps (absolute value)	–	1	6	mV	Applies to High and Low Opamp Bias.
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	$\mu\text{V}/^{\circ}\text{C}$	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to $1 \mu\text{A}$.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C .
V_{CMOA}	Common Mode Voltage Range	0.0	–	Vdd	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
	Common Mode Voltage Range (high power or high opamp bias)	0.5	–	Vdd - 0.5	V	
CMRR_{OA}	Common Mode Rejection Ratio Power = Low	60	–	–	dB	
	Power = Medium	60	–	–	dB	
	Power = High	60	–	–	dB	
G_{OLOA}	Open Loop Gain Power = Low	60	–	–	dB	
	Power = Medium	60	–	–	dB	
	Power = High	80	–	–	dB	
V_{OHIGHOA}	High Output Voltage Swing (internal signals) Power = Low					
	Power = Medium	Vdd - 0.2	–	–	V	
	Power = High	Vdd - 0.2 Vdd - 0.5	– –	– –	V V	
V_{OLOWA}	Low Output Voltage Swing (internal signals) Power = Low					
	Power = Medium	–	–	0.2	V	
	Power = High	–	–	0.2 0.5	V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low	–	200	300	μA	
	Power = Low, Opamp Bias = High	–	400	600	μA	
	Power = Medium, Opamp Bias = Low	–	700	1100	μA	
	Power = Medium, Opamp Bias = High	–	1400	2000	μA	
	Power = High, Opamp Bias = Low	–	2400	3600	μA	
	Power = High, Opamp Bias = High	–	4600	7700	μA	
PSRR_{OA}	Supply Voltage Rejection Ratio	60	–	–	dB	$V_{\text{SS}} \leq V_{\text{IN}} \leq (\text{Vdd} - 2.25)$ or $(\text{Vdd} - 1.25\text{V}) \leq V_{\text{IN}} \leq \text{Vdd}$.

Table 28. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{OSOACT}	Input Offset Voltage CT Blocks (absolute value)	–	1.65	8	mV	
	Power = Low, Opamp Bias = High	–	1.32	8	mV	
	Power = High, Opamp Bias = High	–	–	–	mV	
V _{OSOA}	Input Offset Voltage SC and AGND (absolute value)	–	1	6	mV	Applies to High and Low Opamp Bias.
TCV _{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	μV/°C	
I _{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 μA.
C _{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V _{CMOA}	Common Mode Voltage Range	0.2	–	V _{dd} - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
CMRR _{OA}	Common Mode Rejection Ratio	50	–	–	dB	
	Power = Low	50	–	–	dB	
	Power = High	50	–	–	dB	
G _{OLOA}	Open Loop Gain	60	–	–	dB	
	Power = Low	60	–	–	dB	
	Power = High	80	–	–	dB	
V _{OHIGHOA}	High Output Voltage Swing (internal signals)	V _{dd} - 0.2	–	–	V	
	Power = Low	V _{dd} - 0.2	–	–	V	
	Power = High is 5V only	V _{dd} - 0.2	–	–	V	
V _{OLOWOA}	Low Output Voltage Swing (internal signals)	–	–	0.2	V	
	Power = Low	–	–	0.2	V	
	Power = High	–	–	0.2	V	
I _{SOA}	Supply Current (including associated AGND buffer)	–	200	300	μA	
	Power = Low, Opamp Bias = Low	–	400	600	μA	
	Power = Low, Opamp Bias = High	–	700	1000	μA	
	Power = Medium, Opamp Bias = Low	–	1400	2000	μA	
	Power = Medium, Opamp Bias = High	–	2400	3600	μA	
	Power = High, Opamp Bias = High	–	4600	7500	μA	
PSRR _{OA}	Supply Voltage Rejection Ratio	50	80	–	dB	V _{ss} ≤ V _{IN} ≤ (V _{dd} - 2.25V) or (V _{dd} - 1.25V) ≤ V _{IN} ≤ V _{dd} .

DC Type-E Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of the Limited Type E Analog PSoC blocks.

Table 29. 5V DC Type-E Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)	–	2.5	15	mV	For $0.2\text{V} < V_{\text{in}} < V_{\text{dd}} - 1.2\text{V}$.
		–	2.5	20	mV	For $V_{\text{in}} = 0$ to 0.2V and $V_{\text{in}} > V_{\text{dd}} - 1.2\text{V}$.
TCV_{OSOA}	Average Input Offset Voltage Drift	–	10	–	$\mu\text{V}/^{\circ}\text{C}$	
$I_{\text{EBOA}}^{[14]}$	Input Leakage Current (Port 0 Analog Pins)	–	200	–	nA	Gross tested to $1\ \mu\text{A}$.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C .
V_{CMOA}	Common Mode Voltage Range	0.0	–	Vdd	V	
I_{SOA}	Amplifier Supply Current	–	10	30	μA	

Table 30. 3.3V DC Type-E Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)	–	2.5	15	mV	For $0.2\text{V} < V_{\text{in}} < V_{\text{dd}} - 1.2\text{V}$.
		–	2.5	20	mV	For $V_{\text{in}} = 0$ to 0.2V and $V_{\text{in}} > V_{\text{dd}} - 1.2\text{V}$.
TCV_{OSOA}	Average Input Offset Voltage Drift	–	10	–	$\mu\text{V}/^{\circ}\text{C}$	
$I_{\text{EBOA}}^{[14]}$	Input Leakage Current (Port 0 Analog Pins)	–	200	–	nA	Gross tested to $1\ \mu\text{A}$.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C .
V_{CMOA}	Common Mode Voltage Range	0	–	Vdd	V	
I_{SOA}	Amplifier Supply Current	–	10	30	μA	

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 2.4V to 3.0V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 31. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vdd - 1	V	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	
I_{SLPC}	LPC supply current	–	10	40	μA	

Note

14. Atypical behavior: I_{EBOA} of Port 0 Pin 0 is below 1 nA at 25°C ; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 nA.

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 32. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV _{OSOB}	Average Input Offset Voltage Drift	–	+6	20	μV/°C	
V _{CMOB}	Common-Mode Input Voltage Range	0.5	–	V _{dd} - 1.0	V	
R _{OUTOB}	Output Resistance Power = Low Power = High	– –	1 1	– –	Ω Ω	
V _{OHIGHOB}	High Output Voltage Swing (Load = 32Ω to V _{dd} /2) Power = Low	0.5 x V _{dd} + 1.3	–	–	V	
	Power = High	0.5 x V _{dd} + 1.3	–	–	V	
V _{LOWOB}	Low Output Voltage Swing (Load = 32Ω to V _{dd} /2) Power = Low	–	–	0.5 x V _{dd} - 1.3	V	
	Power = High	–	–	0.5 x V _{dd} - 1.3	V	
I _{SOB}	Supply Current Including Bias Cell (No Load) Power = Low	–	1.1	5.1	mA	
	Power = High	–	2.6	8.8	mA	
PSRR _{OB}	Supply Voltage Rejection Ratio	53	64	–	dB	(0.5 x V _{dd} - 1.0) ≤ V _{OUT} ≤ (0.5 x V _{dd} + 0.9).

Table 33. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	20	$\mu\text{V}/^\circ\text{C}$	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	$V_{DD} - 1.0$	V	
R_{OUTOB}	Output Resistance					
	Power = Low	–	1	–	Ω	
	Power = High	–	1	–	Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1 k Ω to $V_{DD}/2$)					
	Power = Low	$0.5 \times V_{DD} + 1.0$	–	–	V	
	Power = High	$0.5 \times V_{DD} + 1.0$	–	–	V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1 k Ω to $V_{DD}/2$)					
	Power = Low	–	–	$0.5 \times V_{DD} - 1.0$	V	
	Power = High	–	–	$0.5 \times V_{DD} - 1.0$	V	
I_{SOB}	Supply Current Including Bias Cell (No Load)					
	Power = Low	–	0.8	2.0	mA	
	Power = High	–	2.0	4.3	mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	47	64	–	dB	$(0.5 \times V_{DD} - 1.0) \leq V_{OUT} \leq (0.5 \times V_{DD} + 0.9)$.

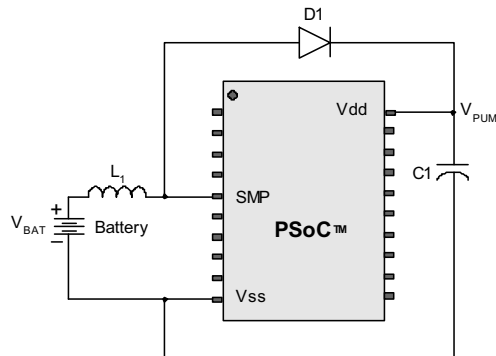
DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 34. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{PUMP} 5V	5V Output Voltage	4.75	5.0	5.25	V	Configuration of footnote. ^[15] Average, neglecting ripple. SMP trip voltage is set to 5.0V.
V _{PUMP} 3V	3V Output Voltage	3.00	3.25	3.60	V	Configuration of footnote. ^[15] Average, neglecting ripple. SMP trip voltage is set to 3.25V.
I _{PUMP}	Available Output Current V _{BAT} = 1.5V, V _{PUMP} = 3.25V V _{BAT} = 1.8V, V _{PUMP} = 5.0V	8 5	– –	– –	mA mA	Configuration of footnote. ^[15] SMP trip voltage is set to 3.25V. SMP trip voltage is set to 5.0V.
V _{BAT} 5V	Input Voltage Range from Battery	1.8	–	5.0	V	Configuration of footnote. ^[15] SMP trip voltage is set to 5.0V.
V _{BAT} 3V	Input Voltage Range from Battery	1.5	–	3.3	V	Configuration of footnote. ^[15] SMP trip voltage is set to 3.25V.
V _{BAT} START	Minimum Input Voltage from Battery to Start Pump	2.6	–	–	V	Configuration of footnote. ^[15]
ΔV _{PUMP_Line}	Line Regulation (over V _{BAT} range)	–	5	–	%V _O	Configuration of footnote. ^[15] V _O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 45 on page 47.
ΔV _{PUMP_Load}	Load Regulation	–	5	–	%V _O	Configuration of footnote. ^[15] V _O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 45 on page 47.
ΔV _{PUMP_Ripple}	Output Voltage Ripple (depends on capacitor/load)	–	100	–	mVpp	Configuration of footnote. ^[15] Load is 5mA.
E ₃	Efficiency	35	50	–	%	Configuration of footnote. ^[15] Load is 5 mA. SMP trip voltage is set to 3.25V.
F _{PUMP}	Switching Frequency	–	1.3	–	MHz	
DC _{PUMP}	Switching Duty Cycle	–	50	–	%	

Figure 8. Basic Switch Mode Pump Circuit



Note

15. L₁ = 2 uH inductor, C₁ = 10 uF capacitor, D₁ = Schottky diode. See Figure 8.

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 35. 5V DC Analog Reference Specifications for High Power

Symbol	Description	Min	Typ	Max	Units
V _{BG5}	Bandgap Voltage Reference 5V	1.28	1.30	1.32	V
–	AGND = Vdd/2 ^[16]	Vdd/2 - 0.021	Vdd/2 - 0.001	Vdd/2 + 0.019	V
–	AGND = 2 x BandGap ^[16]	2.516	2.593	2.67	V
–	AGND = P2[4] (P2[4] = Vdd/2) ^[16]	P2[4] - 0.014	P2[4] - 0.001	P2[4] + 0.012	V
–	AGND = BandGap ^[16]	1.268	1.298	1.328	V
–	AGND = 1.6 x BandGap ^[16]	2.025	2.075	2.125	V
–	AGND Block to Block Variation (AGND = Vdd/2) ^[16]	-29	0	29	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + 1.211	Vdd/2 + 1.282	Vdd/2 + 1.353	V
–	RefHi = 3 x BandGap	3.745	3.879	4.013	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	P2[6] + 2.466	P2[6] + 2.574	P2[6] + 2.734	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + 1.213	P2[4] + 1.281	P2[4] + 1.387	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.070	P2[4] + P2[6] - 0.020	P2[4] + P2[6] + 0.030	V
–	RefHi = 2 x BandGap	2.501	2.587	2.673	V
–	RefHi = 3.2 x BandGap	4.014	4.139	4.264	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 - 1.368	Vdd/2 - 1.303	Vdd/2 - 1.238	V
–	RefLo = BandGap	1.224	1.298	1.372	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2.511 - P2[6]	2.603 - P2[6]	2.689 - P2[6]	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] - 1.358	P2[4] - P2[6] - 0.003	P2[4] - 1.236	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.039	P2[4] - P2[6] - 0.003	P2[4] - P2[6] + 0.045	V

Table 36. 5V DC Analog Reference Specifications for Medium Power

Symbol	Description	Min	Typ	Max	Units
V _{BG5}	Bandgap Voltage Reference 5V	1.28	1.30	1.32	V
–	AGND = Vdd/2 ^[16]	Vdd/2 - 0.021	Vdd/2 - 0.001	Vdd/2 + 0.019	V
–	AGND = 2 x BandGap ^[16]	2.523	2.597	2.671	V
–	AGND = P2[4] (P2[4] = Vdd/2) ^[16]	P2[4] - 0.014	P2[4] - 0.001	P2[4] + 0.012	V
–	AGND = BandGap ^[16]	1.267	1.297	1.327	V
–	AGND = 1.6 x BandGap ^[16]	2.026	2.076	2.126	V
–	AGND Block to Block Variation (AGND = Vdd/2) ^[16]	-29	0	29	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + 1.1221	Vdd/2 + 1.287	Vdd/2 + 1.353	V
–	RefHi = 3 x BandGap	3.76	3.889	4.018	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	P2[6] + 2.484	P2[6] + 2.584	P2[6] + 2.716	V

Note

¹⁶. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 36. 5V DC Analog Reference Specifications for Medium Power (continued)

Symbol	Description	Min	Typ	Max	Units
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + 1.220	P2[4] + 1.286	P2[4] + 1.380	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.061	P2[4] + P2[6] - 0.014	P2[4] + P2[6] + 0.033	V
–	RefHi = 2 x BandGap	2.505	2.59	2.675	V
–	RefHi = 3.2 x BandGap	4.024	4.146	4.268	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 - 1.361	Vdd/2 - 1.298	Vdd/2 - 1.235	V
–	RefLo = BandGap	1.225	1.298	1.371	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2.514 - P2[6]	2.605 - P2[6]	2.686 - P2[6]	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] - 1.362	P2[4] - P2[6] - 0.002	P2[4] - 1.242	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.039	P2[4] - P2[6] - 0.002	P2[4] - P2[6] + 0.035	V

Table 37. 5V DC Analog Reference Specifications for Low Power

Symbol	Description	Min	Typ	Max	Units
V _{BG5}	Bandgap Voltage Reference 5V	1.28	1.3	1.32	V
–	AGND = Vdd/2 ^[16]	Vdd/2 - 0.021	Vdd/2 - 0.001	Vdd/2 + 0.019	V
–	AGND = 2 x BandGap ^[16]	2.523	2.597	2.671	V
–	AGND = P2[4] (P2[4] = Vdd/2) ^[16]	P2[4] - 0.014	P2[4] - 0.001	P2[4] + 0.012	V
–	AGND = BandGap ^[16]	1.267	1.297	1.327	V
–	AGND = 1.6 x BandGap ^[16]	2.026	2.076	2.126	V
–	AGND Block to Block Variation (AGND = Vdd/2) ^[16]	-29	0	29	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + 1.220	Vdd/2 + 1.288	Vdd/2 + 1.356	V
–	RefHi = 3 x BandGap	3.765	3.892	4.019	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	P2[6] + 2.490	P2[6] + 2.587	P2[6] + 2.710	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + 1.222	P2[4] + 1.288	P2[4] + 1.378	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.059	P2[4] + P2[6] - 0.012	P2[4] + P2[6] + 0.035	V
–	RefHi = 2 x BandGap	2.506	2.591	2.676	V
–	RefHi = 3.2 x BandGap	4.026	4.148	4.27	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 - 1.361	Vdd/2 - 1.297	Vdd/2 - 1.233	V
–	RefLo = BandGap	1.223	1.297	1.371	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2.515 - P2[6]	2.605 - P2[6]	2.685 - P2[6]	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] - 1.363	P2[4] - P2[6] - 0.003	P2[4] - 1.243	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.040	P2[4] - P2[6] - 0.004	P2[4] - P2[6] + 0.032	V

Table 38. 3.3V DC Analog Reference Specifications for High Power

Symbol	Description	Min	Typ	Max	Units
V _{BG33}	Bandgap Voltage Reference 3.3V	1.28	1.30	1.32	V
–	AGND = Vdd/2 ^[16]	Vdd/2 - 0.022	Vdd/2 - 0.002	Vdd/2 + 0.018	V
–	AGND = 2 x BandGap ^[16]	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.015	P2[4] - 0.003	P2[4] + 0.009	V
–	AGND = BandGap ^[16]	1.266	1.296	1.326	V
–	AGND = 1.6 x BandGap ^[16]	Not Allowed			
–	AGND Block to Block Variation (AGND = Vdd/2) ^[16]	-27	0	27	mV

Table 38. 3.3V DC Analog Reference Specifications for High Power (continued)

Symbol	Description	Min	Typ	Max	Units
–	RefHi = Vdd/2 + BandGap		Not Allowed		
–	RefHi = 3 x BandGap		Not Allowed		
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)		Not Allowed		
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)		Not Allowed		
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.062	P2[4] + P2[6] - 0.020	P2[4] + P2[6] + 0.022	V
–	RefHi = 2 x BandGap	2.481	2.581	2.681	V
–	RefHi = 3.2 x BandGap		Not Allowed		
–	RefLo = Vdd/2 - BandGap		Not Allowed		
–	RefLo = BandGap		Not Allowed		
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)		Not Allowed		
–	RefLo = P2[4] - BandGap (P2[4] = Vdd/2)		Not Allowed		
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.033	P2[4] - P2[6] + 0.003	P2[4] - P2[6] + 0.039	V

Table 39. 3.3V DC Analog Reference Specifications for Medium Power

Symbol	Description	Min	Typ	Max	Units
V _{BG33}	Bandgap Voltage Reference 3.3V	1.28	1.30	1.32	V
–	AGND = Vdd/2 ^[16]	Vdd/2 - 0.021	Vdd/2 - 0.001	Vdd/2 + 0.019	V
–	AGND = 2 x BandGap ^[16]		Not Allowed		
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.014	P2[4] - 0.003	P2[4] + 0.008	V
–	AGND = BandGap ^[16]	1.266	1.296	1.326	V
–	AGND = 1.6 x BandGap ^[16]		Not Allowed		
–	AGND Block to Block Variation (AGND = Vdd/2) ^[16]	-27	0	27	mV
–	RefHi = Vdd/2 + BandGap		Not Allowed		
–	RefHi = 3 x BandGap		Not Allowed		
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)		Not Allowed		
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)		Not Allowed		
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.049	P2[4] + P2[6] - 0.014	P2[4] + P2[6] + 0.021	V
–	RefHi = 2 x BandGap	2.484	2.584	2.684	V
–	RefHi = 3.2 x BandGap		Not Allowed		
–	RefLo = Vdd/2 - BandGap		Not Allowed		
–	RefLo = BandGap		Not Allowed		
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)		Not Allowed		
–	RefLo = P2[4] - BandGap (P2[4] = Vdd/2)		Not Allowed		
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.034	P2[4] - P2[6] + -0.002	P2[4] - P2[6] + 0.030	V

Table 40. 3.3V DC Analog Reference Specifications for Low Power

Symbol	Description	Min	Typ	Max	Units
V _{BG33}	Bandgap Voltage Reference 3.3V	1.28	1.30	1.32	V
–	AGND = V _{dd} /2 ^[16]	V _{dd} /2 - 0.021	V _{dd} /2 - 0.001	V _{dd} /2 + 0.019	V
–	AGND = 2 x BandGap ^[16]	Not Allowed			
–	AGND = P2[4] (P2[4] = V _{dd} /2)	P2[4] - 0.014	P2[4] - 0.003	P2[4] + 0.008	V
–	AGND = BandGap ^[16]	1.266	1.296	1.326	V
–	AGND = 1.6 x BandGap ^[16]	Not Allowed			
–	AGND Block to Block Variation (AGND = V _{dd} /2) ^[16]	-27	0	27	mV
–	RefHi = V _{dd} /2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = V _{dd} /2)	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = V _{dd} /2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.048	P2[4] + P2[6] - 0.013	P2[4] + P2[6] + 0.022	V
–	RefHi = 2 x BandGap	2.485	2.585	2.685	V
–	RefHi = 3.2 x BandGap	Not Allowed			
–	RefLo = V _{dd} /2 - BandGap	Not Allowed			
–	RefLo = BandGap	Not Allowed			
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefLo = P2[4] - BandGap (P2[4] = V _{dd} /2)	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = V _{dd} /2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.034	P2[4] - P2[6] + -0.003	P2[4] - P2[6] + 0.028	V

Note See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 41. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R _{CT}	Resistor Unit Value (Continuous Time)	–	12.24	–	kΩ	
C _{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 42. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R _{SW}	Switch Resistance to Common Analog Bus	–	–	400	Ω	V _{dd} ≥ 3.0V
R _{VSS}	Resistance of Initialization Switch to VSS	–	–	800	Ω	

DC SAR10 ADC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 43. DC SAR10 ADC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
INL _{SAR10}	Integral nonlinearity for VREF ≥ 3V	-2.5	-	2.5	LSB	10-bit resolution
	Integral nonlinearity for VREF < 3V	-5	-	5	LSB	10-bit resolution
DNL _{SAR10}	Differential nonlinearity for VREF ≥ 3V	-1.5	-	1.5	LSB	10-bit resolution
	Differential nonlinearity for VREF > 3V	-4	-	4	LSB	10-bit resolution
I _{SAR10}	Active current consumption	0.08	0.5	0.497	mA	
I _{VREFSAR10}	Input current into P2[5] when configured as the SAR10 ADC's VREF input.	-	-	0.5	mA	The internal voltage reference buffer is disabled in this configuration.
V _{VREFSAR10}	Input reference voltage at P2[5] when configured as the SAR10 ADC's external voltage reference.	3.0	-	4.95	V	When VREF is buffered inside the SAR10 ADC, the voltage level at P2[5] (when configured as the external reference voltage) must always be at least 300 mV less than the chip supply voltage level on the Vdd pin. (V _{VREFSAR10} < (Vdd - 300 mV)).
V _{OSSAR10}	Offset voltage	5	7.7	10	mV	
SAR _{IMP}	SAR input impedance	-	1.64	-	MΩ	Frequency dependant = 1/ Fs°C. 142.9 kHz (maximum) and Cin = 4.28 pF (typical)

Table 44. DC IDAC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	-5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_INL	Integral nonlinearity	-5.0	2.0	5.0	LSB	Valid for all 3 current ranges
IDAC_Gain	Gain per bit - Range 1 (91 μA)	283	357	447	nA	Measured at full scale
	Gain per bit - Range 2 (318 μA)	985	1250	1532	nA	
	Gain per bit - Range 3 (637 μA)	1959	2500	3056	nA	
IDACOffset	Offset at Code 0 vs LSB Ideal - Range 1 (91 μA)		2.0%	20%	%	Measured as a % of LSB (Current @ Code 0)/(LSB Ideal Current)
	Offset at Code 0 vs LSB Ideal - Range 2 (318 μA)		1.0%	10%	%	
	Offset at Code 0 vs LSB Ideal - Range 3 (637 μA)		1.0%	10%	%	

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register. See the *PSoC Technical Reference Manual* for CY8C28xxx PSoC devices, for more information on the VLT_CR register.

Table 45. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V _{PPOR0R} V _{PPOR1R} V _{PPOR2R}	Vdd Value for PPOR Trip (positive ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	– – –	2.91 4.39 4.55	2.985 4.49 4.65	V V V	Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V _{PPOR0} V _{PPOR1} V _{PPOR2}	Vdd Value for PPOR Trip (negative ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	– – –	2.82 4.39 4.55	2.90 4.49 4.64	V V V	Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V _{PH0} V _{PH1} V _{PH2}	PPOR Hysteresis PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	– – –	92 0 0	– – –	mV mV mV	
V _{LVD0} V _{LVD1} V _{LVD2} V _{LVD3} V _{LVD4} V _{LVD5} V _{LVD6} V _{LVD7}	Vdd Value for LVD Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.83 2.93 3.04 3.90 4.38 4.54 4.62 4.71	2.91 3.01 3.12 3.99 4.47 4.63 4.71 4.80	3.00 ^[17] 3.10 3.21 4.09 4.58 4.74 ^[18] 4.83 4.92	V V V V V V V V	
V _{PUMP0} V _{PUMP1} V _{PUMP2} V _{PUMP3} V _{PUMP4} V _{PUMP5} V _{PUMP6} V _{PUMP7}	Vdd Value for PUMP Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.93 3.00 3.16 4.09 4.53 4.61 4.70 4.88	3.01 3.08 3.24 4.17 4.62 4.71 4.80 4.98	3.10 3.17 3.33 4.28 4.74 4.82 4.91 5.10	V V V V V V V V	

Notes

17. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
18. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 46. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying V_{ilp} to P1[0] or P1[1] During Programming or Verify	–	–	0.21	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying V_{ihp} to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	$V_{dd} - 1.0$	–	V_{dd}	V	
Flash _{ENPB}	Flash Endurance (per block)	50,000 ^[19]	–	–	–	Erase/write cycles per block.
Flash _{ENT}	Flash Endurance (total) ^[20]	1,800,000	–	–	–	Erase/write cycles. Must be programmed and read at the same voltage to meet this.
Flash _{DR}	Flash Data Retention	10	–	–	Years	

Note

19. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 3.0V to 3.6V and 4.75V to 5.25V.

20. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 47. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6 ^[21]	MHz	Trimmed. Utilizing factory trim values. SLIMO Mode = 0.
F _{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5 ^[21]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. SLIMO Mode = 1.
F _{CPU1}	CPU Frequency (5V Nominal)	0.091	24	24.6 ^[21, 22]	MHz	Trimmed. Utilizing factory trim values.
F _{CPU2}	CPU Frequency (3.3V Nominal)	0.091	12	12.3 ^[22, 23]	MHz	Trimmed. Utilizing factory trim values.
F _{BLK5}	Digital PSoC Block Frequency	0	-	49.2 ^[21, 22, 24]	MHz	4.75V < V _{dd} < 5.25V
F _{BLK33}	Digital PSoC Block Frequency	0	24	24.6 ^[22, 24]	MHz	3.0V < V _{dd} < 3.6V
F _{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	Trimmed. Utilizing factory trim values.
F _{32K2}	External Crystal Oscillator	-	32.768	-	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F _{32K_U}	Internal Low Speed Oscillator Untrimmed Frequency	5	-	-	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference manual for details on timing this.
F _{PLL}	PLL Frequency	-	23.986	-	MHz	Multiple (x732) of crystal frequency.
Jitter24M2	24 MHz RMS Period Jitter (PLL)	-	-	600	ps	
T _{PLLSLEW}	PLL Lock Time	0.5	-	10	ms	
T _{PLLSLEWSLOW}	PLL Lock Time for Low Gain Setting	0.5	-	50	ms	
T _{OS}	External Crystal Oscillator Startup to 1%	-	1700	2620	ms	
T _{OSACC}	External Crystal Oscillator Startup to 100 ppm	-	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T _{OSACC} period. Correct operation assumes a properly loaded 1 μW maximum drive level 32.768 kHz crystal. 3.0V ≤ V _{dd} ≤ 5.5V, -40°C ≤ T _A ≤ 85°C.
Jitter32k	32 kHz RMS Period Jitter	-	100	-	ns	
T _{XRST}	External Reset Pulse Width	10	-	-	μs	
DC _{24M}	24 MHz Duty Cycle	40	50	60	%	
DC _{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
F _{out48M}	48 MHz Output Frequency	46.8	48.0	49.2 ^[21, 23]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz RMS Period Jitter (IMO)	-	600	-	ps	
F _{MAX}	Maximum Frequency of Signal on Row Input or Row Output.	-	-	12.3	MHz	
SR _{POWERUP}	Supply Ramp Time	0	-	-	μs	
T _{POWERUP}	Time for POR Release to Code Execution	-	16	100	ms	

Notes

21. 4.75V < V_{dd} < 5.25V.

22. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{dd} range.

23. 3.0V < V_{dd} < 3.6V. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.

24. See the individual user module data sheets for information on maximum frequencies for user modules.

Figure 9. PLL Lock Timing Diagram

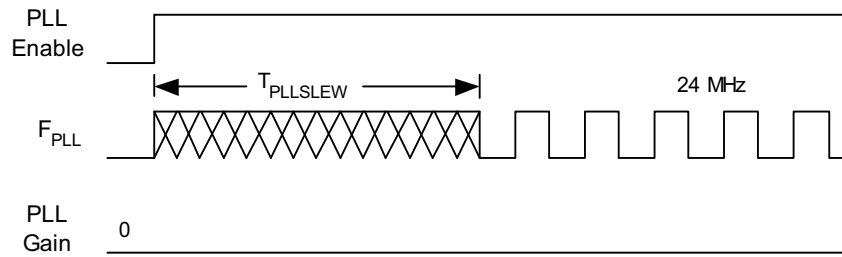


Figure 10. PLL Lock for Low Gain Setting Timing Diagram

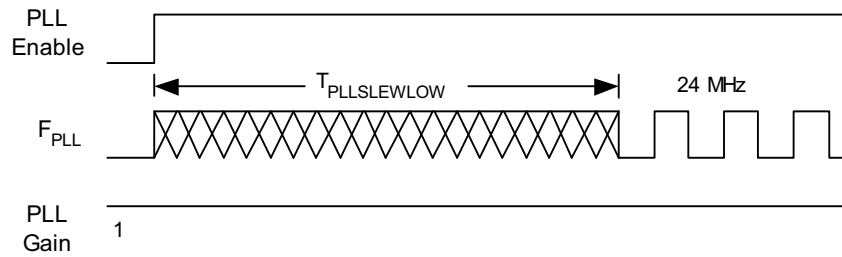


Figure 11. External Crystal Oscillator Startup Timing Diagram

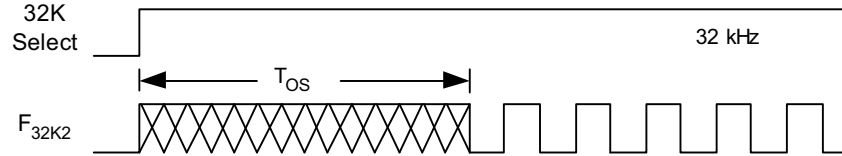


Figure 12. 24 MHz Period Jitter (IMO) Timing Diagram

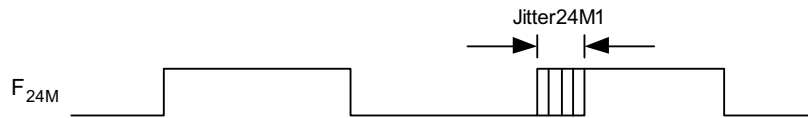


Figure 13. 32 kHz Period Jitter (ECO) Timing Diagram



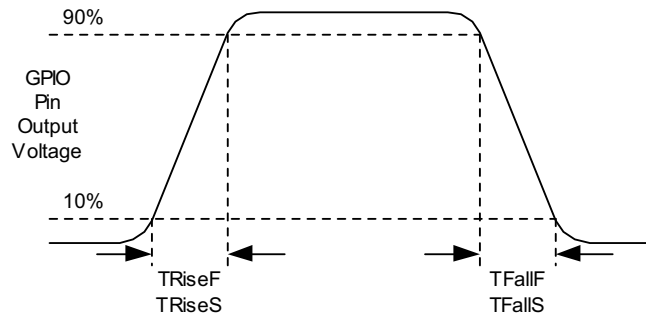
AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 48. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{GPIO}	GPIO Operating Frequency	0	–	12.3	MHz	Normal Strong Mode
T _{RiseF}	Rise Time, Normal Strong Mode, Load = 50 pF	3	–	18	ns	V _{dd} = 4.5 to 5.25V, 10% - 90%
T _{FallF}	Fall Time, Normal Strong Mode, Load = 50 pF	2	–	18	ns	V _{dd} = 4.5 to 5.25V, 10% - 90%
T _{RiseS}	Rise Time, Slow Strong Mode, Load = 50 pF	10	27	–	ns	V _{dd} = 3 to 5.25V, 10% - 90%
T _{FallS}	Fall Time, Slow Strong Mode, Load = 50 pF	10	22	–	ns	V _{dd} = 3 to 5.25V, 10% - 90%

Figure 14. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 49. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T _{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain)	–	–	3.9	μs	
	Power = Low, Opamp Bias = Low	–	–	0.72	μs	
	Power = High, Opamp Bias = High	–	–	0.62	μs	
T _{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain)	–	–	5.9	μs	
	Power = Low, Opamp Bias = Low	–	–	0.92	μs	
	Power = High, Opamp Bias = High	–	–	0.72	μs	
SR _{ROA}	Rising Slew Rate (20% to 80%)(Active Probe Loading, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.15	–	–	V/μs	
	Power = High, Opamp Bias = High	1.7	–	–	V/μs	

Table 49. 5V AC Operational Amplifier Specifications (continued)

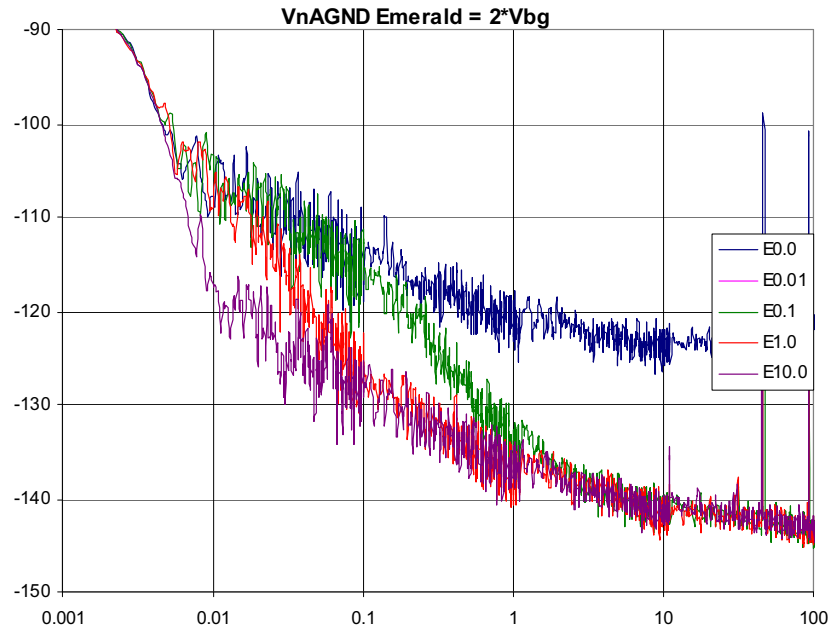
Symbol	Description	Min	Typ	Max	Units	Notes
SR _{FOA}	Falling Slew Rate (80% to 20%)(Active Probe Loading, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.01	–	–	V/μs	
	Power = Medium, Opamp Bias = High	0.5	–	–	V/μs	
BW _{OA}	Gain Bandwidth Product					
	Power = Low, Opamp Bias = Low	0.75	–	–	MHz	
	Power = Medium, Opamp Bias = High	3.1	–	–	MHz	
E _{NOA}	Noise at 1 kHz	–	100	–	nV/rt-Hz	
	Power = Medium, Opamp Bias = High					

Table 50. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T _{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain)					
	Power = Low, Opamp Bias = Low	–	–	3.92	μs	
	Power = Low, Opamp Bias = High	–	–	0.72	μs	
T _{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (Active Probe Loading, Unity Gain)					
	Power = Low, Opamp Bias = Low	–	–	5.41	μs	
	Power = Medium, Opamp Bias = High	–	–	0.72	μs	
SR _{ROA}	Rising Slew Rate (20% to 80%)(Active Probe Loading, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.31	–	–	V/μs	
SR _{FOA}	Falling Slew Rate (80% to 20%)(Active Probe Loading, Unity Gain)					
	Power = Medium, Opamp Bias = High	2.7	–	–	V/μs	
BW _{OA}	Gain Bandwidth Product					
	Power = Low, Opamp Bias = Low	0.24	–	–	V/μs	
E _{NOA}	Noise at 1 kHz	–	100	–	nV/rt-Hz	
	Power = Medium, Opamp Bias = High	1.8	–	–	V/μs	

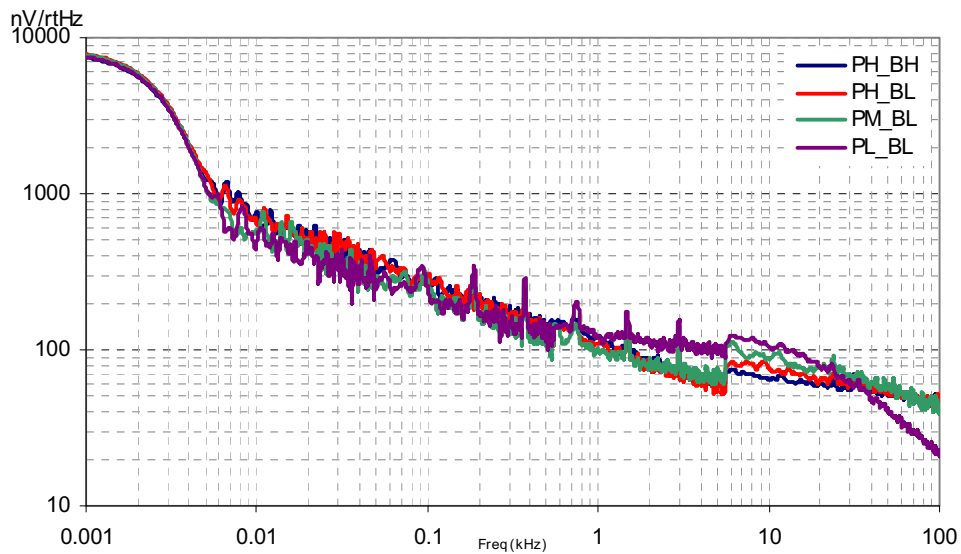
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 15. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to $1/f$, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 16. Typical Opamp Noise



AC Type-E Operational Amplifier Specifications

Table 51 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 2.4V to 3.0V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only. The Operational Amplifiers covered by these specifications are components of the Limited Type E Analog PSoC blocks.

Table 51. AC Type-E Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T _{COMP}	Comparator Mode Response Time	–	75	100	ns	50 mV overdrive.

AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 2.4V to 3.0V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 52. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T _{RLPC}	LPC Response Time	–	–	50	μs	≥ 50 mV overdrive.

AC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 53. AC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{SW}	Switch Rate	–	–	3.17	MHz	

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 54. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency (> 4.75V)	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Block Clocking Frequency (< 4.75V)	–	–	24.6	MHz	3.0V < Vdd < 4.75V.
Timer	Capture Pulse Width	50 ^[25]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50 ^[25]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50 ^[25]	–	–	ns	
	Disable Mode	50 ^[25]	–	–	ns	
CRCPRS (PRS Mode)	Maximum Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50 ^[25]	–	–	ns	
Transmitter	Full Vdd Range	–	–	24.6	MHz	Maximum data rate at 3.16 MHz due to 8 x over clocking.
	Vdd ≥ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.30 MHz due to 8 x over clocking.
Receiver	Full Vdd Range	–	–	24.6	MHz	Maximum data rate at 3.16 MHz due to 8 x over clocking.
	Vdd ≥ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.30 MHz due to 8 x over clocking.

Note

25. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 55. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T _{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	–	–	2.5	μs	
		–	–	2.9	μs	
T _{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	–	–	2.3	μs	
		–	–	2.3	μs	
SR _{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	0.65	–	–	V/μs	
		0.65	–	–	V/μs	
SR _{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	0.65	–	–	V/μs	
		0.65	–	–	V/μs	
BW _{OB}	Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100 pF Load Power = Low Power = High	0.8	–	–	MHz	
		0.8	–	–	MHz	
BW _{OB}	Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100 pF Load Power = Low Power = High	300	–	–	kHz	
		300	–	–	kHz	

Table 56. 3.3V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T _{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	–	–	3.8	μs	
		–	–	3.8	μs	
T _{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	–	–	3.2	μs	
		–	–	2.9	μs	
SR _{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	0.5	–	–	V/μs	
		0.5	–	–	V/μs	
SR _{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	0.5	–	–	V/μs	
		0.5	–	–	V/μs	
BW _{OB}	Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100 pF Load Power = Low Power = High	0.64	–	–	MHz	
		0.64	–	–	MHz	
BW _{OB}	Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100 pF Load Power = Low Power = High	200	–	–	kHz	
		200	–	–	kHz	

AC SAR10 ADC Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 57. AC SAR10 ADC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{INSAR10}	Input clock frequency for SAR10 ADC	–	–	2.0	MHz	
F _{SSAR10}	Sample rate for SAR10 ADC SAR10 ADC Resolution = 10 bits	–	–	142.9	ksps	For 10-bit resolution, the sample rate is the ADC's input clock divided by 14.

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 58. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	μs	

Table 59. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{OSCEXT}	Frequency with CPU Clock divide by 1 ^[26]	0.093	–	12.3	MHz	
F _{OSCEXT}	Frequency with CPU Clock divide by 2 or greater ^[27]	0.186	–	24.6	MHz	
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	μs	

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 60. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T _{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T _{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T _{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	–	–	ns	
T _{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F _{SCLK}	Frequency of SCLK	0	–	8	MHz	
T _{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T _{WRITE}	Flash Block Write Time	–	40	–	ms	
T _{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	55	ns	V _{dd} > 3.6

Table 60. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T _{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	75	ns	3.0 ≤ V _{dd} ≤ 3.6
T _{ERASEALL}	Flash Erase Time (Bulk)	–	40	–	ms	Erase all blocks and protection fields at once.
T _{PROGRAM_HOT}	Flash Block Erase + Flash Block Write Time	–	–	100 ^[28]	ms	0°C ≤ T _j ≤ 100°C
T _{PROGRAM_COLD}	Flash Block Erase + Flash Block Write Time	–	–	200 ^[28]	ms	-40°C ≤ T _j ≤ 0°C

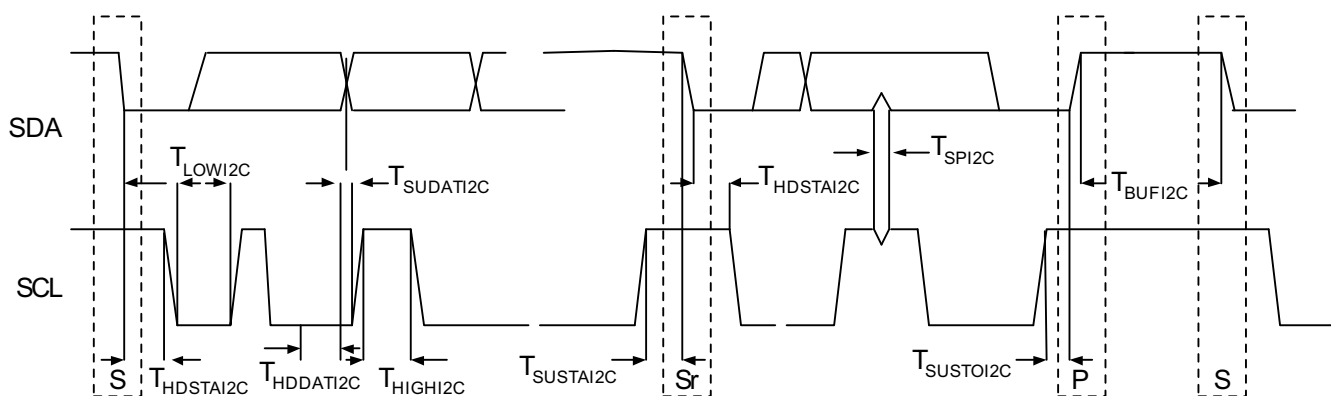
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 61. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F _{SCL I2C}	SCL Clock Frequency	0	100	0	400	kHz	
T _{HDSTAI2C}	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	μs	
T _{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	μs	
T _{HIGHI2C}	HIGH Period of the SCL Clock	4.0	–	0.6	–	μs	
T _{SUSTAI2C}	Setup Time for a Repeated START Condition	4.7	–	0.6	–	μs	
T _{HDDATI2C}	Data Hold Time	0	–	0	–	μs	
T _{SUDATI2C}	Data Setup Time	250	–	100 ^[29]	–	ns	
T _{SUSTOI2C}	Setup Time for STOP Condition	4.0	–	0.6	–	μs	
T _{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	μs	
T _{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Figure 17. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

- 26. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
- 27. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
- 28. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note, AN2015 at <http://www.cypress.com> under Application Notes for more information.
- 29. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement T_{SUDATI2C} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + T_{SUDATI2C} = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Packaging Information

This section illustrates the packaging specifications for the CY8C28xxx PSoC devices, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the drawings at <http://www.cypress.com/design/MR10161>.

Packaging Dimensions

Figure 18. 20-Pin (210-Mil) SSOP

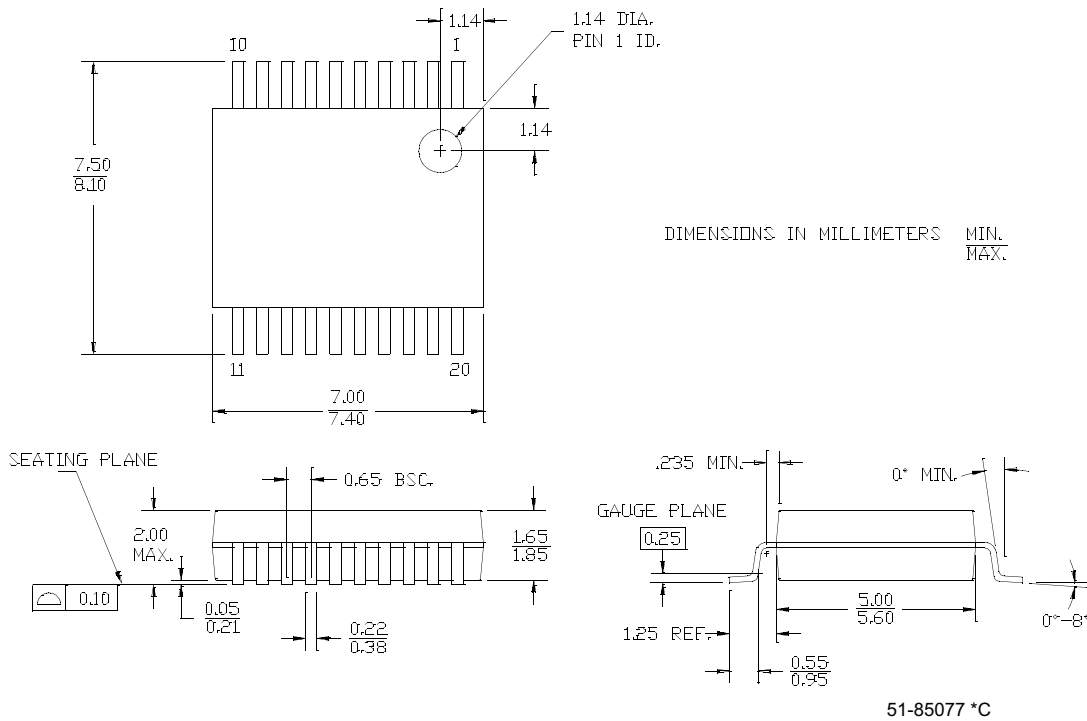
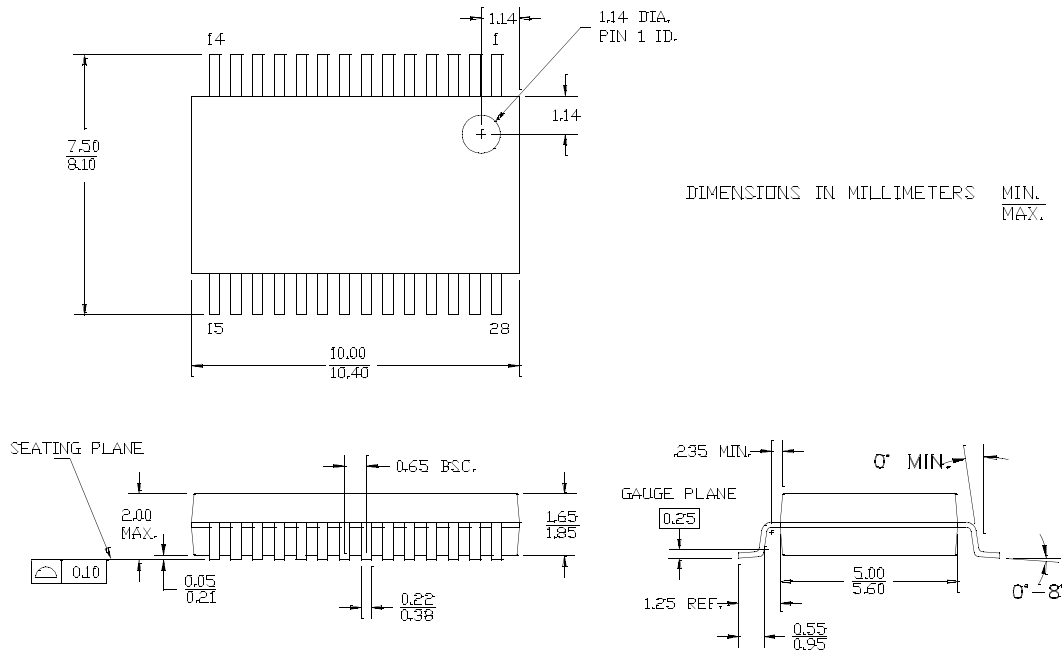
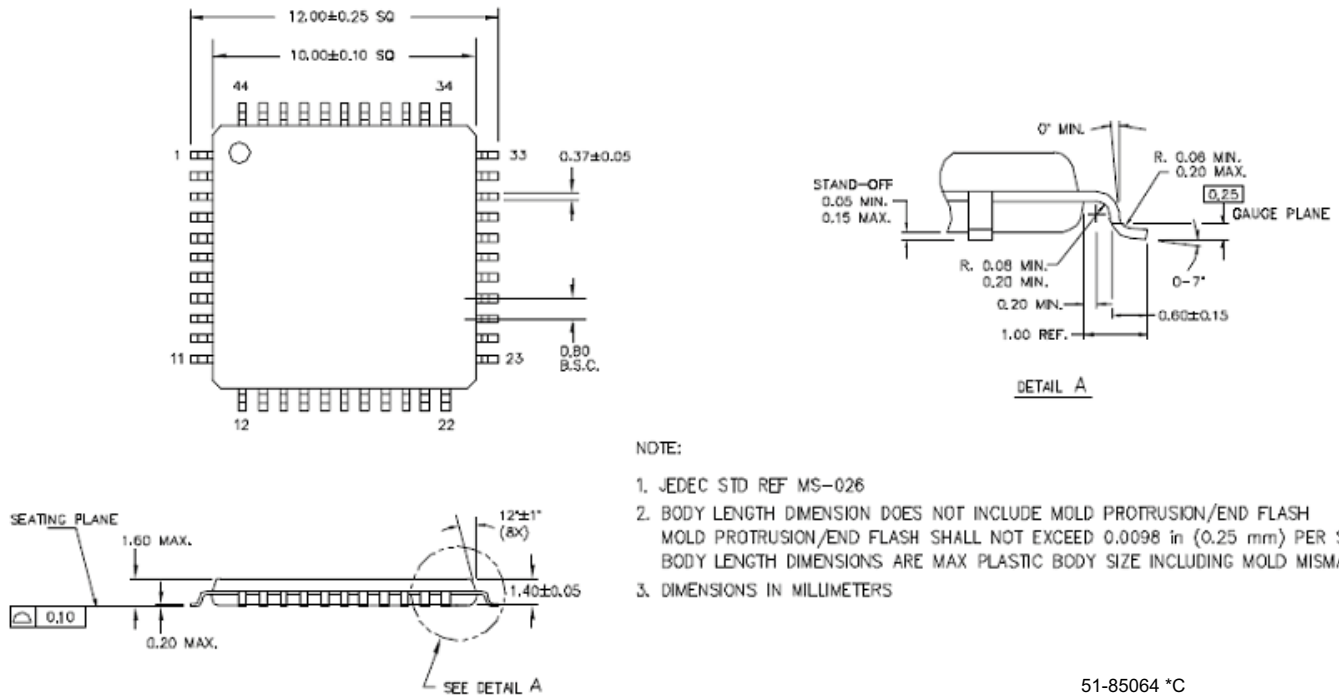


Figure 19. 28-Pin (210-Mil) SSOP



51-85079 °C

Figure 20. 44-Pin TQFP

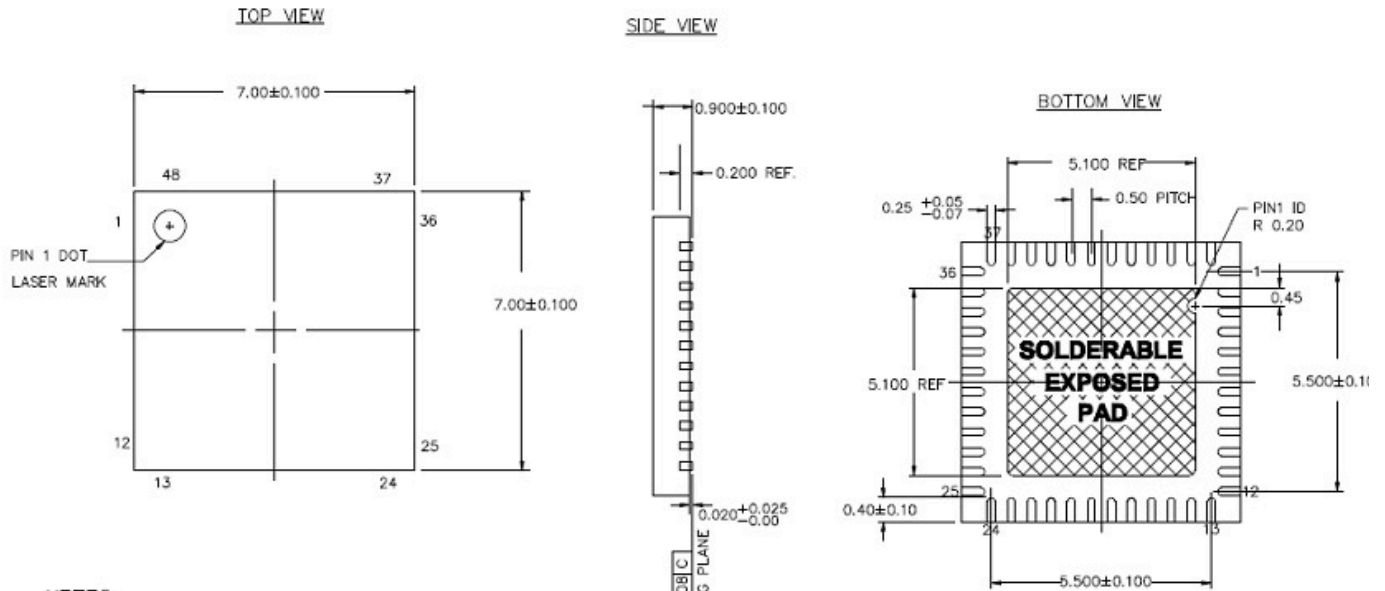


51-85064 °C

NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

Figure 21. 48-Pin (7x7 mm) QFN



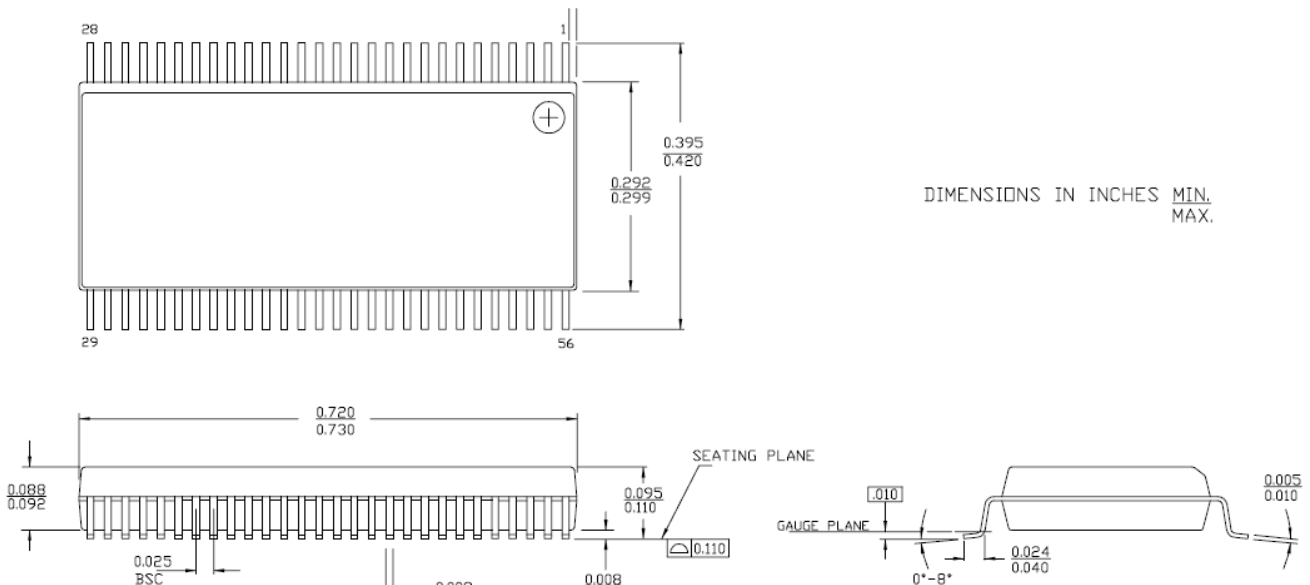
NOTES:

1. [Hatched Area] HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *D

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Figure 22. 56-Pin SSOP Package



DIMENSIONS IN INCHES MIN. MAX.

51-85062 *C

Thermal Impedances

Table 62. Thermal Impedances per Package

Package	Typical θ_{JA} [30]
20 SSOP	80.8 °C/W
28 SSOP	45.4 °C/W
44 TQFP	24.0 °C/W
48 QFN	16.7 °C/W
56 SSOP	67.5 °C/W

Capacitance on Crystal Pins

Table 63. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
20 SSOP	Pin9 = 0.0056 pF Pin11 = 0.006048 pF
28 SSOP	Pin13 = 0.006796 pF Pin15 = 0.006755 pF
44 TQFP	Pin16 = 0.009428 pF Pin18 = 0.008635 pF
48 QFN	Pin17 = 0.008493 pF Pin19 = 0.008742 pF
56 SSOP	Pin27 = 0.007916 pF Pin31 = 0.007132 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 64. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature [31]	Maximum Peak Temperature
20 SSOP	245°C	260°C
28 SSOP	245°C	260°C
44 TQFP	245°C	260°C
48 QFN	245°C	260°C
56 SSOP	245°C	260°C

Notes

30. $T_J = T_A + \text{POWER} \times \theta_{JA}$

31. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CY8C28xxx family.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at <http://www.cypress.com/psocdesigner>.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at <http://www.cypress.com/psocprogrammer>.

PSoC C Compilers

CY3202 is the optional upgrade to PSoC Designer that enables the iMAGEcraft C compiler. It can be purchased from the Cypress Online Store. At <http://www.cypress.com>, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Development Kits

All development kits can be purchased from the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the content of specific memory locations. Advanced emulation features are supported in PSoC Designer. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- Pod kit for CY8C29x66 PSoC Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note The CY3207ISSP programmer needs the PSoC ISSP software. It is not compatible with the PSoC Programmer

software. The latest PSoC ISSP software for this kit can be downloaded from <http://www.cypress.com>. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 65. Emulation and Programming Accessories

Part #	Pin Package	Pod Kit ^[32]	Foot Kit ^[33]	Adapter ^[34]
CY8C28243-24PVXI	20 SSOP	CY3250-28XXX	CY3250-20SSOP-FK	Adapters can be found at http://www.emulation.com .
CY8C28403-24PVXI	28 SSOP	CY3250-28XXX	CY3250-28SSOP-FK	
CY8C28413-24PVXI				
CY8C28433-24PVXI				
CY8C28445-24PVXI				
CY8C28452-24PVXI				
CY8C28513-24AXI	44 TQFP	CY3250-28XXX	CY3250-44TQFP-FK	
CY8C28533-24AXI				
CY8C28545-24AXI				
CY8C28623-24LTXI	48 QFN	CY3250-28XXXQFN	CY3250-48QFN-FK	
CY8C28643-24LTXI				
CY8C28645-24LTXI				

3rd-Party Tools

Several tools have been specially designed by the following 3rd-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at <http://www.cypress.com> under DESIGN RESOURCES >> Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note "Debugging - Build a PSoC Emulator into Your Board - AN2323" at <http://www.cypress.com/an2323>.

Notes

32. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.

33. Foot kit includes surface mount feet that can be soldered to the target PCB.

34. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at <http://www.emulation.com>.

Ordering Information

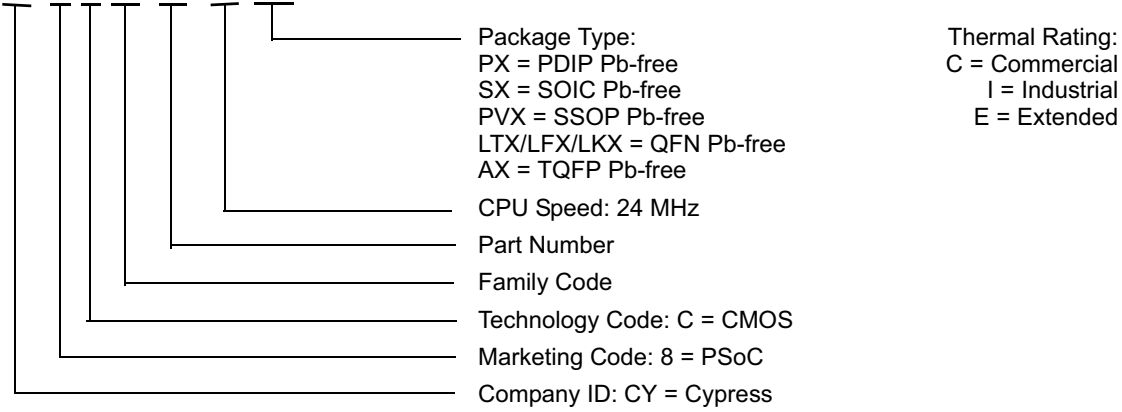
The following table lists the CY8C28xxx PSoC devices key package features and ordering codes.

Package	Ordering Code	Temperature Range	CapSense	Digital Blocks	Regular Analog Blocks	Limited Analog Blocks	HW μ C	Decimators	10-bit SAR ADC	Digital I/O Pins	Analog Inputs	Analog Outputs	Flash (KBytes)	RAM (KBytes)	XRES Pin
28-Pin (210 Mil) SSOP	CY8C28403-24PVXI	-40 to 85	N	12	0	0	2	0	Y	24	8	0	16	1	Y
28-Pin (210 Mil) SSOP (Tape and Reel)	CY8C28403-24PVXIT	-40 to 85	N	12	0	0	2	0	Y	24	8	0	16	1	Y
28-Pin (210 Mil) SSOP	CY8C28413-24PVXI	-40 to 85	Y	12	0	4	1	2	Y	24	24	0	16	1	Y
28-Pin (210 Mil) SSOP (Tape and Reel)	CY8C28413-24PVXIT	-40 to 85	Y	12	0	4	1	2	Y	24	24	0	16	1	Y
44-Pin TQFP	CY8C28513-24AXI	-40 to 85	Y	12	0	4	1	2	Y	40	40	0	16	1	Y
44-Pin TQFP (Tape and Reel)	CY8C28513-24AXIT	-40 to 85	Y	12	0	4	1	2	Y	40	40	0	16	1	Y
48-Pin Sawn QFN	CY8C28623-24LTXI	-40 to 85	N	12	6	0	2	2	N	44	10	2	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28623-24LTXIT	-40 to 85	N	12	6	0	2	2	N	44	10	2	16	1	Y
28-Pin (210 Mil) SSOP	CY8C28433-24PVXI	-40 to 85	Y	12	6	4	1	4	Y	24	24	2	16	1	Y
28-Pin (210 Mil) SSOP (Tape and Reel)	CY8C28433-24PVXIT	-40 to 85	Y	12	6	4	1	4	Y	24	24	2	16	1	Y
44-Pin TQFP	CY8C28533-24AXI	-40 to 85	Y	12	6	4	1	4	Y	40	40	2	16	1	Y
44-Pin TQFP (Tape and Reel)	CY8C28533-24AXIT	-40 to 85	Y	12	6	4	1	4	Y	40	40	2	16	1	Y
20-Pin (210 Mil) SSOP	CY8C28243-24PVXI	-40 to 85	N	12	12	0	2	4	Y	16	16	4	16	1	Y
20-Pin (210 Mil) SSOP (Tape and Reel)	CY8C28243-24PVXIT	-40 to 85	N	12	12	0	2	4	Y	16	16	4	16	1	Y
48-Pin Sawn QFN	CY8C28643-24LTXI	-40 to 85	N	12	12	0	2	4	Y	44	44	4	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28643-24LTXIT	-40 to 85	N	12	12	0	2	4	Y	44	44	4	16	1	Y
28-Pin (210 Mil) SSOP	CY8C28445-24PVXI	-40 to 85	Y	12	12	4	2	4	Y	24	24	4	16	1	Y
28-Pin (210 Mil) SSOP (Tape and Reel)	CY8C28445-24PVXIT	-40 to 85	Y	12	12	4	2	4	Y	24	24	4	16	1	Y
44-Pin TQFP	CY8C28545-24AXI	-40 to 85	Y	12	12	4	2	4	Y	40	40	4	16	1	Y
44-Pin TQFP (Tape and Reel)	CY8C28545-24AXIT	-40 to 85	Y	12	12	4	2	4	Y	40	40	4	16	1	Y
48-Pin Sawn QFN	CY8C28645-24LTXI	-40 to 85	Y	12	12	4	2	4	Y	44	44	4	16	1	Y
48-Pin Sawn QFN (Tape and Reel)	CY8C28645-24LTXIT	-40 to 85	Y	12	12	4	2	4	Y	44	44	4	16	1	Y
28-Pin (210 Mil) SSOP	CY8C28452-24PVXI	-40 to 85	Y	8	12	4	1	4	N	24	24	4	16	1	Y
28-Pin (210 Mil) SSOP (Tape and Reel)	CY8C28452-24PVXIT	-40 to 85	Y	8	12	4	1	4	N	24	24	4	16	1	Y
56-Pin SSOP OCD	CY8C28000-24PVXI	-40 to 85	Y	12	12	4	2	4	Y	44	44	4	16	1	Y

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions

CY 8 C 28 xxx - SP xxxx



Document History Page

Document Title: CY8C28243, CY8C28403, CY8C28413, CY8C28433, CY8C28445, CY8C28452, CY8C28513, CY8C28533, CY8C28545, CY8C28623, CY8C28643, CY8C28645 PSoC® Programmable System-on-Chip Document Number: 001-48111				
Revision	ECN No.	Origin of Change	Submission Date	Description of Change
**	2593460	BTK/PYRS	10/20/08	New document (Revision **).
*A	2652217	BTK/PYRS	02/02/09	Extensive updates to content. Added registers maps. Updated Getting Started section Updated Development Tools section Added some SAR10 ADC specifications. Added more analog system figures
*B	2675937	BTK	03/18/09	Updated DC Analog Reference Specifications tables Minor content updates
*C	2679015	HMI	03/26/2009	Post to external web.
*D	2750217	TDU	08/10/09	Updates to Electrical Specifications section Minor content updates
*E	2768143	TDU	09/23/09	Updated DC Operational Amplifier, DC Analog Reference, DC SAR10ADC, and DC POR specifications; Added Figure 15 and Figure 16; Updated AC TypeE-Operational and AC SAR10ADC specifications
*F	2805324	ALH	11/11/09	Added Contents page. Updated Electrical Specifications .

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