9-Mbit (256 K × 32) Pipelined DCD Sync SRAM

Features

■ Registered inputs and outputs for pipelined operation

■ Optimal for performance (double-cycle deselect)
  ❏ Depth expansion without wait state

■ 256 K × 32-bit common I/O architecture

■ 3.3 V core power supply (V_{DD})

■ 2.5 V / 3.3 V I/O power supply (V_{DDQ})

■ Fast clock-to-output times
  ❏ 2.8 ns (for 250-MHz device)

■ Provide high-performance 3-1-1-1 access rate

■ User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences

■ Multiple chip enables for depth expansion: Three chip enables for A package version and two chip enables for AJ package version

■ Separate processor and controller address strobes

■ Synchronous self-timed writes

■ Asynchronous output enable

■ Available in JEDEC-standard lead-free 100-pin TQFP package

■ "ZZ" sleep mode option

Functional Description[1]

The CY7C1368C SRAM integrates 256 K × 32 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{CE}_1$), depth-expansion chip enables (CE_2 and $\overline{CE}_3$[2]), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), write enables ($\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$, and $\overline{BWE}$), and global write ($\overline{GW}$). Asynchronous inputs include the output enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor ($\overline{ADSP}$) or address strobe controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin ($\overline{ADV}$).
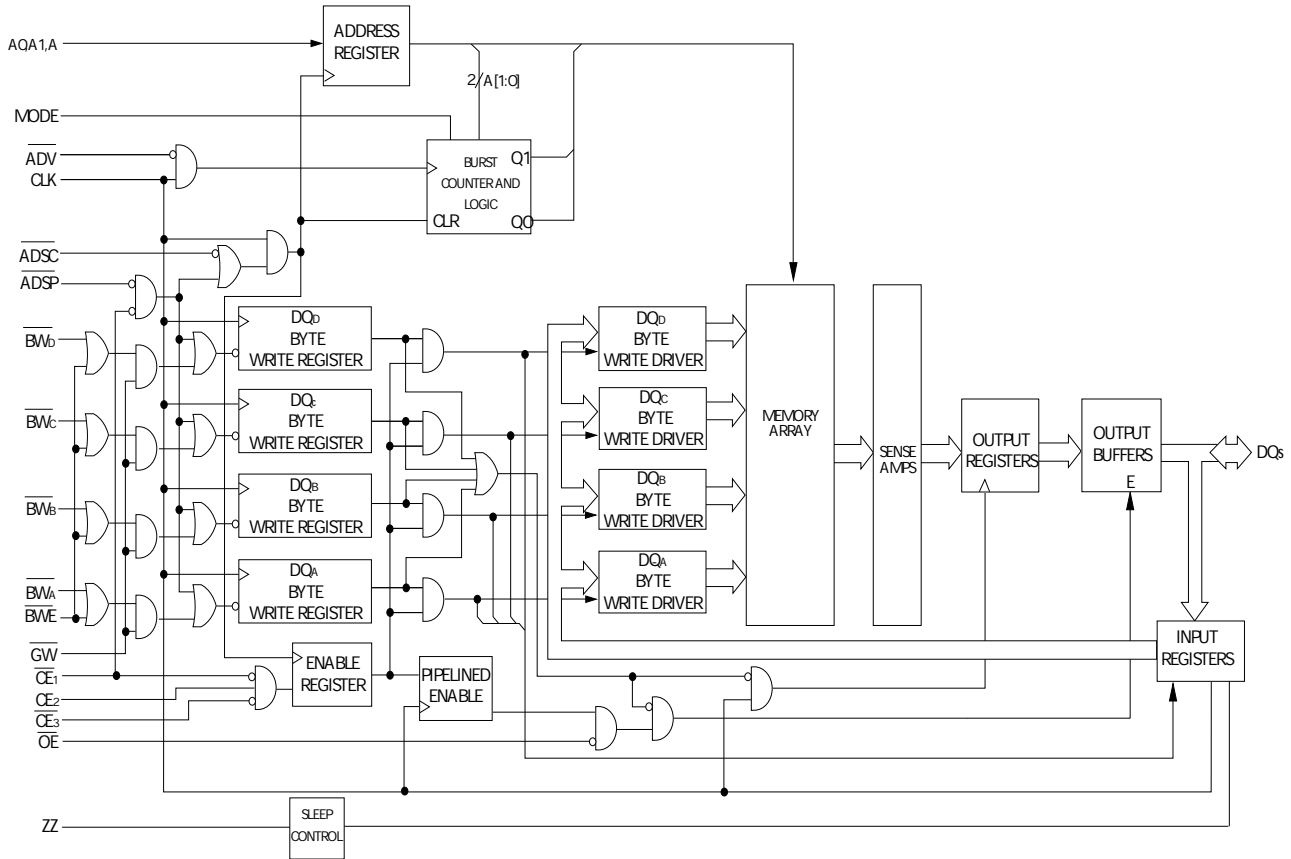
Address, data inputs, and write controls are registered on-chip to initiate a self-timed write cycle. This part supports byte write operations (see Pin Descriptions and Truth Table for further details). Write cycles can be one to four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ active LOW causes all bytes to be written. This device incorporates an additional pipelined enable register which delays turning off the output buffers an additional cycle when a deselect is executed. This feature allows depth expansion without penal izing system performance.

The CY7C1368C operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 V or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

Functional Block Diagram - CY7C1368C (256 K × 32)

Contents

Selection Guide

Description	250 MHz	200 MHz	166 MHz	Unit
Maximum access time	2.8	3.0	3.5	ns
Maximum operating current	250	220	180	mA
Maximum CMOS standby current	40	40	40	mA

Pin Configurations

100-pin TQFP Pinout (2-Chip Enable) (AJ version)

Top View

[+] Feedback
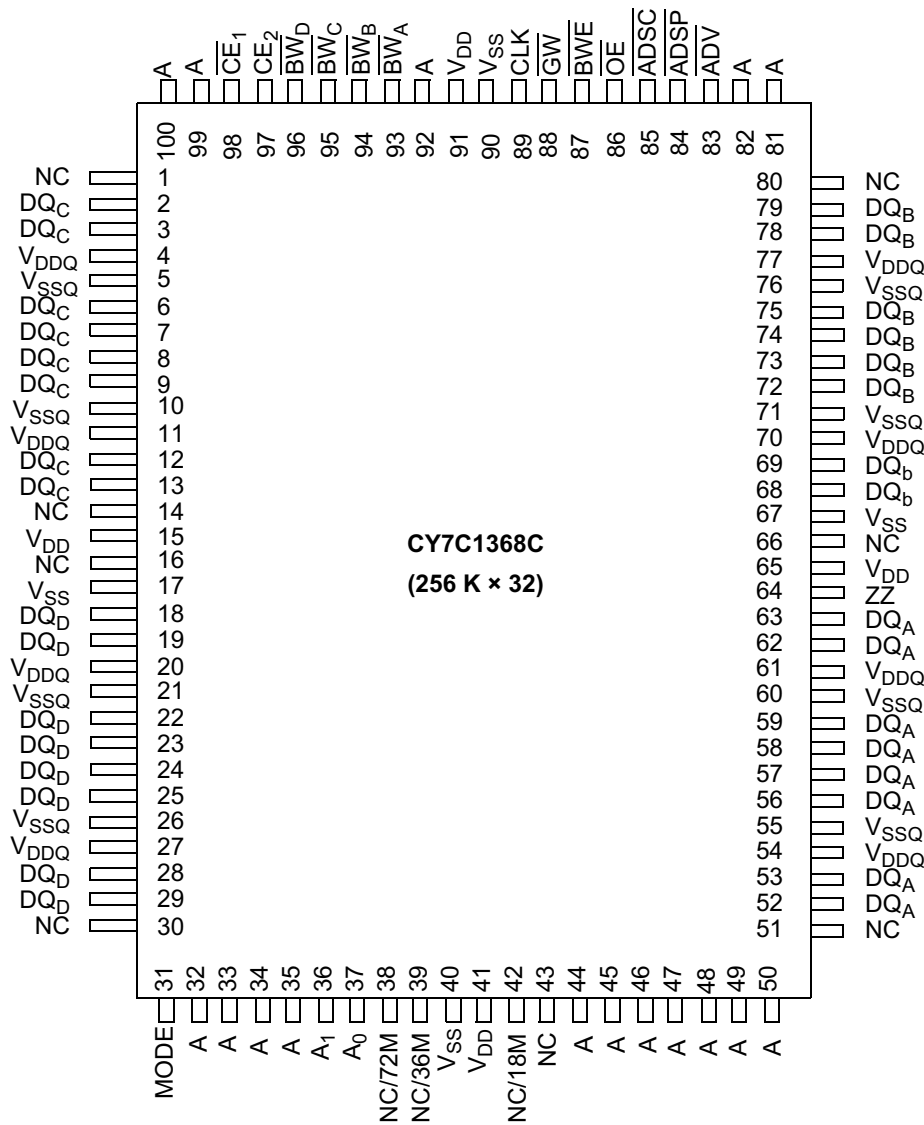
Pin Configurations (continued)

100-pin TQFP Pinout (3-Chip Enable) (A version)
Top View

Top pins (left to right, 100–81): A, A, $\overline{CE}_1$, CE_2, $\overline{BW}_D$, $\overline{BW}_C$, $\overline{BW}_B$, $\overline{BW}_A$, $\overline{CE}_3$, V_{DD}, V_{SS}, CLK, $\overline{GW}$, $\overline{BWE}$, $\overline{OE}$, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, A, A

Left side (pins 1–30):
- 1 NC
- 2 DQ_C
- 3 DQ_C
- 4 V_{DDQ}
- 5 V_{SSQ}
- 6 DQ_C
- 7 DQ_C
- 8 DQ_C
- 9 DQ_C
- 10 V_{SSQ}
- 11 V_{DDQ}
- 12 DQ_C
- 13 DQ_C
- 14 NC
- 15 V_{DD}
- 16 NC
- 17 V_{SS}
- 18 DQ_D
- 19 DQ_D
- 20 V_{DDQ}
- 21 V_{SSQ}
- 22 DQ_D
- 23 DQ_D
- 24 DQ_D
- 25 DQ_D
- 26 V_{SSQ}
- 27 V_{DDQ}
- 28 DQ_D
- 29 DQ_D
- 30 NC

Center: **CY7C1368C** **(256 K × 32)**

Right side (pins 80–51):
- 80 NC
- 79 DQ_B
- 78 DQ_B
- 77 V_{DDQ}
- 76 V_{SSQ}
- 75 DQ_B
- 74 DQ_B
- 73 DQ_B
- 72 DQ_B
- 71 V_{SSQ}
- 70 V_{DDQ}
- 69 DQ_B
- 68 DQ_B
- 67 V_{SS}
- 66 NC
- 65 V_{DD}
- 64 ZZ
- 63 DQ_A
- 62 DQ_A
- 61 V_{DDQ}
- 60 V_{SSQ}
- 59 DQ_A
- 58 DQ_A
- 57 DQ_A
- 56 DQ_A
- 55 V_{SSQ}
- 54 V_{DDQ}
- 53 DQ_A
- 52 DQ_A
- 51 NC

Bottom pins (left to right, 31–50): MODE, A, A, A, A, A_1, A_0, NC/72M, NC/36M, V_{SS}, V_{DD}, NC/18M, A, A, A, A, A, A, A, A

[+] Feedback

Pin Descriptions

Pin	TQFP	Type	Description
A_0, A_1, A	37, 36, 32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 80, 81, 82, 99, 100, 92 (AJC), 43 (AC)	Input-synchronous	**Address inputs used to select one of the 256 K address locations**. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE_1}$, CE_2, and $\overline{CE_3}$[3] are sampled active. $A_{[1:0]}$ are fed to the two-bit counter.
$\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$	93, 94	Input-synchronous	**Byte write select inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	88	Input-synchronous	**Global write enable input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW_{[A:D]}}$ and $\overline{BWE}$).
$\overline{BWE}$	87	Input-synchronous	**Byte write enable input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	89	Input-clock	**Clock input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE_1}$	98	Input-synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select/deselect the device. ADSP is ignored if $\overline{CE_1}$ is HIGH. $\overline{CE_1}$ is sampled only when a new external address is loaded.
CE_2	97	Input-synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE_3}$[2]	92	Input-synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select/deselect the device. Not available for AJ package version. $\overline{CE_3}$[3] is assumed active throughout this document for BGA. $\overline{CE_3}$ is sampled only when a new external address is loaded.
$\overline{OE}$	86	Input-asynchronous	**Output enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	83	Input-synchronous	**Advance input signal, sampled on the rising edge of CLK, active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	84	Input-synchronous	**Address strobe from processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE_1}$ is deasserted HIGH.
$\overline{ADSC}$	85	Input-synchronous	**Address strobe from controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	64	Input-asynchronous	**ZZ "sleep" input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs	2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29, 52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79	I/O-synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs are placed in a tri-state condition.

Note
3. $\overline{CE_3}$ is for A version (3 Chip enable option) only.

Pin Descriptions (continued)

Pin	TQFP	Type	Description
V_{DD}	15, 41, 65, 91	Power supply	**Power supply inputs to the core of the device**.
V_{SS}	17, 40, 67, 90	Ground	**Ground for the core of the device**.
V_{DDQ}	4, 11, 20, 27, 54, 61, 70, 77	I/O power supply	**Power supply for the I/O circuitry**.
V_{SSQ}	5, 10, 21, 26, 55, 60, 71, 76	I/O ground	**Ground for the I/O circuitry**.
MODE	31	Input-static	**Selects burst order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode pin has an internal pull-up.
NC	1, 16, 30, 38, 39, 42, 43(AJC), 51, 66, 80		**No connects**. Not internally connected to the die. NC/(18M,36M, 72M, 144M, 288M, 576M, 1G) **These pins are not connected**. They will be used for expansion to the 18M, 36M, 72M, 144M, 288M, 576M and 1G densities.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock.

The CY7C1368C supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe (ADSP) or the controller address strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable (BWE) and byte write select ($BW_{[A:D]}$) inputs. A global write enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Synchronous chip selects $\overline{CE}_1$, CE_2, $\overline{CE}_3$ and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. ADSP is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2) chip selects are all asserted active, and (3) the write signals (GW, BWE) are all deasserted HIGH. ADSP is ignored if $\overline{CE}_1$ is HIGH. The address presented to the address inputs is stored into the address advancement logic and the address register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the output registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within t_{co} if OE is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tri-stated during the first cycle of the access. After the

first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported.

The CY7C1368C is a double-cycle deselect part. Once the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output will tri-state immediately after the next clock rise.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) chip select is asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The write signals (GW, BWE, and $BW_{[A:D]}$) and ADV inputs are ignored during this first cycle.

ADSP triggered write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQx inputs is written into the corresponding address location in the memory core. If GW is HIGH, then the write operation is controlled by BWE and $BW_{[A:D]}$ signals. The CY7C1368C provides byte write capability that is described in the Write Cycle Description table. Asserting the byte write enable input (BWE) with the selected byte write input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1368C is a common I/O device, the output enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by $\overline{ADSC}$

ADSC write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3) chip select is asserted active, and (4) the appropriate combination of the write inputs (GW, BWE, and $BW_{[A:D]}$) are asserted active to conduct a write to the desired byte(s). ADSC triggered write accesses require a single clock cycle to complete. The address presented is loaded into the address register and

the address advancement logic while being delivered to the memory core. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the DQ_X is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1368C is a common I/O device, the output enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ_X inputs. Doing so will tri-state the output drivers. As a safety precaution, DQ_X are automatically tri-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1368C provides a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input. Both read and write burst operations are supported.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. CEs, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1, A0	Second Address A1, A0	Third Address A1, A0	Fourth Address A1, A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Truth Table[4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE_1}$	$\overline{CE_3}$	CE_2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected cycle, power-down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	X	L	L	L	X	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	H	X	L	L	X	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	X	L	L	H	L	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	H	X	L	H	L	X	X	X	L-H	Tri-state
ZZ mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tri-state
Read cycle, begin burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
Read cycle, begin burst	External	L	L	H	L	L	X	X	X	H	L-H	Tri-state
Write cycle, begin burst	External	L	L	H	L	H	L	X	L	X	L-H	D
Read cycle, begin burst	External	L	L	H	L	H	L	X	H	L	L-H	Q

Notes
4. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
5. $\overline{WRITE}$ = L when any one or more byte write enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all byte write enable signals (BW_A, BW_B, BW_C, BW_D), BWE, GW = H.
6. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
7. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}_{[A:D]}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
8. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when OE is active (LOW).

Truth Table[4, 5, 6, 7, 8] (continued)

Operation	Address Used	$\overline{CE_1}$	$\overline{CE_3}$	CE_2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Read cycle, begin burst	External	L	L	H	L	H	L	X	H	H	L-H	Tri-state
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-state
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-state
Write cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-state
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-state
Write cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Truth Table for Read/Write[9, 10]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_A}$	$\overline{BW_B}$	$\overline{BW_C}$	$\overline{BW_D}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte A - (DQ_A and DQP_A)	H	L	L	H	H	H
Write byte B - (DQ_B and DQP_B)	H	L	H	L	H	H
Write byte C - (DQ_C and DQP_C)	H	L	H	H	L	H
Write byte D - (DQ_D and DQP_D)	H	L	H	H	H	L
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	sleep mode standby current	$ZZ \geq V_{DD} - 0.2$ V	–	50	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2$ V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ recovery time	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit sleep current	This parameter is sampled	0	–	ns

Notes
9. X = "Don't Care." H = Logic HIGH, L =Logic LOW.
10. $\overline{WRITE}$ = L when any one or more byte write enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all byte write enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$), $\overline{BWE}$, $\overline{GW}$ = H.

[+] Feedback

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with
power applied .... –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND ....–0.5 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND .... –0.5 V to +V_{DD}

DC voltage applied to outputs
in tri-state ....–0.5 V to V_{DDQ} + 0.5 V

DC input voltage .... –0.5 V to V_{DD}+ 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage.. > 2001 V

(per MIL-STD-883,method 3015)

Latch-up current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Electrical Characteristics

Over the Operating Range[11, 12]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power supply voltage			3.135	3.6	V
V_{DDQ}	I/O supply voltage	for 3.3 V I/O		3.135	V_{DD}	V
		for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage[11]	for 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage[11]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}			5	µA
	Input current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}			30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DDQ}, output disabled		–5	5	µA
I_{DD}	V_{DD} operating supply current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	4-ns cycle, 250 MHz	–	250	mA
			5-ns cycle, 200 MHz	–	220	mA
			6-ns cycle,166 MHz	–	180	mA
I_{SB1}	Automatic CE power-down current—TTL inputs	V_{DD} = Max, device deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = 1/t_{CYC}	4-ns cycle, 250 MHz	–	130	mA
			5-ns cycle, 200 MHz		120	
			6-ns cycle,166 MHz		110	

Notes
11. Overshoot: V_{IH}(AC) < V_{DD} + 1.5 V(Pulse width less than t_{CYC}/2), undershoot: V_{IL}(AC) > –2 V(Pulse width less than t_{CYC}/2).
12. Power-up: Assumes a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

[+] Feedback

Electrical Characteristics (continued)

Over the Operating Range[11, 12]

Parameter	Description	Test Conditions		Min	Max	Unit
I_{SB2}	Automatic CE power-down current—CMOS inputs	V_{DD} = Max, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = 0	All speeds	–	40	mA
I_{SB3}	Automatic CE power-down current—CMOS inputs	V_{DD} = Max., device deselected, or $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = f_{MAX} = 1/t_{CYC}	4-ns cycle, 250 MHz	–	120	mA
			5-ns cycle, 200 MHz		110	
			6-ns cycle, 166 MHz		100	
I_{SB4}	Automatic CE power-down current—TTL inputs	V_{DD} = Max, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	All speeds	–	40	mA

Capacitance[13]

Parameter	Description	Test Conditions	100 TQFP Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V V_{DDQ} = 2.5 V	4	pF
C_{CLK}	Clock input capacitance		4	pF
$C_{I/O}$	Input/output capacitance		4	pF

Thermal Characteristics[13]

Parameter	Description	Test Conditions	100 TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	29.41	°C/W
Θ_{JC}	Thermal resistance (junction to case)		6.13	°C/W

AC Test Loads and Waveforms

3.3 V I/O Test Load
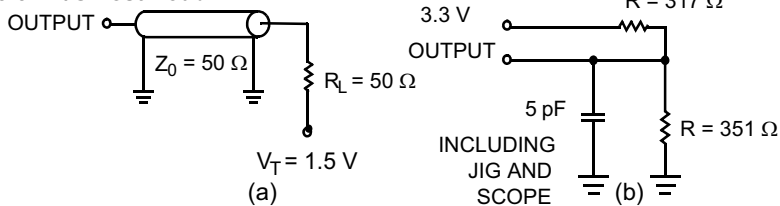
2.5 V I/O Test Load
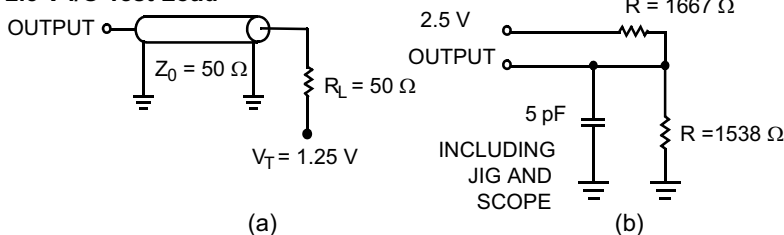
Note
13. Tested initially and after any design or process change that may affect these parameters.

[+] Feedback

Switching Characteristics

Over the Operating Range [14, 15]

Parameter	Description	–250		–200		–166		Unit
		Min	Max	Min	Max	Min	Max	
t_{POWER}	V_{DD}(Typical) to the first access[16]	1	–	1	–	1	–	ms
Clock								
t_{CYC}	Clock cycle time	4.0	–	5.0	–	6.0	–	ns
t_{CH}	Clock HIGH	1.8	–	2.0	–	2.4	–	ns
t_{CL}	Clock LOW	1.8	–	2.0	–	2.4	–	ns
Output Times								
t_{CO}	Data output valid after CLK rise	–	2.8	–	3.0	–	3.5	ns
t_{DOH}	Data output hold after CLK rise	1.25	–	1.25	–	1.25	–	ns
t_{CLZ}	Clock to low Z[17, 18, 19]	1.25	–	1.25	–	1.25	–	ns
t_{CHZ}	Clock to high Z[17, 18, 19]	1.25	2.8	1.25	3.0	1.25	3.5	ns
t_{OEV}	OE LOW to output valid	–	2.8	–	3.0	–	3.5	ns
t_{OELZ}	OE LOW to output low Z[17, 18, 19]	0	–	0	–	0	–	ns
t_{OEHZ}	OE HIGH to output high Z[17, 18, 19]	–	2.8	–	3.0	–	3.5	ns
Set-up Times								
t_{AS}	Address set-up before CLK rise	1.4	–	1.5	–	1.5	–	ns
t_{ADS}	ADSC, ADSP set-up before CLK rise	–	–	1.5	–	1.5	–	ns
t_{ADVS}	ADV set-up before CLK rise	1.4	–	1.5	–	1.5	–	ns
t_{WES}	GW, OE, BW$_{[A:D]}$ set-up before CLK rise	1.4	–	1.5	–	1.5	–	ns
t_{DS}	Data input set-up before CLK rise	1.4	–	1.5	–	1.5	–	ns
t_{CES}	Chip enable set-up before CLK rise	1.4	–	1.5	–	1.5	–	ns
Hold Times								
t_{AH}	Address hold after CLK rise	0.4	–	0.5	–	0.5	–	ns
t_{ADH}	ADSP, ADSC hold after CLK rise	0.4	–	0.5	–	0.5	–	ns
t_{ADVH}	ADV hold after CLK rise	0.4	–	0.5	–	0.5	–	ns
t_{WEH}	GW, BWE, BW$_{[A:D]}$ hold after CLK rise	0.4	–	0.5	–	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.4	–	0.5	–	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.4	–	0.5	–	0.5	–	ns

Notes
14. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
15. Test conditions shown in (a) of AC Test Loads unless otherwise noted.
16. This part has a voltage regulator internally; tpower is the time that the power needs to be supplied above V_{DD} minimum initially before a read or write operation can be initiated.
17. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
18. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
19. This parameter is sampled and not 100% tested.
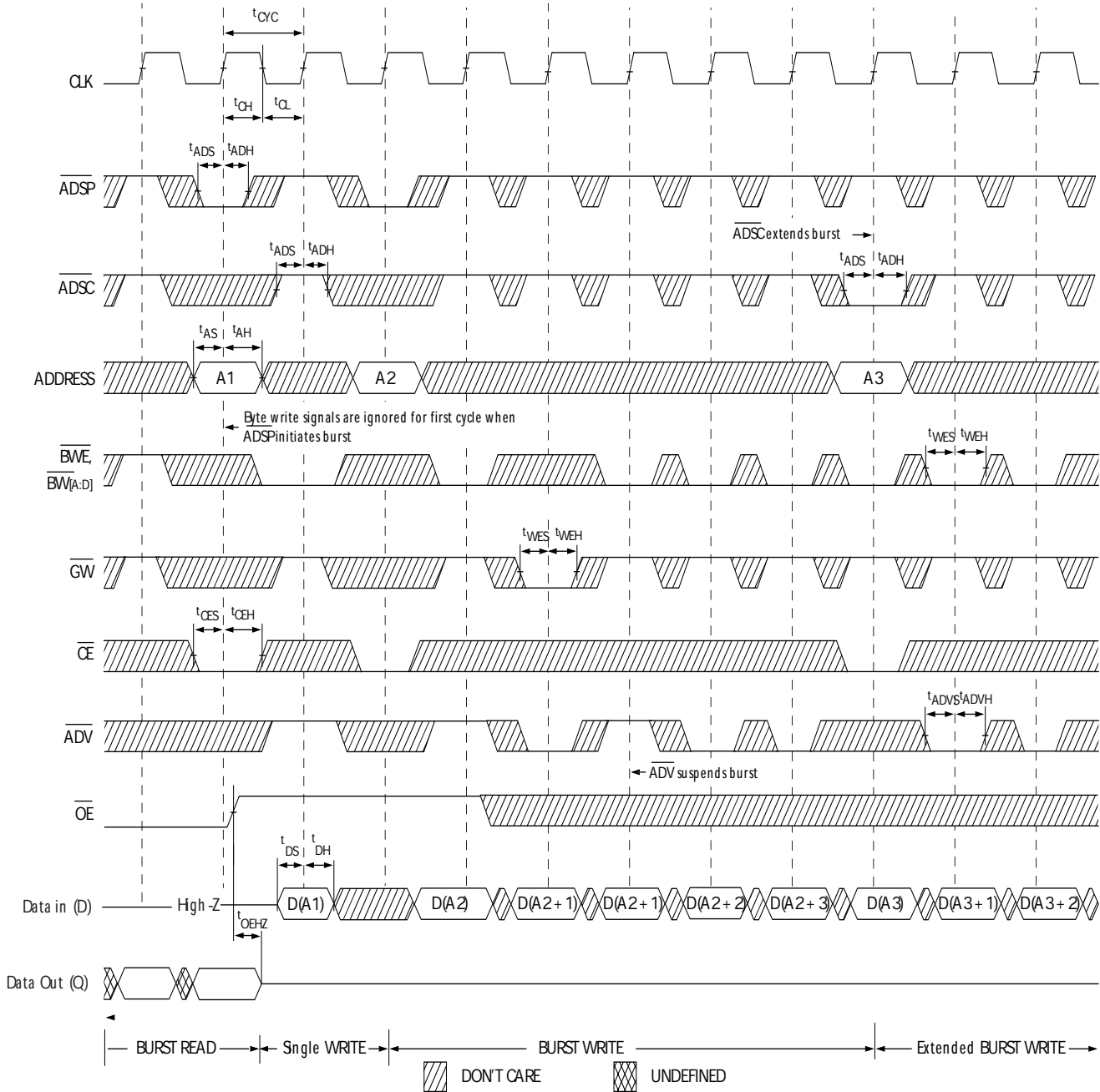
[+] Feedback

Switching Waveforms

Read Timing[20]
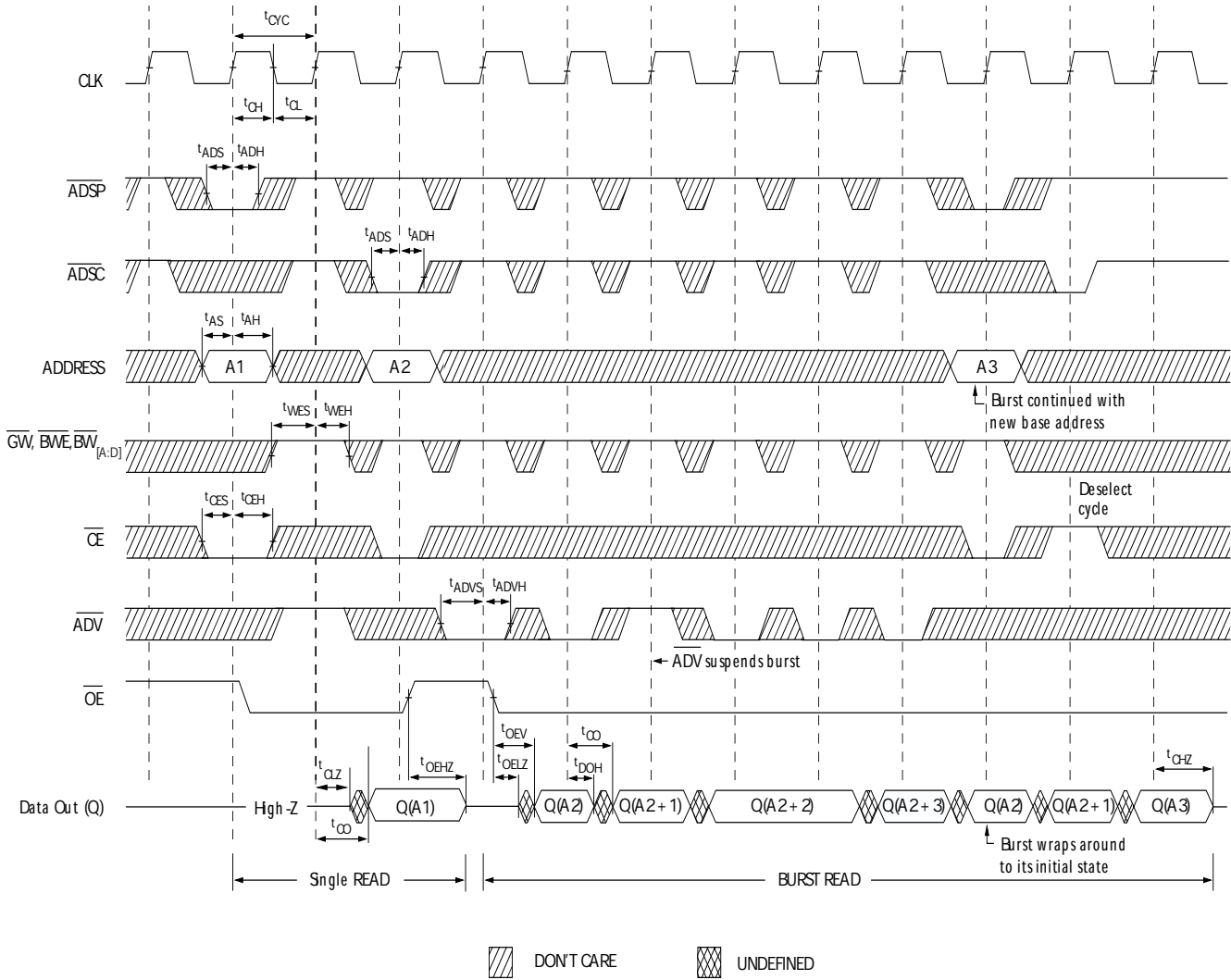
Note
20. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE_1}$ is HIGH or CE_2 is LOW or $\overline{CE_3}$ is HIGH.
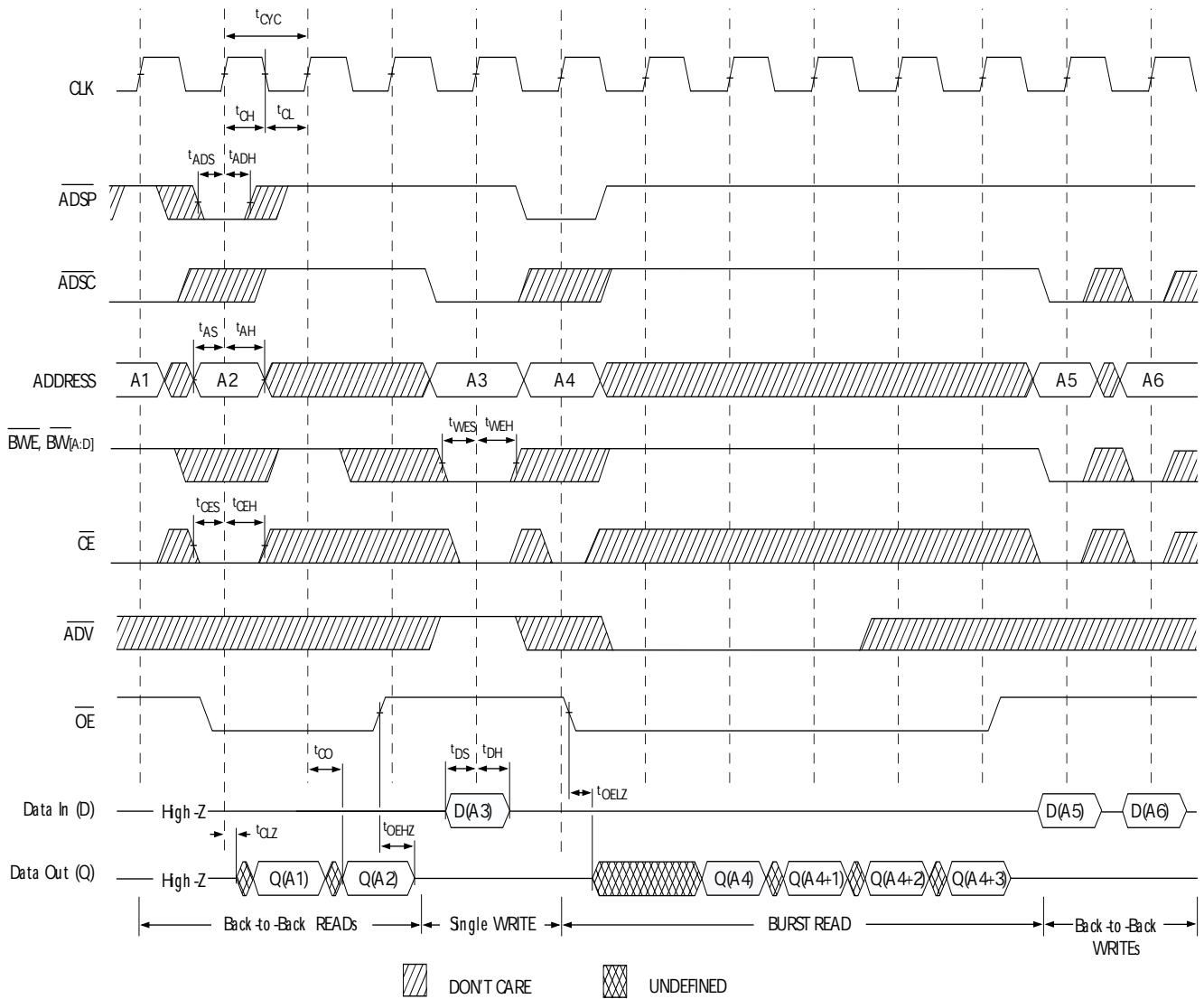
Switching Waveforms (continued)

Write Timing[21, 22]

Notes
21. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
22. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_{[A:D]}$ LOW.

Switching Waveforms (continued)

Read/Write Timing[23, 24, 25]

Notes
23. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
24. The data bus (Q) remains in tri-state following a WRITE cycle unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
25. $\overline{GW}$ is HIGH.

[+] Feedback

Switching Waveforms (continued)

ZZ Mode Timing [26, 27]
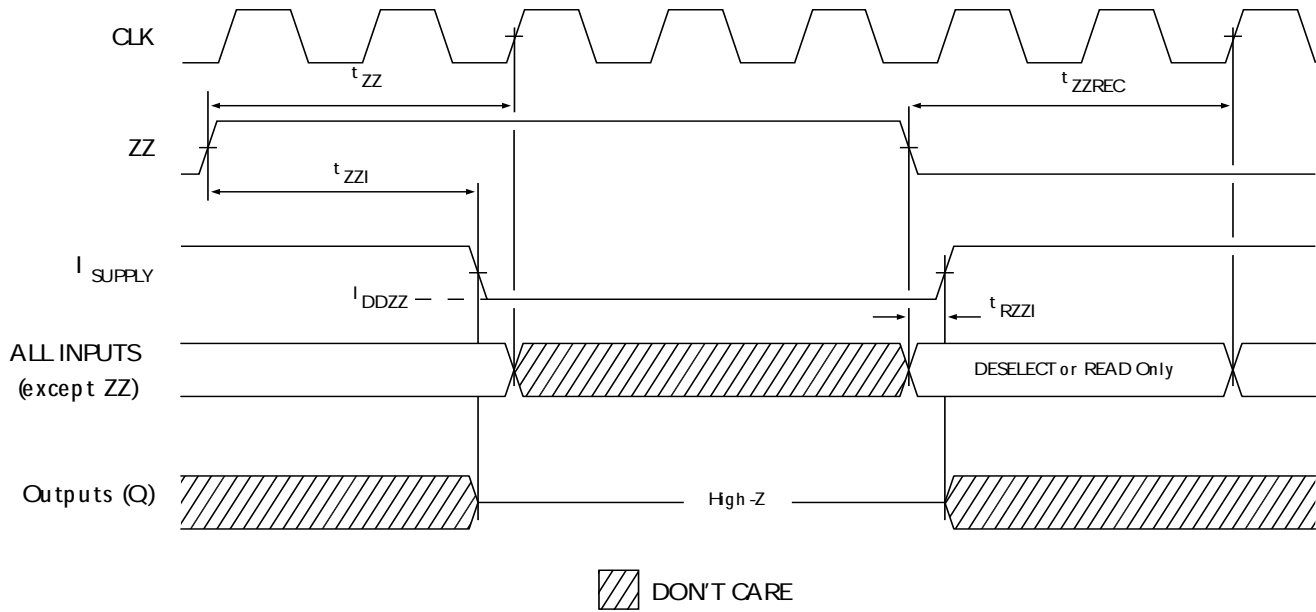
Notes
26. Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
27. DQs are in tri-state when exiting ZZ sleep mode.

[+] Feedback

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.

For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
166	CY7C1368C-166AXC	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free (3 Chip enable)	Commercial

Ordering Code Definitions

CY7C 1368 C - 166 AX C

Temperature range:
C = Commercial

Package Type:
AX = 100-pin TQFP (Pb-free)

Speed Grade (166 MHz)

Process Technology ≥ 90 nm

1368 = DCD, 256 K × 32 (9 Mb)

CY7C = Cypress SRAMs

[+] Feedback
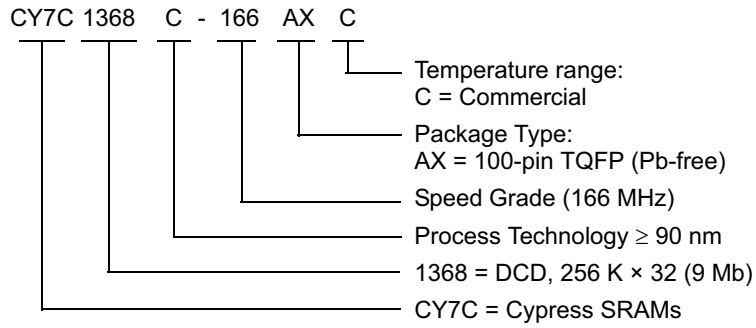
Package Diagram

100-pin TQFP (14 x 20 x 1.4 mm), 51-85050
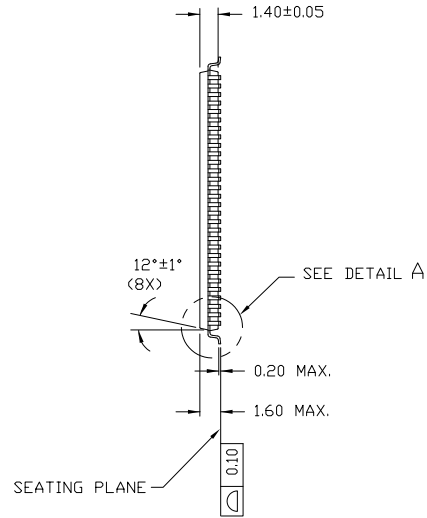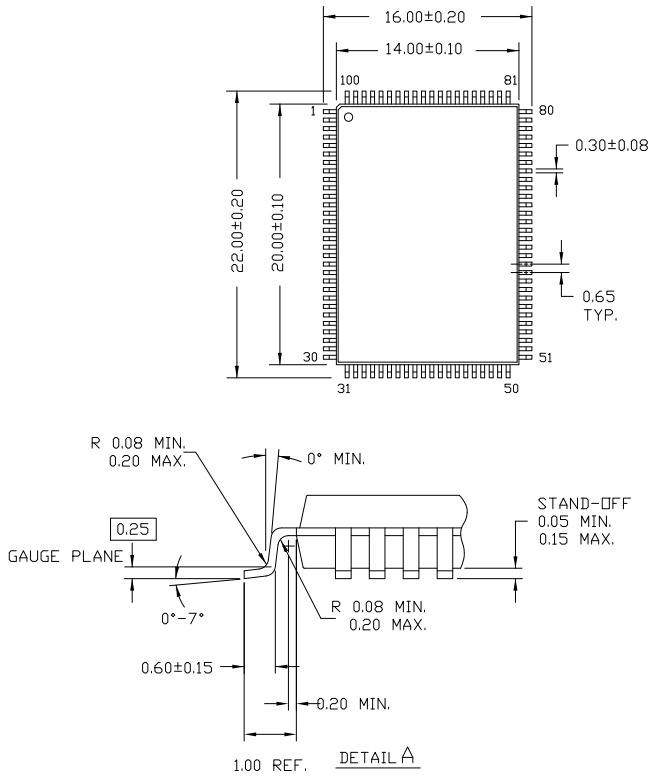
NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *C

[+] Feedback

Acronyms

Acronym	Description
CE	chip enable
CEN	clock enable
CMOS	complementary metal oxide semiconductor
FPBGA	fine-pitch ball grid array
I/O	input/output
OE	output enable
SRAM	static random access memory
TQFP	thin quad flat pack
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
ms	milli seconds
MHz	Mega Hertz
pF	pico Farad
W	Watts
°C	degree Celcius

[+] Feedback

Document History Page

Document Title: CY7C1368C 9-Mbit (256 K × 32) Pipelined DCD Sync SRAM				
Document Number: 38-05686				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	286269	See ECN	PCI	New data sheet
*A	323636	See ECN	PCI	Changed frequency of 225 MHz to 250 MHz Added t_{CYC} to 4.0 ns for 250 MHz Changed Θ_{JA} and Θ_{JC} for TQFP Package from 25 and 9 °C/W to 29.41 and 6.13 °C/W respectively Added Industrial temperature range Replaced Snooze with Sleep in the ZZ Mode Electrical Characteristics Added 3 chip enable and 2 chip enable for AX and AJX packages in the ordering information table
*B	332879	See ECN	PCI	Shaded 250 MHz speed bin in the AC/DC Table and Selection Guide Added Address Expansion pins in the Pin Definition Table Modified V_{OL}, V_{OH} test conditions Corrected V_{DDQ} from (2.5V − 5% to V_{DD}) to (3.3V −5%/+10%) on page# 9 Updated Ordering Information Table
*C	377095	See ECN	PCI	Changed I_{SB2} from 30 to 40 mA Modified test condition in note# 9 from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$
*D	408725	See ECN	RXU	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Converted from Preliminary to Final Replaced Package Name column with Package Diagram in the Ordering Information table Updated the ordering information
*E	429278	See ECN	NXR	Added 2.5VI/O option Updated Ordering Information Table
*F	501828	See ECN	VKN	Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND Updated the Ordering Information table.
*G	2896585	03/20/2010	NJY	Removed obsolete parts from Ordering Information table. Updated package diagram, data sheet template, and Sales, Solutions, and Legal Information section.
*H	3046851	10/04/2010	NJY	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Minor edits and updated in new template.

[+] Feedback

Sales, Solutions, and Legal Information

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PSoC 1 | PSoC 3 | PSoC 5

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