



**CY7C1041G**  
**CY7C1041GE**

## 4-Mbit (256K words × 16 bit) Static RAM with Error-Correcting Code (ECC)

### Features

- High speed
  - $t_{AA} = 10 \text{ ns} / 15 \text{ ns}$
- Embedded ECC for single-bit error correction<sup>[1]</sup>
- Low active and standby currents
  - Active current:  $I_{CC} = 38\text{-mA}$  typical
  - Standby current:  $I_{SB2} = 6\text{-mA}$  typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Pb-free 44-pin SOJ, 44-pin TSOP II, and 48-ball VFBGA packages

### Functional Description

CY7C1041G and CY7C1041GE are high-performance CMOS fast static RAM devices with embedded ECC. Both devices are offered in single and dual chip-enable options and in multiple pin configurations. The CY7C1041GE device includes an ERR pin that signals an error-detection and correction event during a read cycle.

Data writes are performed by asserting the Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW, while providing the data on I/O<sub>0</sub> through I/O<sub>15</sub> and address on A<sub>0</sub> through A<sub>17</sub> pins. The Byte High Enable (BHE) and Byte Low Enable (BLE) inputs control write operations to the upper and lower bytes of the specified memory location. BHE controls I/O<sub>8</sub> through I/O<sub>15</sub> and BLE controls I/O<sub>0</sub> through I/O<sub>7</sub>.

Data reads are performed by asserting the Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) inputs LOW and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O<sub>0</sub> through I/O<sub>15</sub>). Byte accesses can be performed by asserting the required byte enable signal ( $\overline{BHE}$  or  $\overline{BLE}$ ) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state during the following events:

- The device is deselected ( $\overline{CE}$  HIGH)
- The control signals ( $\overline{OE}$ ,  $\overline{BLE}$ ,  $\overline{BHE}$ ) are de-asserted

On the CY7C1041GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = HIGH)<sup>[1]</sup>. See the [Truth Table on page 14](#) for a complete description of read and write modes.

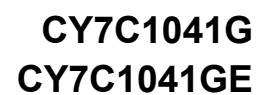
The logic block diagram is on page 2.

### Product Portfolio

| Product <sup>[2]</sup> | Features and Options (see <a href="#">Pin Configurations on page 4</a> ) | Range      | V <sub>CC</sub> Range (V) | Speed (ns)<br>10/15 | Power Dissipation                |     |                                |     |
|------------------------|--------------------------------------------------------------------------|------------|---------------------------|---------------------|----------------------------------|-----|--------------------------------|-----|
|                        |                                                                          |            |                           |                     | Operating I <sub>CC</sub> , (mA) |     | Standby, I <sub>SB2</sub> (mA) |     |
|                        |                                                                          |            |                           |                     | f = f <sub>max</sub>             |     |                                |     |
|                        |                                                                          |            |                           |                     | Typ <sup>[3]</sup>               | Max | Typ <sup>[3]</sup>             | Max |
| CY7C1041G(E)18         | Single or Dual Chip Enables<br><br>Optional ERR pins                     | Industrial | 1.65 V–2.2 V              | 15                  | –                                | 40  | 6                              | 8   |
| CY7C1041G(E)30         |                                                                          |            | 2.2 V–3.6 V               | 10                  | 38                               | 45  |                                |     |
| CY7C1041G(E)           |                                                                          |            | 4.5 V–5.5 V               | 10                  | 38                               | 45  |                                |     |

#### Notes

1. This device does not support automatic write-back on error detection.
2. The ERR pin is available only for devices which have ERR option "E" in the ordering code. Refer [Ordering Information on page 15](#) for details.
3. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for a V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V (for a V<sub>CC</sub> range of 2.2 V–3.6 V), and V<sub>CC</sub> = 5 V (for a V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.

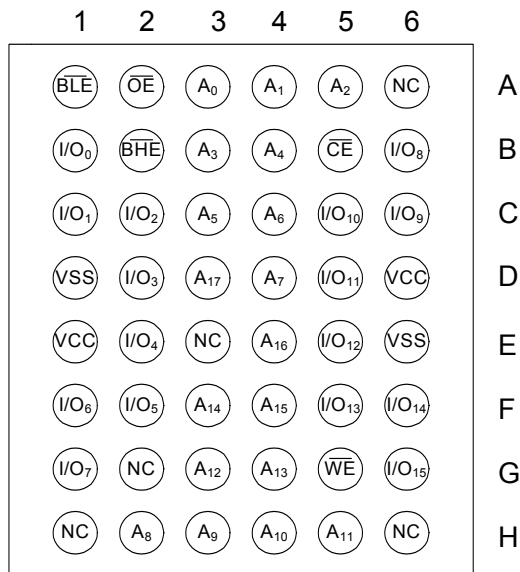
[illegible][illegible]

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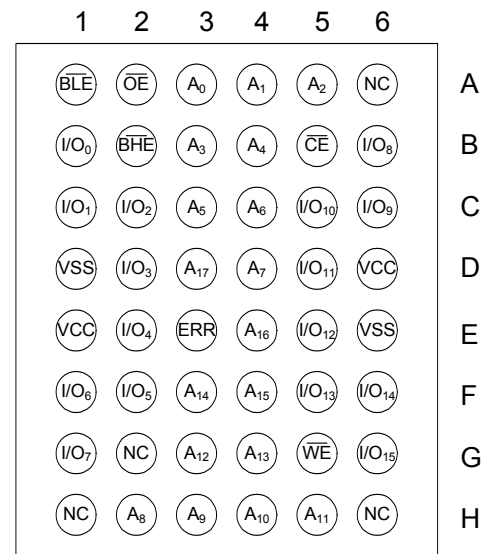
|                                             |           |                                                      |           |
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## Pin Configurations

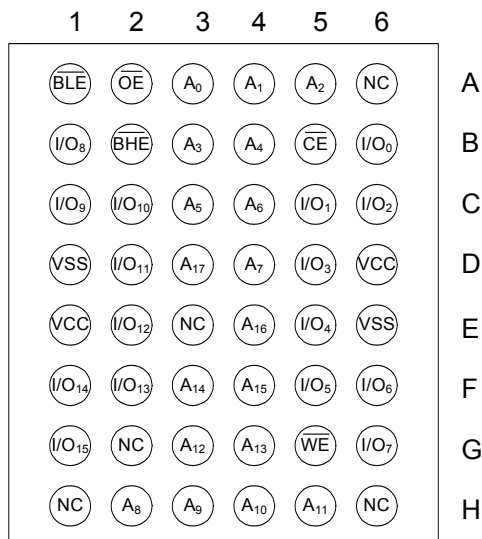
**Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable without ERR, CY7C1041G** <sup>[4]</sup>, Package/Grade ID: BVXI <sup>[6]</sup>



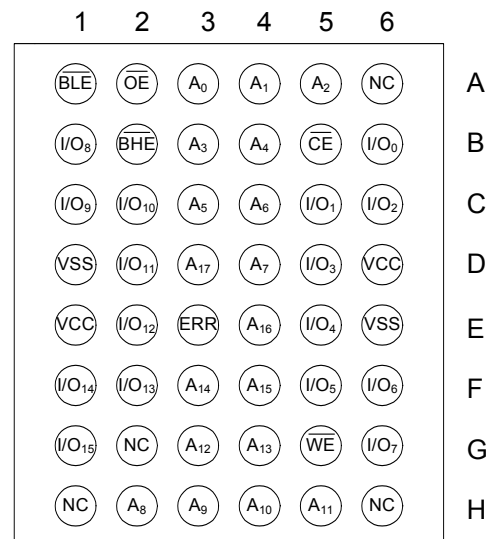
**Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable with ERR, CY7C1041GE** <sup>[4, 5]</sup>, Package/Grade ID: BVXI <sup>[6]</sup>



**Figure 3. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable without ERR, CY7C1041G** <sup>[4]</sup>, Package/Grade ID: BVJXI <sup>[6]</sup>



**Figure 4. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable with ERR, CY7C1041GE** <sup>[4, 5]</sup>, Package/Grade ID: BVJXI <sup>[6]</sup>



### Notes

- NC pins are not connected internally to the die.
- ERR is an output pin.
- Package type BVJXI is JEDEC compliant compared to package type BVXI. The difference between the two is that the higher and lower byte I/Os (I/O<sub>[7:0]</sub> and I/O<sub>[15:8]</sub> balls are swapped.

## Pin Configurations (continued)

Figure 5. 44-pin TSOP II/44-pin SOJ Single Chip Enable with ERR, CY7C1041GE [7, 8]

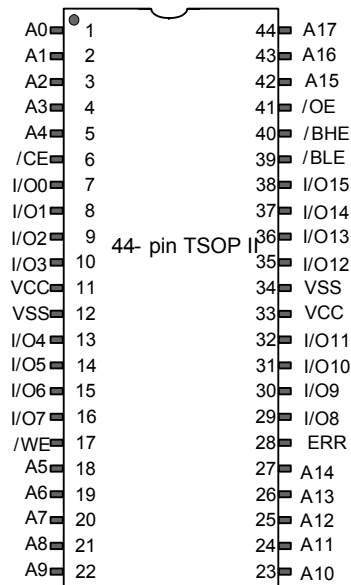
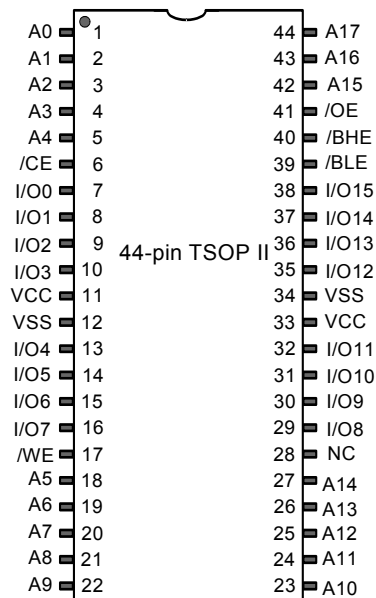


Figure 6. 44-pin TSOP II/44-pin SOJ Single Chip Enable without ERR, CY7C1041G [7]



### Notes

7. NC pins are not connected internally to the die.
8. ERR is an output pin.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature  
with power applied ..... -55 °C to +125 °C

Supply voltage  
on  $V_{CC}$  relative to GND <sup>[9]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC voltage applied to outputs  
in HI-Z State <sup>[9]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage <sup>[9]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (in LOW state) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

## Operating Range

| Grade      | Ambient Temperature | $V_{CC}$                                              |
|------------|---------------------|-------------------------------------------------------|
| Industrial | -40 °C to +85 °C    | 1.65 V to 2.2 V,<br>2.2 V to 3.6 V,<br>4.5 V to 5.5 V |

## DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

| Parameter | Description                                   | Test Conditions                                                                                                  | 10 ns / 15 ns                  |                     |                               | Unit |
|-----------|-----------------------------------------------|------------------------------------------------------------------------------------------------------------------|--------------------------------|---------------------|-------------------------------|------|
|           |                                               |                                                                                                                  | Min                            | Typ <sup>[10]</sup> | Max                           |      |
| $V_{OH}$  | Output HIGH voltage                           | 1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OH} = -0.1$ mA                                                          | 1.4                            | —                   | —                             | V    |
|           |                                               | 2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OH} = -1.0$ mA                                                           | 2                              | —                   | —                             |      |
|           |                                               | 2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA                                                           | 2.2                            | —                   | —                             |      |
|           |                                               | 4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA                                                           | 2.4                            | —                   | —                             |      |
|           |                                               | 4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -0.1$ mA                                                           | $V_{CC} - 0.5$ <sup>[11]</sup> | —                   | —                             |      |
| $V_{OL}$  | Output LOW voltage                            | 1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OL} = 0.1$ mA                                                           | —                              | —                   | 0.2                           | V    |
|           |                                               | 2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OL} = 2$ mA                                                              | —                              | —                   | 0.4                           |      |
|           |                                               | 2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OL} = 8$ mA                                                              | —                              | —                   | 0.4                           |      |
|           |                                               | 4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OL} = 8$ mA                                                              | —                              | —                   | 0.4                           |      |
| $V_{IH}$  | Input HIGH voltage                            | 1.65 V to 2.2 V —                                                                                                | 1.4                            | —                   | $V_{CC} + 0.2$ <sup>[9]</sup> | V    |
|           |                                               | 2.2 V to 2.7 V —                                                                                                 | 2                              | —                   | $V_{CC} + 0.3$ <sup>[9]</sup> |      |
|           |                                               | 2.7 V to 3.6 V —                                                                                                 | 2                              | —                   | $V_{CC} + 0.3$ <sup>[9]</sup> |      |
|           |                                               | 4.5 V to 5.5 V —                                                                                                 | 2.2                            | —                   | $V_{CC} + 0.5$ <sup>[9]</sup> |      |
| $V_{IL}$  | Input LOW voltage                             | 1.65 V to 2.2 V —                                                                                                | -0.2 <sup>[9]</sup>            | —                   | 0.4                           | V    |
|           |                                               | 2.2 V to 2.7 V —                                                                                                 | -0.3 <sup>[9]</sup>            | —                   | 0.6                           |      |
|           |                                               | 2.7 V to 3.6 V —                                                                                                 | -0.3 <sup>[9]</sup>            | —                   | 0.8                           |      |
|           |                                               | 4.5 V to 5.5 V —                                                                                                 | -0.5 <sup>[9]</sup>            | —                   | 0.8                           |      |
| $I_{IX}$  | Input leakage current                         | $GND \leq V_{IN} \leq V_{CC}$                                                                                    | -1                             | —                   | +1                            | μA   |
| $I_{OZ}$  | Output leakage current                        | $GND \leq V_{OUT} \leq V_{CC}$ , Output disabled                                                                 | -1                             | —                   | +1                            | μA   |
| $I_{CC}$  | Operating supply current                      | Max $V_{CC}$ , $I_{OUT} = 0$ mA, CMOS levels, $f = 100$ MHz                                                      | —                              | 38                  | 45                            | mA   |
|           |                                               | $f = 66.7$ MHz                                                                                                   | —                              | —                   | 40                            |      |
| $I_{SB1}$ | Automatic CE power-down current – TTL inputs  | Max $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$        | —                              | —                   | 15                            | mA   |
| $I_{SB2}$ | Automatic CE power-down current – CMOS inputs | Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ | —                              | 6                   | 8                             | mA   |

### Notes

9.  $V_{IL(\text{min})} = -2.0$  V and  $V_{IH(\text{max})} = V_{CC} + 2$  V for pulse durations of less than 2 ns.

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8$  V (for  $V_{CC}$  range of 1.65 V – 2.2 V),  $V_{CC} = 3$  V (for  $V_{CC}$  range of 2.2 V – 3.6 V), and  $V_{CC} = 5$  V (for  $V_{CC}$  range of 4.5 V – 5.5 V),  $T_A = 25$  °C.

11. This parameter is guaranteed by design and not tested.

## Capacitance

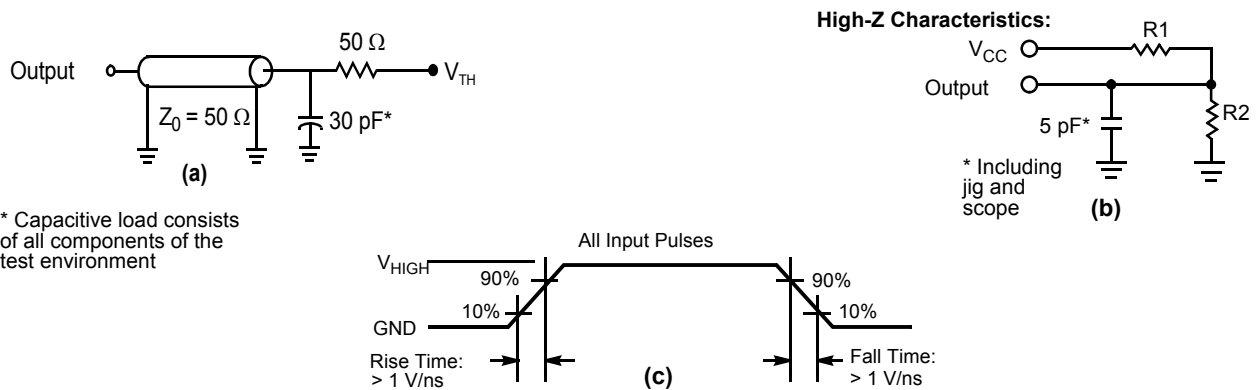
| Parameter <sup>[12]</sup> | Description       | Test Conditions                                                                  | 48-ball VFBGA | 44-pin SOJ | 44-pin TSOP II | Unit |
|---------------------------|-------------------|----------------------------------------------------------------------------------|---------------|------------|----------------|------|
| $C_{IN}$                  | Input capacitance | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ ,<br>$V_{CC} = V_{CC(\text{typ})}$ | 10            | 10         | 10             | pF   |
| $C_{OUT}$                 | I/O capacitance   |                                                                                  | 10            | 10         | 10             | pF   |

## Thermal Resistance

| Parameter <sup>[12]</sup> | Description                              | Test Conditions                                                         | 48-ball VFBGA | 44-pin SOJ | 44-pin TSOP II | Unit               |
|---------------------------|------------------------------------------|-------------------------------------------------------------------------|---------------|------------|----------------|--------------------|
| $\Theta_{JA}$             | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board | 31.35         | 55.37      | 68.85          | $^\circ\text{C/W}$ |
| $\Theta_{JC}$             | Thermal resistance (junction to case)    |                                                                         | 14.74         | 30.41      | 15.97          | $^\circ\text{C/W}$ |

## AC Test Loads and Waveforms

Figure 7. AC Test Loads and Waveforms <sup>[13]</sup>



| Parameters | 1.8 V | 3.0 V | 5.0 V | Unit     |
|------------|-------|-------|-------|----------|
| R1         | 1667  | 317   | 317   | $\Omega$ |
| R2         | 1538  | 351   | 351   | $\Omega$ |
| $V_{TH}$   | 0.9   | 1.5   | 1.5   | V        |
| $V_{HIGH}$ | 1.8   | 3     | 3     | V        |

### Notes

12. Tested initially and after any design or process changes that may affect these parameters.

13. Full-device AC operation assumes a 100- $\mu\text{s}$  ramp time from 0 to  $V_{CC(\text{min})}$  and a 100- $\mu\text{s}$  wait time after  $V_{CC}$  stabilization.

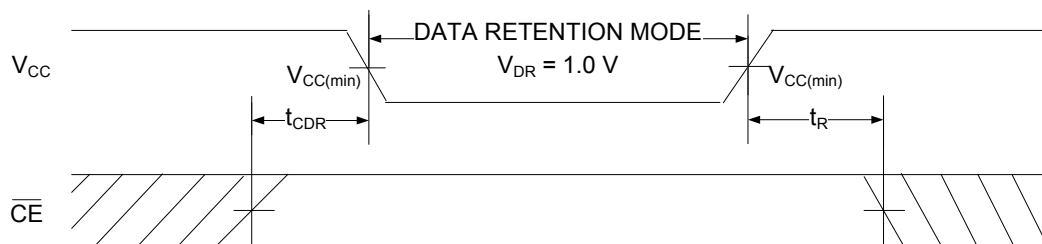
## Data Retention Characteristics

Over the operating range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

| Parameter                 | Description                          | Conditions                                                                                                                                                                                     | Min | Max | Unit |
|---------------------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|
| $V_{\text{DR}}$           | $V_{\text{CC}}$ for data retention   |                                                                                                                                                                                                | 1   | –   | V    |
| $I_{\text{CCDR}}$         | Data retention current               | $V_{\text{CC}} = 1.2\text{ V}$ , $\overline{\text{CE}} \geq V_{\text{CC}} - 0.2\text{ V}^{[14]}$ ,<br>$V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{ V}$ , or $V_{\text{IN}} \leq 0.2\text{ V}$ | –   | 8   | mA   |
| $t_{\text{CDR}}^{[15]}$   | Chip deselect to data retention time |                                                                                                                                                                                                | 0   | –   | ns   |
| $t_{\text{R}}^{[14, 15]}$ | Operation recovery time              | $V_{\text{CC}} \geq 2.2\text{ V}$                                                                                                                                                              | 10  | –   | ns   |
|                           |                                      | $V_{\text{CC}} < 2.2\text{ V}$                                                                                                                                                                 | 15  | –   | ns   |

## Data Retention Waveform

Figure 8. Data Retention Waveform <sup>[14]</sup>



### Notes

14. Full-device operation requires linear  $V_{\text{CC}}$  ramp from  $V_{\text{DR}}$  to  $V_{\text{CC(min)}}$   $\geq 100\text{ }\mu\text{s}$  or stable at  $V_{\text{CC(min)}}$   $\geq 100\text{ }\mu\text{s}$ .  
15. These parameters are guaranteed by design.

## AC Switching Characteristics

Over the operating range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

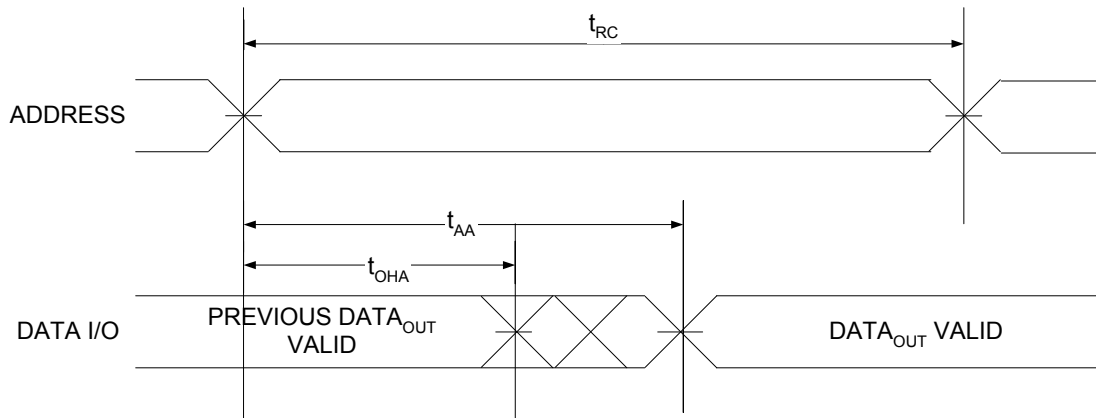
| Parameter <sup>[16]</sup>       | Description                                                  | 10 ns |     | 15 ns |     | Unit |
|---------------------------------|--------------------------------------------------------------|-------|-----|-------|-----|------|
|                                 |                                                              | Min   | Max | Min   | Max |      |
| Read Cycle                      |                                                              |       |     |       |     |      |
| t <sub>RC</sub>                 | Read cycle time                                              | 10    | –   | 15    | –   | ns   |
| t <sub>AA</sub>                 | Address to data / ERR valid                                  | –     | 10  | –     | 15  | ns   |
| t <sub>OHA</sub>                | Data / ERR hold from address change                          | 3     | –   | 3     | –   | ns   |
| t <sub>ACE</sub>                | $\overline{CE}$ LOW to data / ERR valid <sup>[17]</sup>      | –     | 10  | –     | 15  | ns   |
| t <sub>DOE</sub>                | $\overline{OE}$ LOW to data / ERR valid                      | –     | 4.5 | –     | 8   | ns   |
| t <sub>LZOE</sub>               | $\overline{OE}$ LOW to low impedance <sup>[18, 19]</sup>     | 0     | –   | 0     | –   | ns   |
| t <sub>HZOE</sub>               | $\overline{OE}$ HIGH to HI-Z <sup>[18, 19]</sup>             | –     | 5   | –     | 8   | ns   |
| t <sub>LZCE</sub>               | $\overline{CE}$ LOW to low impedance <sup>[17, 18, 19]</sup> | 3     | –   | 3     | –   | ns   |
| t <sub>HZCE</sub>               | $\overline{CE}$ HIGH to HI-Z <sup>[17, 18, 19]</sup>         | –     | 5   | –     | 8   | ns   |
| t <sub>PU</sub>                 | $\overline{CE}$ LOW to power-up <sup>[17, 19, 20]</sup>      | 0     | –   | 0     | –   | ns   |
| t <sub>PD</sub>                 | $\overline{CE}$ HIGH to power-down <sup>[17, 19, 20]</sup>   | –     | 10  | –     | 15  | ns   |
| t <sub>DBE</sub>                | Byte enable to data valid                                    | –     | 4.5 | –     | 8   | ns   |
| t <sub>LZBE</sub>               | Byte enable to low impedance <sup>[19]</sup>                 | 0     | –   | 0     | –   | ns   |
| t <sub>HZBE</sub>               | Byte disable to HI-Z <sup>[19]</sup>                         | –     | 6   | –     | 8   | ns   |
| Write Cycle <sup>[20, 21]</sup> |                                                              |       |     |       |     |      |
| t <sub>WC</sub>                 | Write cycle time                                             | 10    | –   | 15    | –   | ns   |
| t <sub>SCE</sub>                | $\overline{CE}$ LOW to write end <sup>[17]</sup>             | 7     | –   | 12    | –   | ns   |
| t <sub>AW</sub>                 | Address setup to write end                                   | 7     | –   | 12    | –   | ns   |
| t <sub>HA</sub>                 | Address hold from write end                                  | 0     | –   | 0     | –   | ns   |
| t <sub>SA</sub>                 | Address setup to write start                                 | 0     | –   | 0     | –   | ns   |
| t <sub>PWE</sub>                | $\overline{WE}$ pulse width                                  | 7     | –   | 12    | –   | ns   |
| t <sub>SD</sub>                 | Data setup to write end                                      | 5     | –   | 8     | –   | ns   |
| t <sub>HD</sub>                 | Data hold from write end                                     | 0     | –   | 0     | –   | ns   |
| t <sub>LZWE</sub>               | $\overline{WE}$ HIGH to low impedance <sup>[18, 19]</sup>    | 3     | –   | 3     | –   | ns   |
| t <sub>HZWE</sub>               | $\overline{WE}$ LOW to HI-Z <sup>[18, 19]</sup>              | –     | 5   | –     | 8   | ns   |
| t <sub>BW</sub>                 | Byte Enable to write end                                     | 7     | –   | 12    | –   | ns   |

### Notes

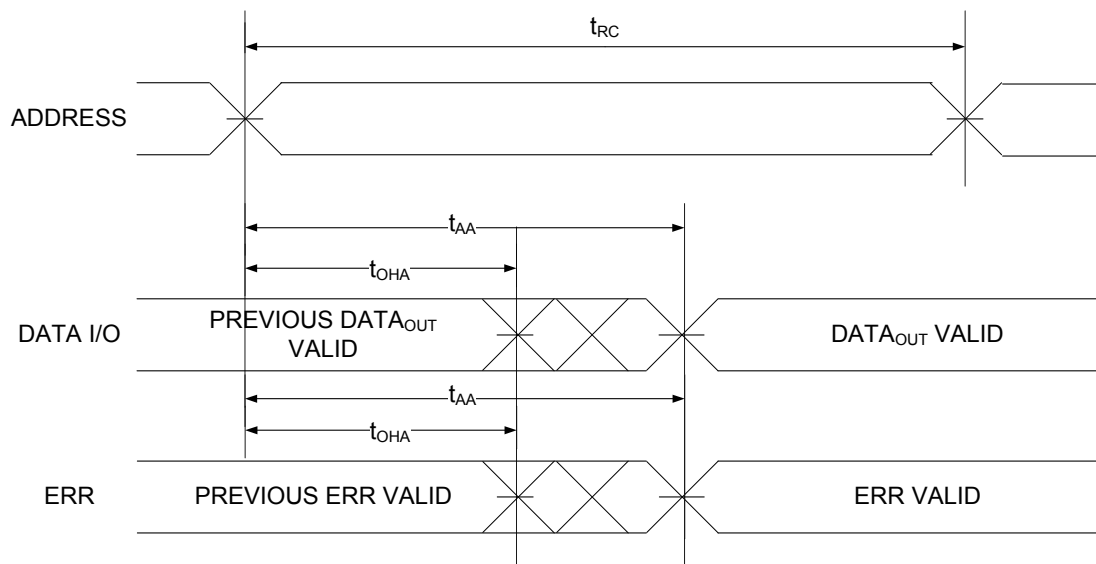
16. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3\text{ V}$ ) and  $V_{CC}/2$  (for  $V_{CC} < 3\text{ V}$ ), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3\text{ V}$ ) and 0 to  $V_{CC}$  (for  $V_{CC} < 3\text{ V}$ ). Test conditions for the read cycle use output loading, as shown in part (a) of Figure 7 on page 7, unless specified otherwise.
17. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
18.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ ,  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ , and  $t_{LZBE}$  are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 7 on page 7. Transition is measured  $\pm 200\text{ mV}$  from steady state voltage.
19. These parameters are guaranteed by design and are not tested.
20. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ , and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
21. The minimum write cycle pulse width in Write Cycle No 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

**Figure 9. Read Cycle No. 1 of CY7C1041G (Address Transition Controlled)** [22, 23]



**Figure 10. Read Cycle No. 1 of CY7C1041GE (Address Transition Controlled)** [22, 23]

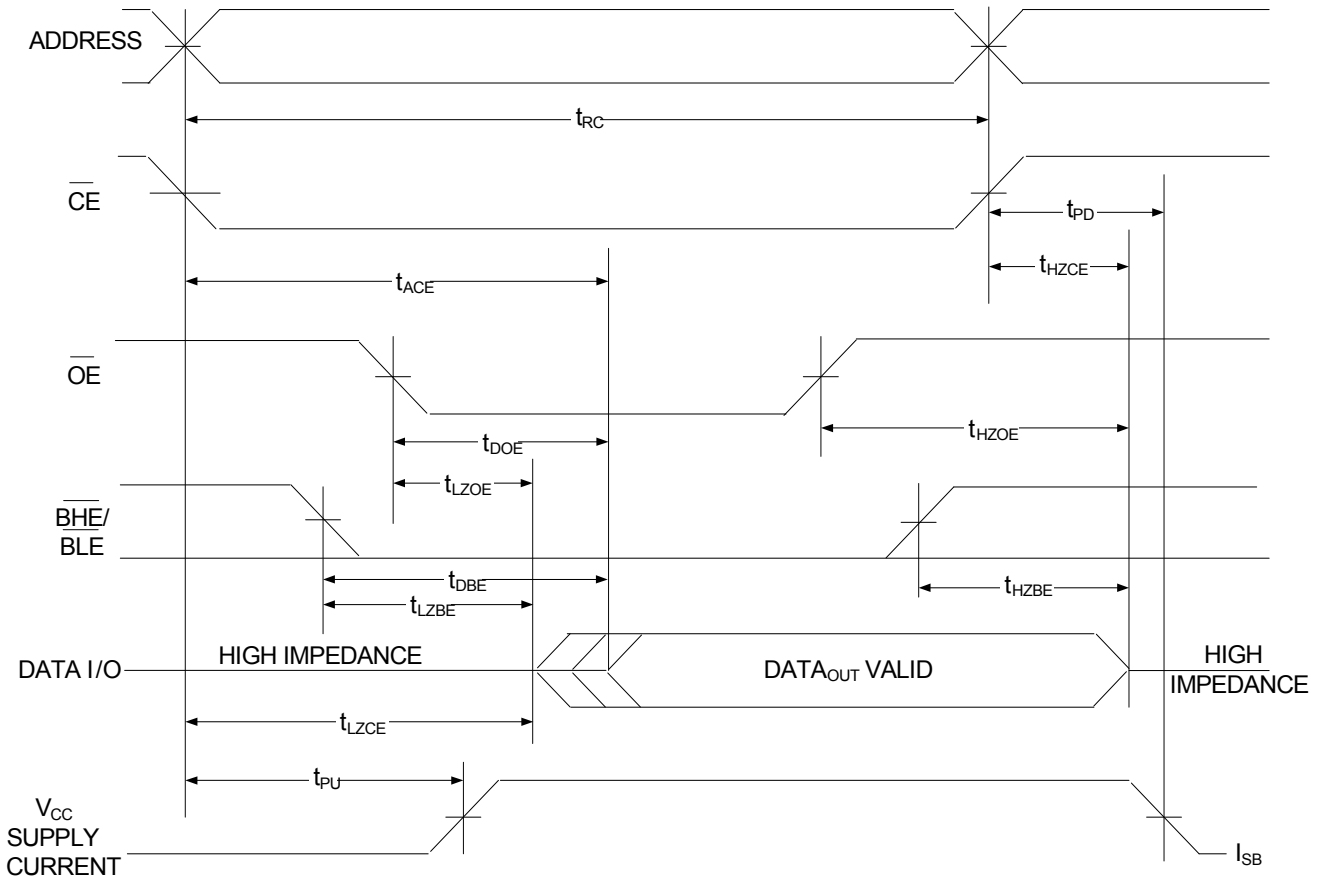


### Notes

22. The device is continuously selected,  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ .  
23.  $\overline{WE}$  is HIGH for the read cycle.

## Switching Waveforms (continued)

**Figure 11. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [24, 25, 26]

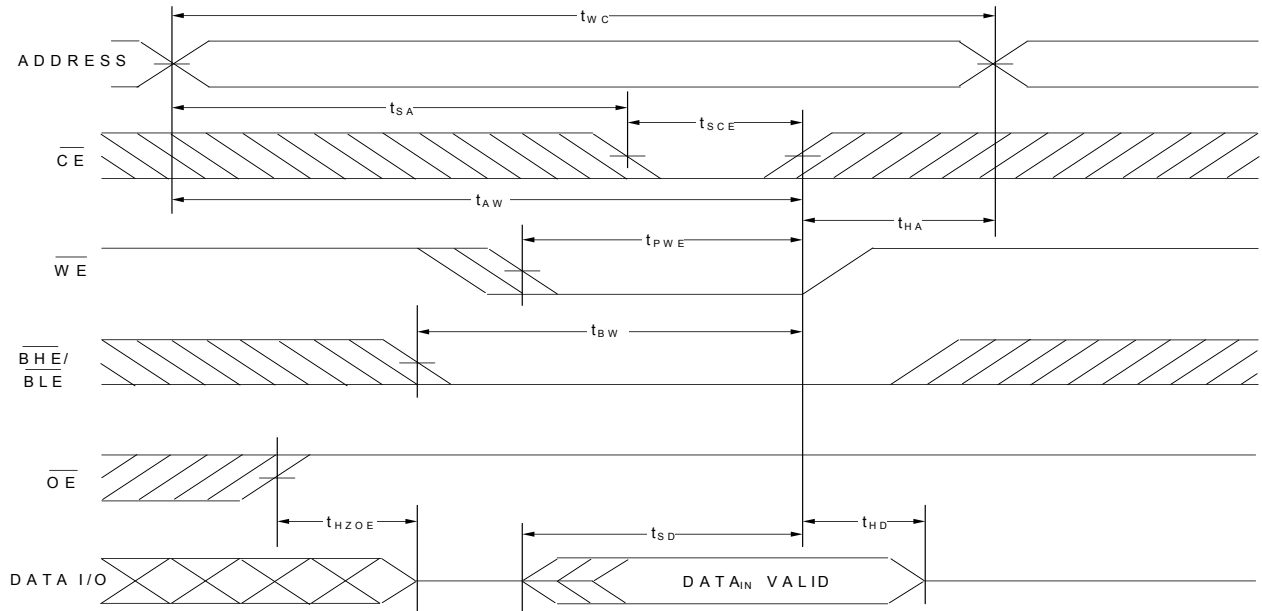


### Notes

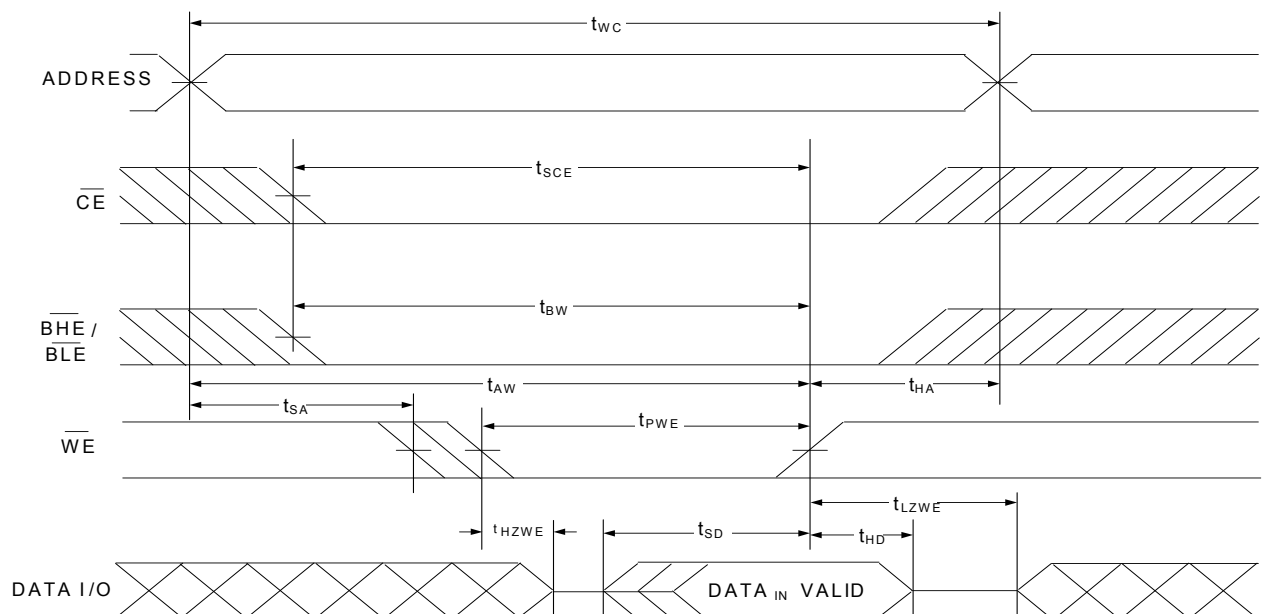
24. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
25.  $\overline{WE}$  is HIGH for the read cycle.
26. Address valid prior to or coincident with  $\overline{CE}$  LOW transition.

## Switching Waveforms (continued)

**Figure 12. Write Cycle No. 1 ( $\overline{CE}$  Controlled)** [27, 28, 29]



**Figure 13. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)** [27, 28, 29, 30]

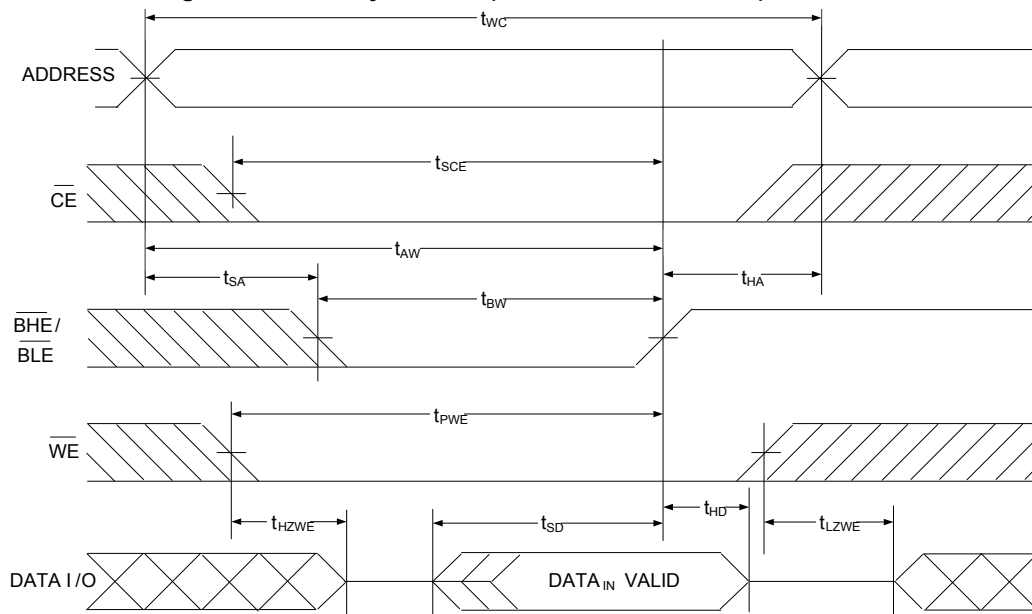


### Notes

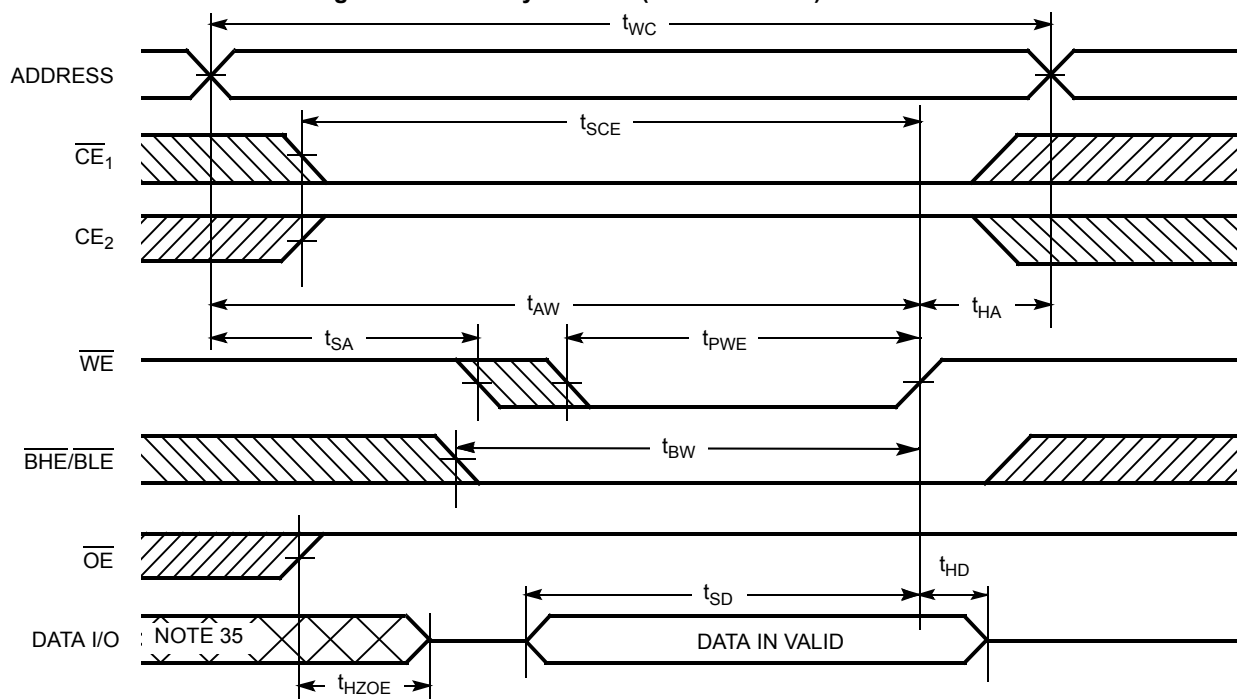
27. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
28. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ , and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
29. Data I/O is in HI-Z state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$ , or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .
30. The minimum write cycle pulse width should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms (continued)

**Figure 14. Write Cycle No. 3 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)** [31, 32, 33]



**Figure 15. Write Cycle No. 4 ( $\overline{\text{WE}}$  Controlled)** [31, 32, 33, 34]



### Notes

31. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
32. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ , and  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}} = V_{\text{IL}}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
33. Data I/O is in HI-Z state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$ , or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .
34. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
35. During this period the I/Os are in output state. Do not apply input signals.

## Truth Table

| $\overline{CE}^{[36]}$ | $\overline{OE}$   | $\overline{WE}$   | $\overline{BLE}$  | $\overline{BHE}$  | I/O <sub>0</sub> –I/O <sub>7</sub> | I/O <sub>8</sub> –I/O <sub>15</sub> | Mode                       | Power                      |
|------------------------|-------------------|-------------------|-------------------|-------------------|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| H                      | X <sup>[37]</sup> | X <sup>[37]</sup> | X <sup>[37]</sup> | X <sup>[37]</sup> | HI-Z                               | HI-Z                                | Power down                 | Standby (I <sub>SB</sub> ) |
| L                      | L                 | H                 | L                 | L                 | Data out                           | Data out                            | Read all bits              | Active (I <sub>CC</sub> )  |
| L                      | L                 | H                 | L                 | H                 | Data out                           | HI-Z                                | Read lower bits only       | Active (I <sub>CC</sub> )  |
| L                      | L                 | H                 | H                 | L                 | HI-Z                               | Data out                            | Read upper bits only       | Active (I <sub>CC</sub> )  |
| L                      | X                 | L                 | L                 | L                 | Data in                            | Data in                             | Write all bits             | Active (I <sub>CC</sub> )  |
| L                      | X                 | L                 | L                 | H                 | Data in                            | HI-Z                                | Write lower bits only      | Active (I <sub>CC</sub> )  |
| L                      | X                 | L                 | H                 | L                 | HI-Z                               | Data in                             | Write upper bits only      | Active (I <sub>CC</sub> )  |
| L                      | H                 | H                 | X                 | X                 | HI-Z                               | HI-Z                                | Selected, outputs disabled | Active (I <sub>CC</sub> )  |
| L                      | X                 | X                 | H                 | H                 | HI-Z                               | HI-Z                                | Selected, outputs disabled | Active (I <sub>CC</sub> )  |

## ERR Output – CY7C1041GE

| Output <sup>[38]</sup> | Mode                                                     |
|------------------------|----------------------------------------------------------|
| 0                      | Read operation, no single-bit error in the stored data.  |
| 1                      | Read operation, single-bit error detected and corrected. |
| HI-Z                   | Device deselected or outputs disabled or Write operation |

### Notes

36. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

37. The input voltage levels on these pins should be either at V<sub>IH</sub> or V<sub>IL</sub>.

38. ERR is an Output pin. If not used, this pin should be left floating

## Ordering Information

| Speed (ns) | Voltage Range | Ordering Code       | Package Diagram | Package Type (all Pb-free)                 | Operating Range |
|------------|---------------|---------------------|-----------------|--------------------------------------------|-----------------|
| 10         | 2.2 V–3.6 V   | CY7C1041GE30-10ZSXI | 51-85087        | 44-pin TSOP II, ERR output                 | Industrial      |
|            |               | CY7C1041G30-10ZSXI  | 51-85087        | 44-pin TSOP II                             |                 |
|            |               | CY7C1041GE30-10BVXI | 51-85150        | 48-ball VFBGA (6 × 8 × 1.0 mm), ERR output |                 |
|            |               | CY7C1041G30-10BVXI  | 51-85150        | 48-ball VFBGA (6 × 8 × 1.0 mm)             |                 |
|            |               | CY7C1041G30-10BVJXI | 51-85150        | 48-ball VFBGA (6 × 8 × 1.0 mm), JEDEC      |                 |
|            |               | CY7C1041G30-10VXI   | 51-85082        | 44-pin SOJ (400 Mils)                      |                 |
|            |               | CY7C1041GE30-10VXI  | 51-85082        | 44-pin SOJ (400 Mils), ERR output          |                 |
|            | 4.5 V–5.5 V   | CY7C1041G-10ZSXI    | 51-85087        | 44-pin TSOP II                             |                 |
|            |               | CY7C1041GE-10ZSXI   | 51-85087        | 44-pin TSOP II, ERR output                 |                 |
|            |               | CY7C1041GE-10VXI    | 51-85082        | 44-pin SOJ (400 Mils), ERR output          |                 |
|            |               | CY7C1041G-10VXI     | 51-85082        | 44-pin SOJ (400 Mils)                      |                 |
| 15         | 1.65 V–2.2 V  | CY7C1041G18-15ZSXI  | 51-85087        | 44-pin TSOP II                             | Industrial      |
|            |               | CY7C1041G18-15VXI   | 51-85082        | 44-pin SOJ (400 Mils)                      |                 |
|            |               | CY7C1041G18-15BVXI  | 51-85150        | 48-ball VFBGA (6 × 8 × 1.0 mm)             |                 |

## Ordering Code Definitions

|    |   |   |   |    |   |   |   |    |   |    |     |                                                                                                                                                                    |
|----|---|---|---|----|---|---|---|----|---|----|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CY | 7 | C | 1 | 04 | 1 | G | E | XX | - | XX | XXX | I                                                                                                                                                                  |
|    |   |   |   |    |   |   |   |    |   |    |     | Temperature Range: I = Industrial                                                                                                                                  |
|    |   |   |   |    |   |   |   |    |   |    |     | Pb-free Package Type: XXX = BVX or VX or ZSX or BVJX<br>BVX = 48-ball VFBGA; VX = 44-pin Molded SOJ;<br>ZSX = 44-pin TSOP II; BVJX = 48-ball VFBGA-JEDEC Compliant |
|    |   |   |   |    |   |   |   |    |   |    |     | Speed: XX = 10 ns or 15 ns                                                                                                                                         |
|    |   |   |   |    |   |   |   |    |   |    |     | Voltage Range:<br>18 = 1.65 V–2.2 V; 30 = 2.2 V–3.6 V; no character = 4.5 V–5.5 V                                                                                  |
|    |   |   |   |    |   |   |   |    |   |    |     | ERR output Single bit error indication                                                                                                                             |
|    |   |   |   |    |   |   |   |    |   |    |     | Revision Code "G": Process Technology – 65 nm                                                                                                                      |
|    |   |   |   |    |   |   |   |    |   |    |     | Data width: 1 = × 16-bits                                                                                                                                          |
|    |   |   |   |    |   |   |   |    |   |    |     | Density: 04 = 4-Mbit                                                                                                                                               |
|    |   |   |   |    |   |   |   |    |   |    |     | Family Code: 1 = Fast Asynchronous SRAM family                                                                                                                     |
|    |   |   |   |    |   |   |   |    |   |    |     | Technology Code: C = CMOS                                                                                                                                          |
|    |   |   |   |    |   |   |   |    |   |    |     | Marketing Code: 7 = SRAM                                                                                                                                           |
|    |   |   |   |    |   |   |   |    |   |    |     | Company ID: CY = Cypress                                                                                                                                           |

## Package Diagrams

Figure 16. 44-pin TSOP II (Z44) Package Outline, 51-85087

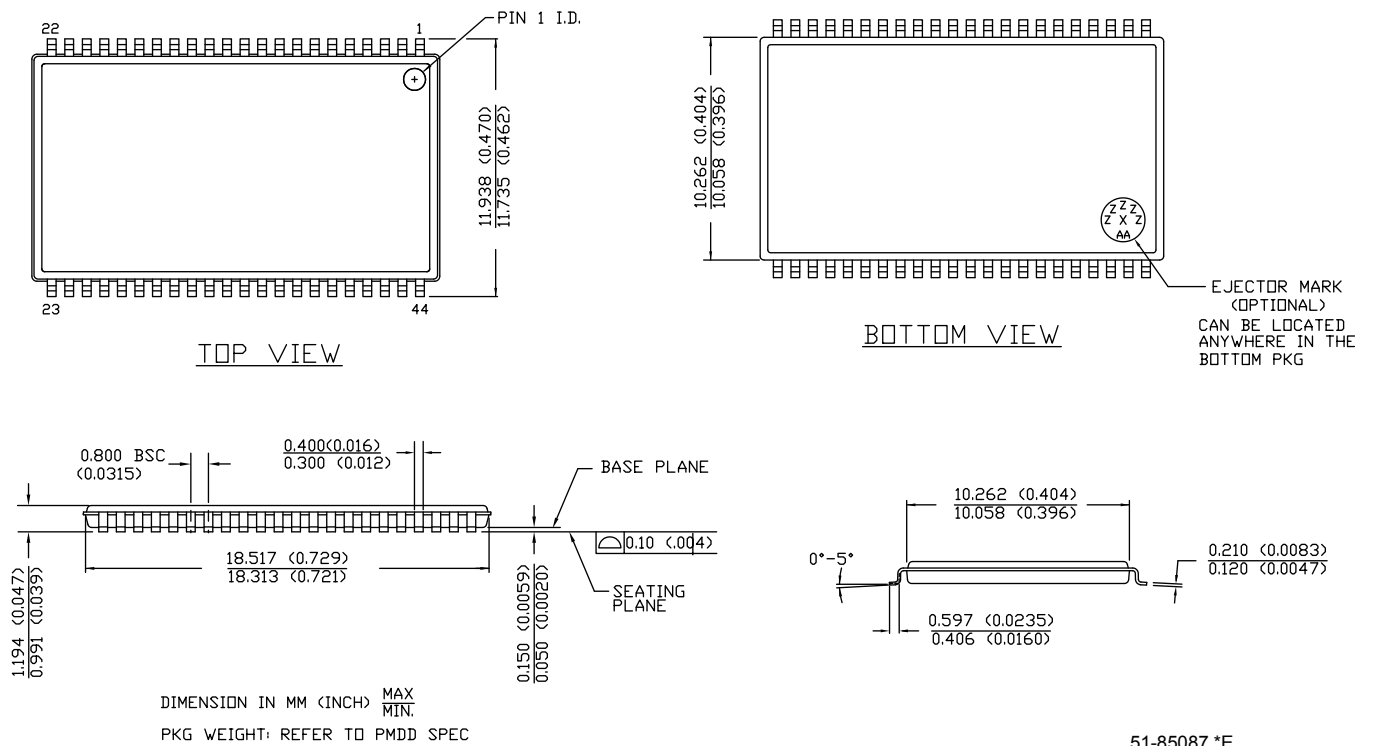
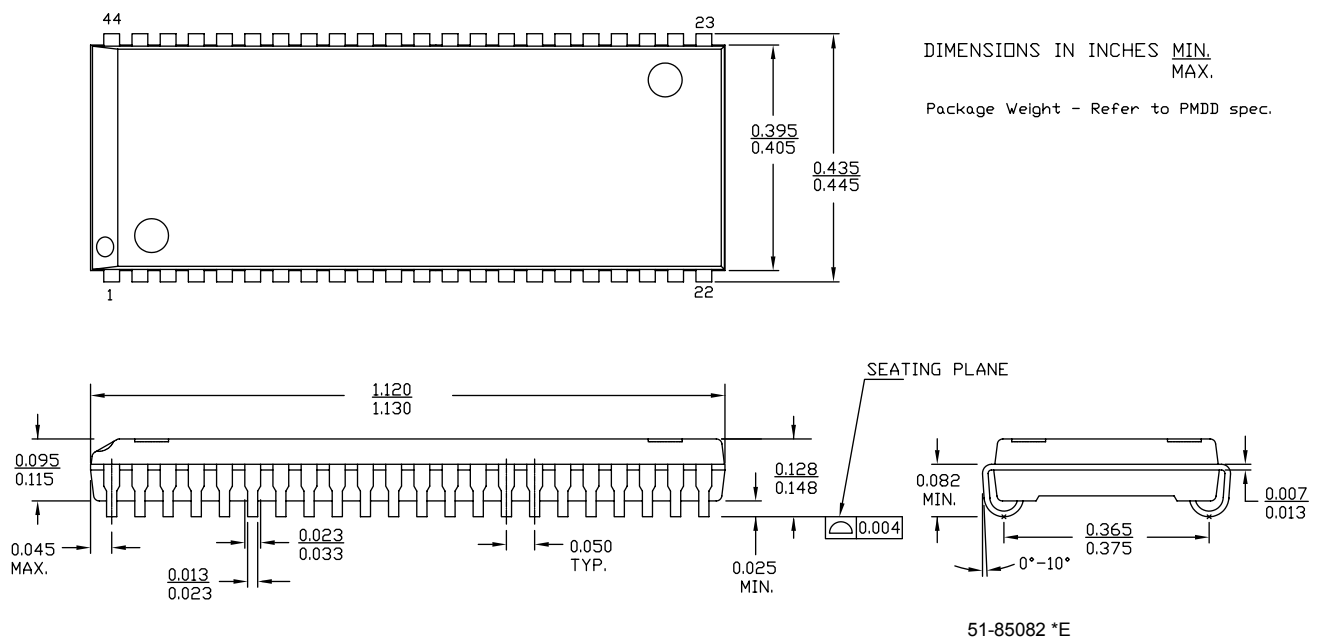
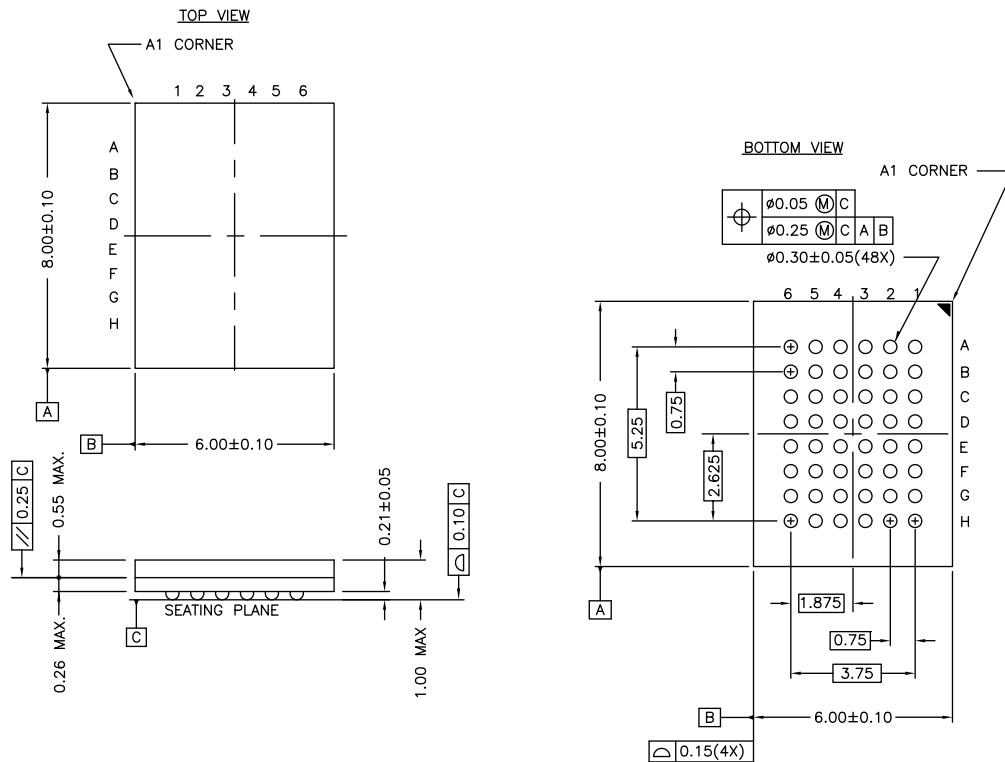


Figure 17. 44-pin SOJ (400 Mils) Package Outline, 51-85082



**Package Diagrams** (continued)

**Figure 18. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150**



NOTE:  
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)  
posted on the Cypress web.

51-85150 \*H

## Acronyms

| Acronym                 | Description                             |
|-------------------------|-----------------------------------------|
| $\overline{\text{BHE}}$ | byte high enable                        |
| $\overline{\text{BLE}}$ | byte low enable                         |
| $\overline{\text{CE}}$  | chip enable                             |
| CMOS                    | complementary metal oxide semiconductor |
| I/O                     | input/output                            |
| $\overline{\text{OE}}$  | output enable                           |
| SRAM                    | static random access memory             |
| TSOP                    | thin small outline package              |
| TTL                     | transistor-transistor logic             |
| VFBGA                   | very fine-pitch ball grid array         |
| $\overline{\text{WE}}$  | write enable                            |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | Degrees Celsius |
| MHz    | megahertz       |
| μA     | microamperes    |
| μs     | microseconds    |
| mA     | milliamperes    |
| mm     | millimeters     |
| ns     | nanoseconds     |
| Ω      | ohms            |
| %      | percent         |
| pF     | picofarads      |
| V      | volts           |
| W      | watts           |

## Document History Page

| Document Title: CY7C1041G/CY7C1041GE, 4-Mbit (256K words × 16 bit) Static RAM with Error-Correcting Code (ECC)<br>Document Number: 001-91368 |         |                 |                 |                                                                         |
|----------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|-------------------------------------------------------------------------|
| Rev.                                                                                                                                         | ECN No. | Orig. of Change | Submission Date | Description of Change                                                   |
| *F                                                                                                                                           | 4867081 | NILE            | 07/31/2015      | Changed status from Preliminary to Final.                               |
| *G                                                                                                                                           | 4876251 | NILE            | 08/07/2015      | Updated <a href="#">Ordering Information</a> :<br>Updated part numbers. |
| *H                                                                                                                                           | 4968879 | NILE            | 10/16/2015      | Fixed typo in bookmarks.                                                |
| *I                                                                                                                                           | 5019226 | VINI            | 11/18/2015      | Updated <a href="#">Ordering Information</a> :<br>Updated part numbers. |
| *J                                                                                                                                           | 5122043 | NILE            | 02/02/2016      | Updated <a href="#">Truth Table</a> .                                   |



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