CY62146GN MoBL®

4-Mbit (256K × 16) Static RAM

Features

- Very high speed: 45 ns
- Temperature ranges
  - Industrial: –40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V and 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 3.5 μA
  - Maximum standby current: 8.7 μA
- Ultra low active power
  - Typical active current: 3.5 mA at f = 1 MHz
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in a 44-pin TSOP II and 48-ball VFBGA Packages

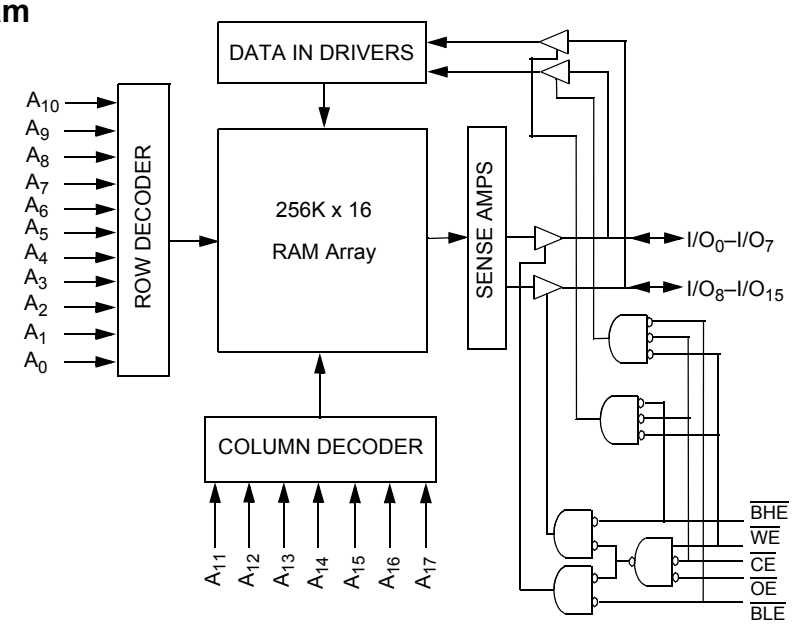
Functional Description

The CY62146GN is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features an advanced circuit design designed to provide an ultra low active current. Ultra low active current is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 80 percent when addresses are not toggling.The device can also be put into standby mode reducing power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation is in progress ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from the I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

Logic Block Diagram



Contents

Pin Configurations

Figure 1. 44-pin TSOP II pinout [1]

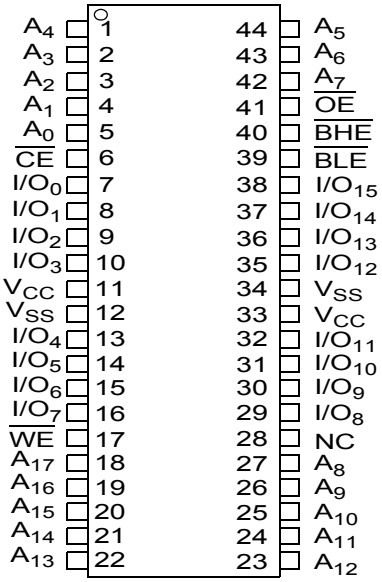
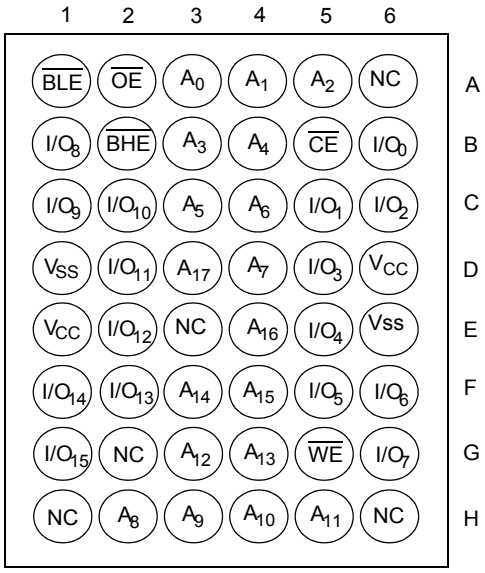


Figure 2. 48-ball VFBGA pinout [1]



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62146GN30	Industrial	2.2	3.0	3.6	45	3.5	6	15	20	3.5	8.7
CY62146GN		4.5	5.0	5.5	45						

Notes
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential ..... –0.3 V to + V_{CC} + 0.5 V

DC voltage applied to outputs in High-Z state [3, 4] ..... –0.3 V to + V_{CC} + 0.5 V

DC input voltage [3, 4] ..... –0.3 V to + V_{CC} + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001 V

Latch-up Current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [5]
CY62146GN30	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V, 4.5 V to 5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description		Test Conditions		45 ns			Unit
					Min	Typ [6]	Max	
V_{OH}	Output high voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –0.1 mA		2	–	–	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.2	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1 mA		V_{CC} – 0.5[7]	–	–	
V_{OL}	Output low voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.4	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
V_{IH}[4]	Input high voltage	2.2 V to 2.7 V	–		2.0	–	V_{CC} + 0.3	V
		2.7 V to 3.6 V	–		2.0	–	V_{CC} + 0.3	
		4.5 V to 5.5 V	–		2.2	–	V_{CC} + 0.5	
V_{IL}[3]	Input LOW Voltage	2.2 V to 2.7 V	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		2.7 V to 3.6 V	V_{CC} = 2.7 V to 3.6 V		–0.3	–	0.8	
		4.5 V to 5.5 V	–		–0.5	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_I ≤ V_{CC}		–1	–	+1	mA
I_{OZ}	Output leakage current		GND ≤ V_O ≤ V_{CC}, Output disabled		–1	–	+1	mA
I_{CC}	V_{CC} operating supply current		f = f_{max} = 1/t_{RC}	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	15	20	mA
			f = 1 MHz		–	3.5	6	
I_{SB1}	Automatic CE power down current – CMOS inputs		$\overline{CE}$ > V_{CC} – 0.2 V, V_{IN} > V_{CC} – 0.2 V or V_{IN} < 0.2 V, f = f_{max} (Address and data only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), V_{CC} = 3.60 V		–	3.5	8.7	µA
I_{SB2} [8]	Automatic CE power down current – CMOS inputs		$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = 3.60 V		–	3.5	8.7	µA

Notes

3. $V_{IL(min)}$ = –2.0 V for pulse durations less than 2 ns.
4. $V_{IH(max)}$ = V_{CC} + 2.0 V for pulse durations less than 2 ns.
5. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ > 100 µs or stable at $V_{CC(min)}$ > 100 µs.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
7. This parameter is guaranteed by design and not tested.
8. Chip enable ($\overline{CE}$) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

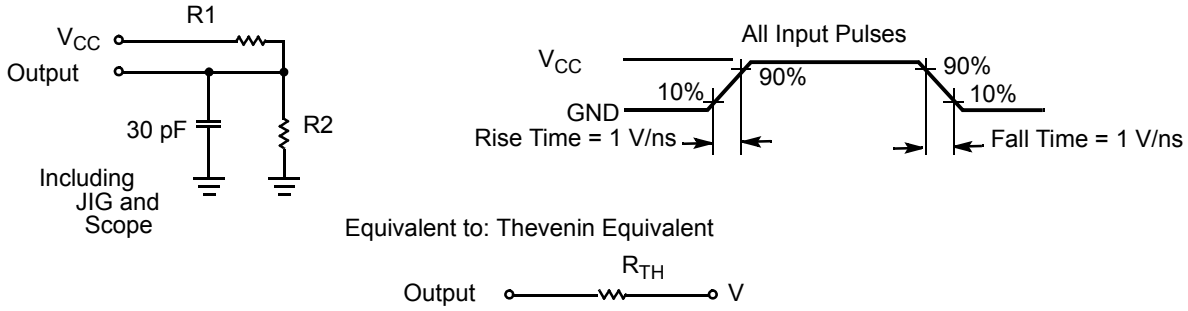
Parameter [9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [9]	Description	Test Conditions	TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	68.85	°C/W
Θ_{JC}	Thermal resistance (junction to case)		15.97	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [10]



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
9. Tested initially and after any design or process changes that may affect these parameters.
10. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ ≥ 100 µs or stable at $V_{CC(min)}$ ≥ 100 µs.

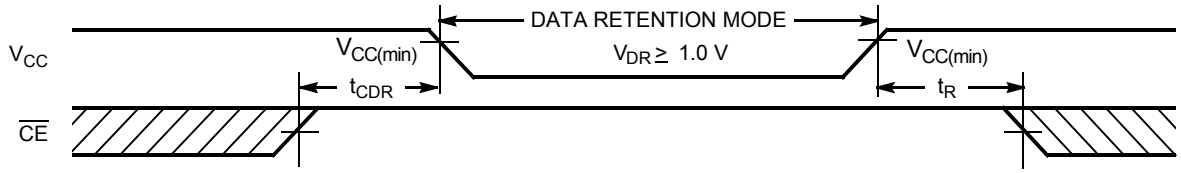
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR} [11, 12]	Data retention current	V_{CC} = 1.2 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	13	µA
t_{CDR} [13]	Chip deselect to data retention time	–	0	–	–	ns
t_R [14]	Operation recovery time	–	45	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

11. Chip enable (CE) needs to be tied to CMOS levels to meet the I_{SB1}/ I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR}.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ > 100 µs or stable at $V_{CC(min)}$ > 100 µs.

Switching Characteristics

Over the Operating Range

Parameter [15, 16]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z [17]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z [17, 18]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z [17]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z [17, 18]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	45	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z [17]	5	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z [17, 18]	–	18	ns
Write Cycle [19, 20]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z [17, 18]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z [17]	10	–	ns

Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 3 on page 5.
16. These parameters are guaranteed by design.
17. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
18. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write
20. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle 1 (Address Transition Controlled) [21, 22]

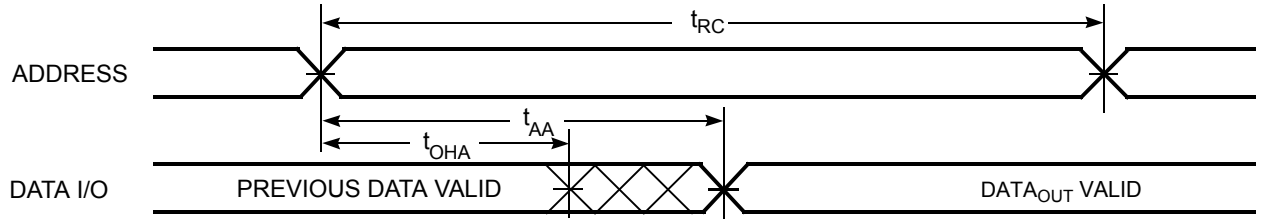
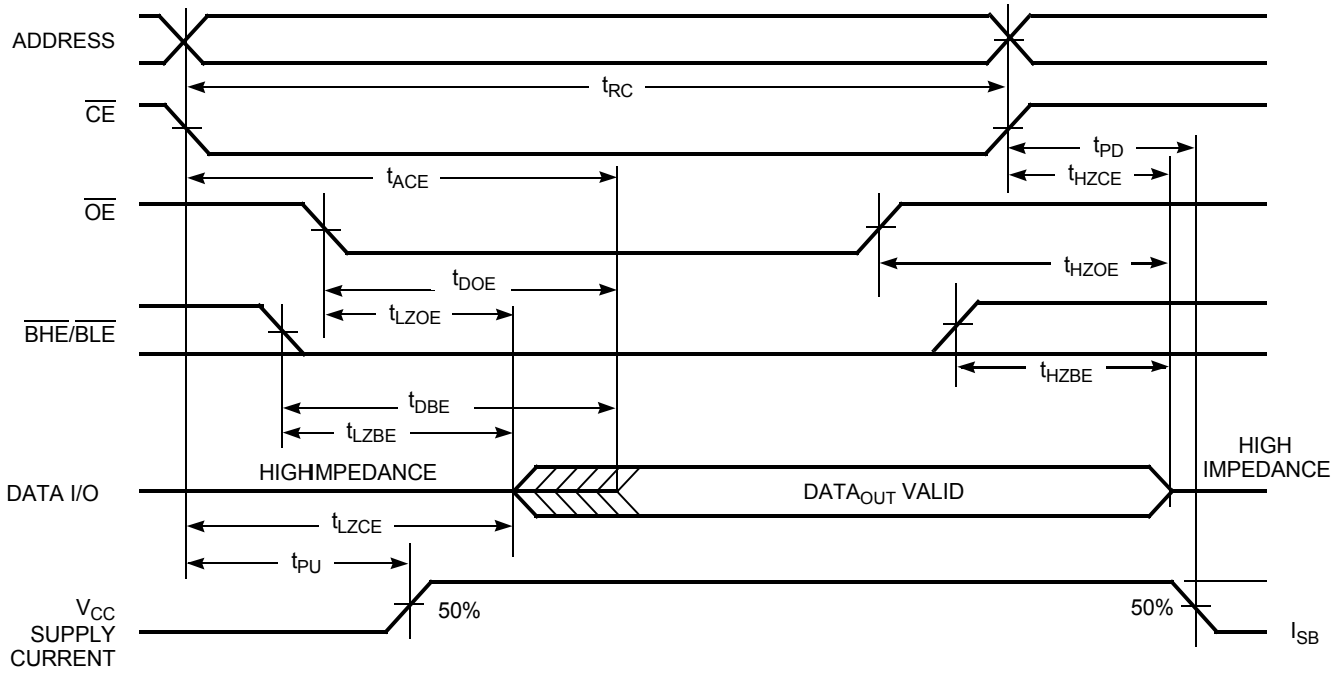


Figure 6. Read Cycle No. 2 (OE Controlled) [22, 23]



Notes
21. The device is continuously selected. OE, CE = V_{IL}, BHE and/or BLE = V_{IL}.
22. WE is HIGH for read cycle.
23. Address valid before or similar to CE.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 (WE Controlled) [24, 25, 26]

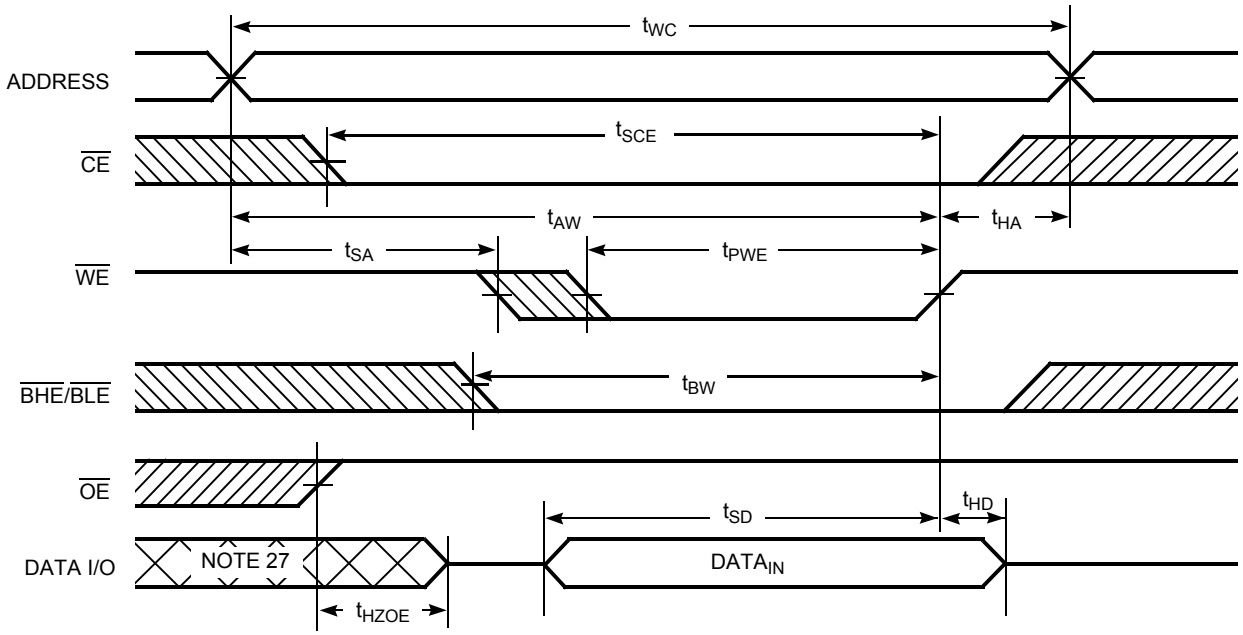
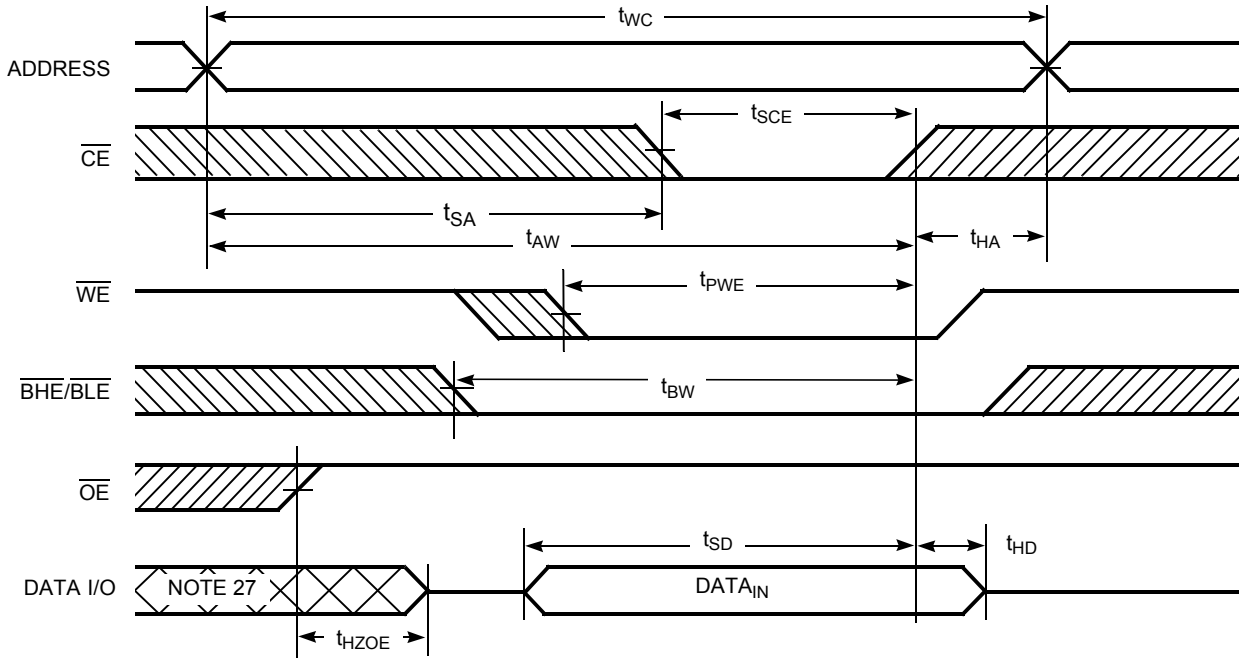


Figure 8. Write Cycle No. 2 (CE Controlled) [24, 25, 26]



Notes

24. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
25. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
26. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
27. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (WE Controlled, OE LOW) [28, 29]

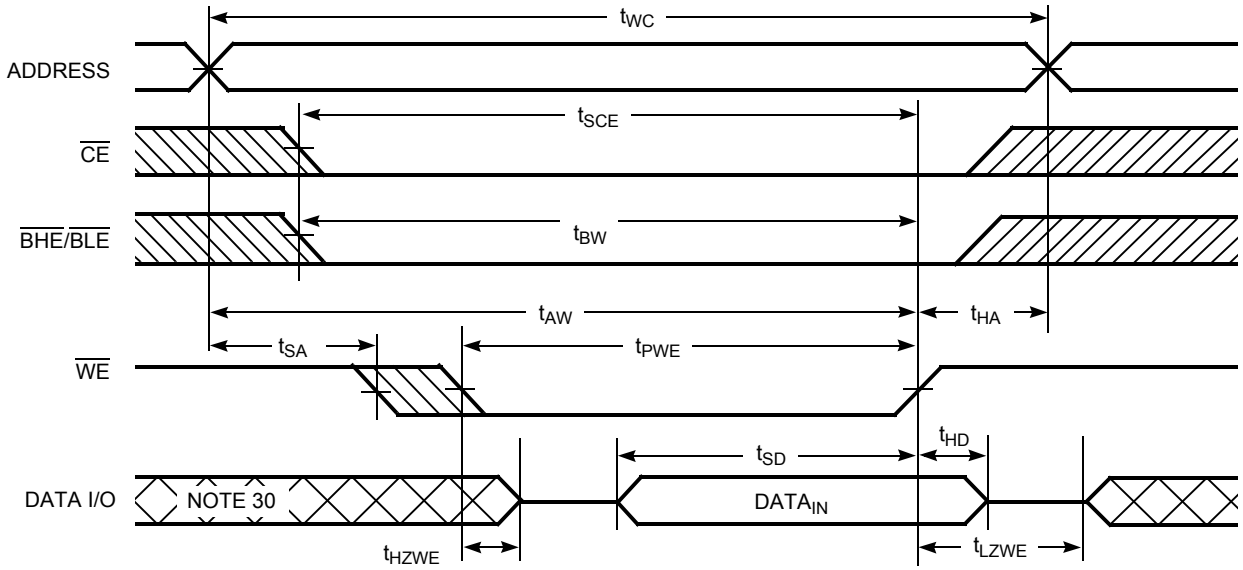
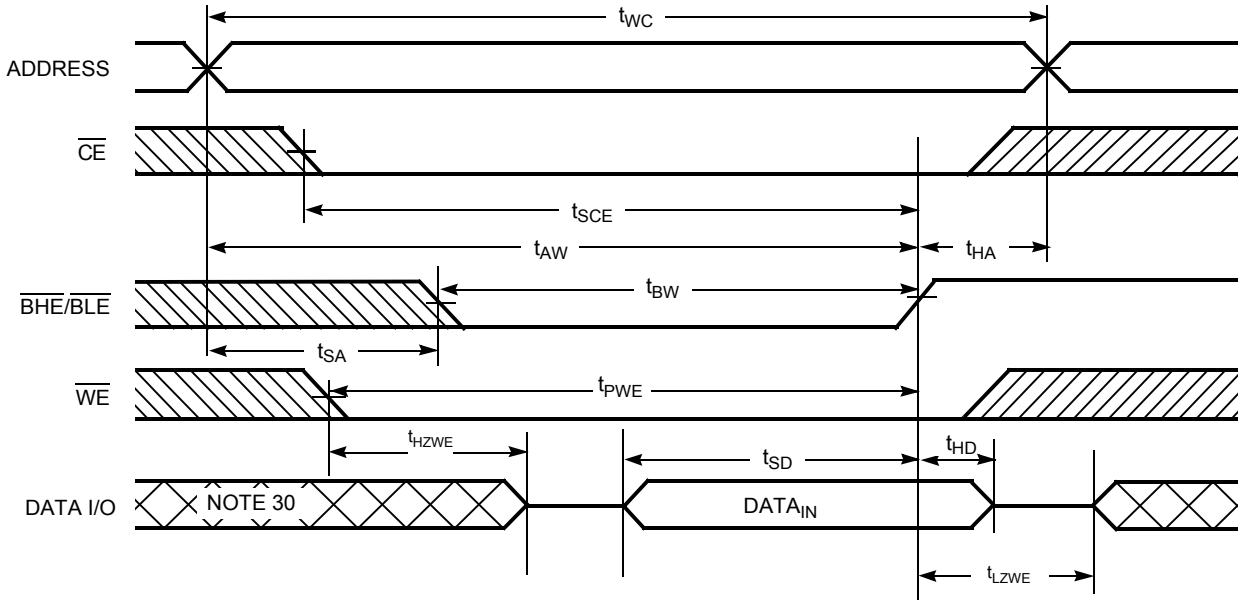


Figure 10. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [28]



Notes
28. If CE goes HIGH simultaneously with WE = V_{IH}, the output remains in a high impedance state.
29. The minimum write pulse width for Write Cycle No. 3 (WE Controlled, OE LOW) should be sum of t_{HZWE} and t_{SD}.
30. During this period, the I/Os are in output state and input signals must not be applied.

Truth Table

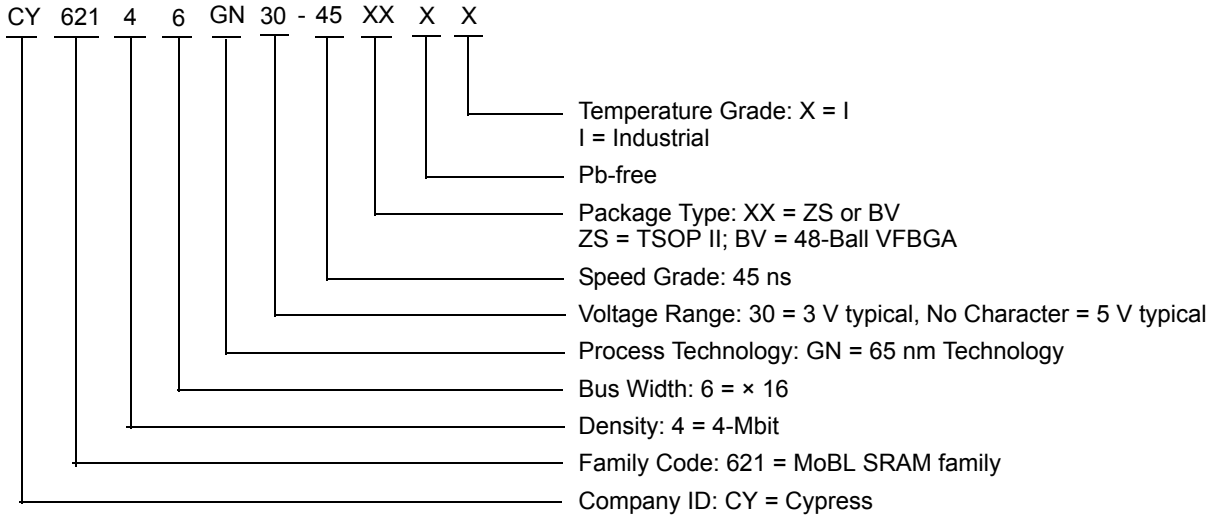
$\overline{CE}$ [31]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/power-down	Standby (I_{SB})
L	X	X	H	H	High-Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Read	Active (I_{CC})
L	H	H	X	X	High-Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Write	Active (I_{CC})

Note
31. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

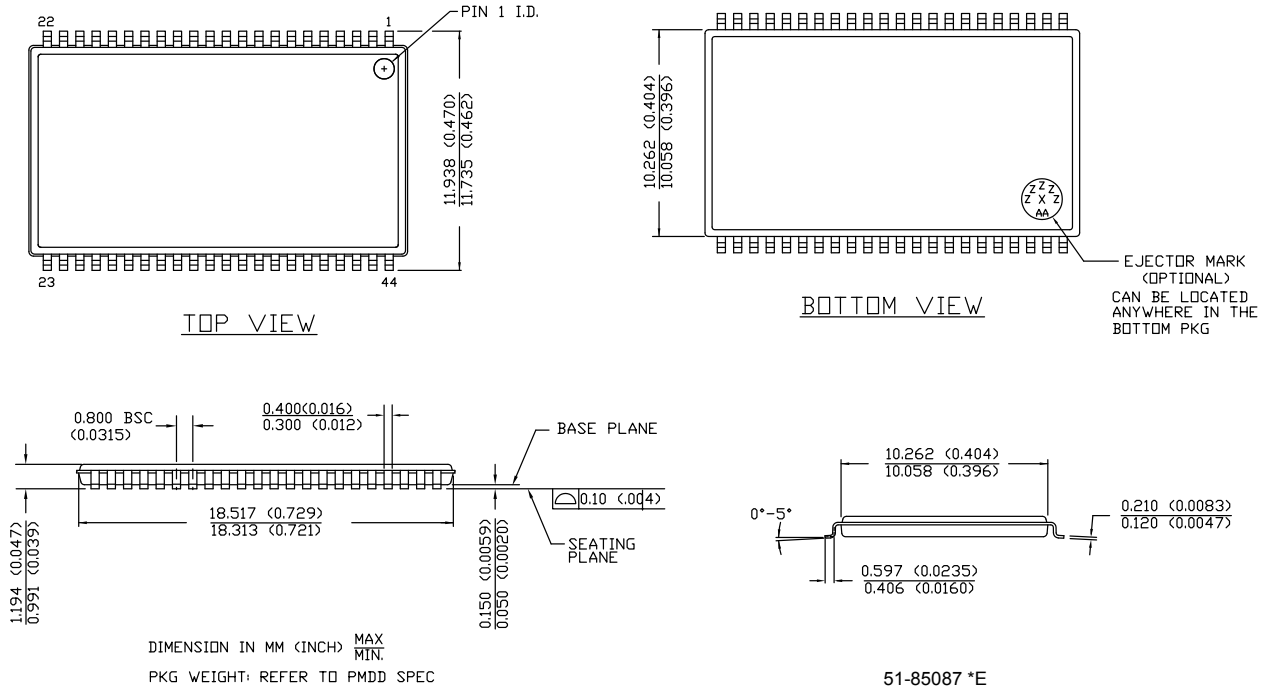
Speed (ns)	Voltage Range (V)	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62146GN30-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial
		CY62146GN30-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free)	
	4.5 V–5.5 V	CY62146GN-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	

Ordering Code Definitions



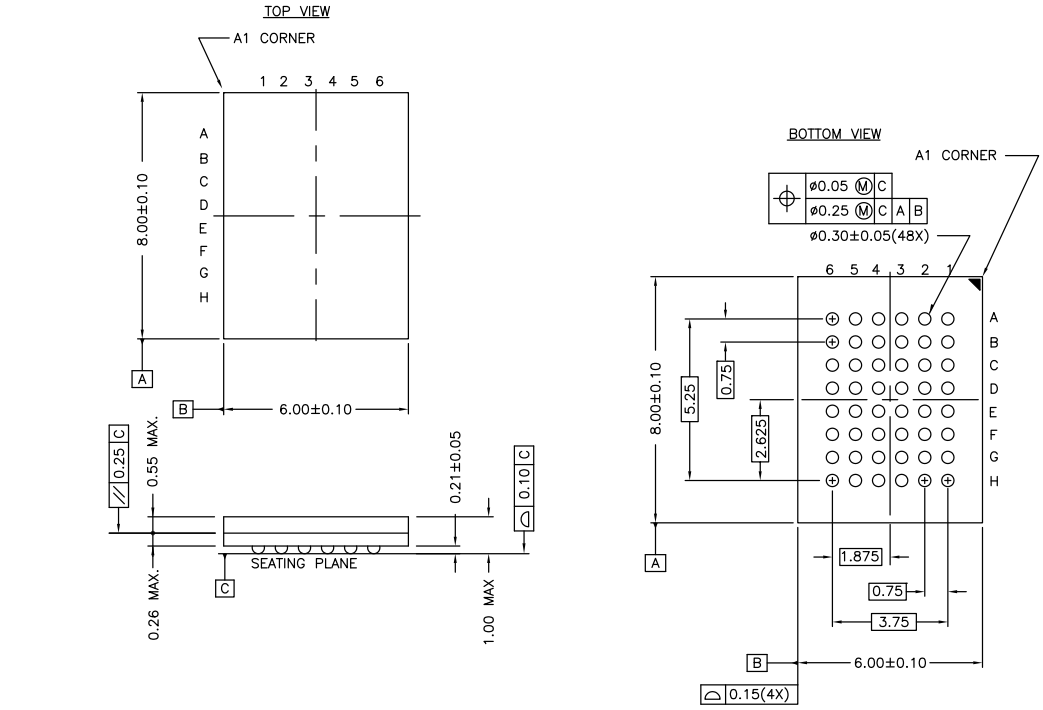
Package Diagrams

Figure 11. 44-pin TSOP Z44-II Package Outline, 51-85087



Package Diagrams (continued)

Figure 12. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{BHE}$	byte high enable
$\overline{BLE}$	byte low enable
CMOS	complementary metal oxide semiconductor
$\overline{CE}$	chip enable
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine-pitch ball grid array
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
µA	microamperes
mA	milliamperes
ns	nanoseconds
Ω	ohms
pF	picofarads
V	volts
W	watts

Document History Page

Document Title: CY62146GN MoBL®, 4-Mbit (256K × 16) Static RAM Document Number: 001-95417				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5048897	NILE	12/14/2015	New data sheet.
*A	5072822	NILE	01/05/2016	Added “4.5 V to 5.5 V” voltage range related information in all instances across the document. Updated Ordering Information: Updated part numbers.
*B	5092237	NILE	01/21/2016	Added 48-ball VFBGA package related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated Package Diagrams: Added spec 51-85150 *H (Figure 12).
*C	5142534	NILE	02/18/2016	Updated Ordering Code Definitions under Ordering Information (Replaced “GN = 90 nm” with “GN = 65 nm Technology”). Updated to new template.

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