

## Features

- Very high speed: 45 ns
- Temperature ranges
  - Industrial: -40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V and 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 3.5 μA
  - Maximum standby current: 8.7 μA
- Ultra low active power
  - Typical active current: 3.5 mA at f = 1 MHz
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in a 44-pin TSOP II and 48-ball VFBGA Packages

## Functional Description

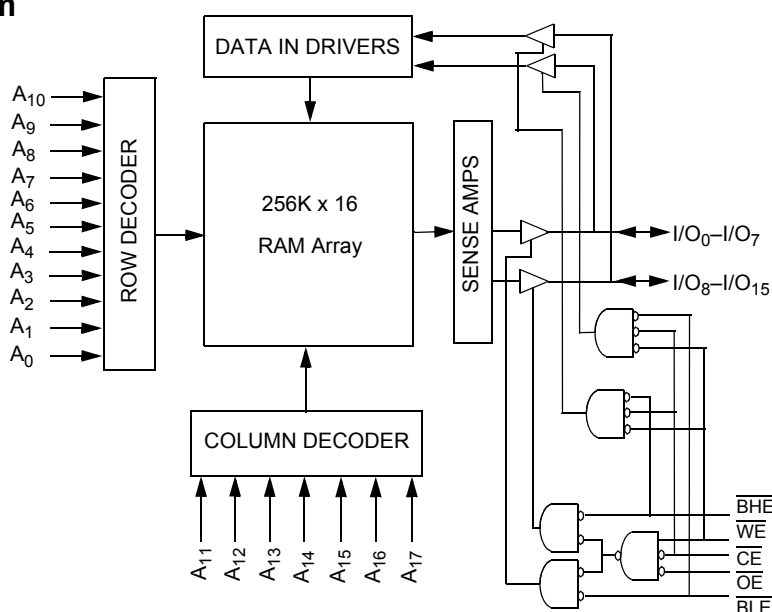
The CY62146GN is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features an advanced circuit design designed to provide an ultra low active current. Ultra low active current is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular

telephones. The device also has an automatic power down feature that significantly reduces power consumption by 80 percent when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99 percent when deselected (CE HIGH). The input and output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high impedance state when the device is deselected (CE HIGH), outputs are disabled (OE HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or a write operation is in progress (CE LOW and WE LOW).

To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). If Byte High Enable (BHE) is LOW, then data from the I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. See the [Truth Table on page 11](#) for a complete description of read and write modes.

## Logic Block Diagram



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## Pin Configurations

Figure 1. 44-pin TSOP II pinout <sup>[1]</sup>

|                  |    |    |                   |
|------------------|----|----|-------------------|
| A <sub>4</sub>   | 1  | 44 | A <sub>5</sub>    |
| A <sub>3</sub>   | 2  | 43 | A <sub>6</sub>    |
| A <sub>2</sub>   | 3  | 42 | A <sub>7</sub>    |
| A <sub>1</sub>   | 4  | 41 | OE                |
| A <sub>0</sub>   | 5  | 40 | BHE               |
| CE               | 6  | 39 | BLE               |
| I/O <sub>0</sub> | 7  | 38 | I/O <sub>15</sub> |
| I/O <sub>1</sub> | 8  | 37 | I/O <sub>14</sub> |
| I/O <sub>2</sub> | 9  | 36 | I/O <sub>13</sub> |
| I/O <sub>3</sub> | 10 | 35 | I/O <sub>12</sub> |
| V <sub>CC</sub>  | 11 | 34 | V <sub>SS</sub>   |
| V <sub>SS</sub>  | 12 | 33 | V <sub>CC</sub>   |
| I/O <sub>4</sub> | 13 | 32 | I/O <sub>11</sub> |
| I/O <sub>5</sub> | 14 | 31 | I/O <sub>10</sub> |
| I/O <sub>6</sub> | 15 | 30 | I/O <sub>9</sub>  |
| I/O <sub>7</sub> | 16 | 29 | I/O <sub>8</sub>  |
| WE               | 17 | 28 | NC                |
| A <sub>17</sub>  | 18 | 27 | A <sub>8</sub>    |
| A <sub>16</sub>  | 19 | 26 | A <sub>9</sub>    |
| A <sub>15</sub>  | 20 | 25 | A <sub>10</sub>   |
| A <sub>14</sub>  | 21 | 24 | A <sub>11</sub>   |
| A <sub>13</sub>  | 22 | 23 | A <sub>12</sub>   |

Figure 2. 48-ball VFBGA pinout <sup>[1]</sup>

|  | 1                 | 2                 | 3               | 4               | 5                | 6                |   |
|--|-------------------|-------------------|-----------------|-----------------|------------------|------------------|---|
|  | BLE               | OE                | A <sub>0</sub>  | A <sub>1</sub>  | A <sub>2</sub>   | NC               | A |
|  | I/O <sub>8</sub>  | BHE               | A <sub>3</sub>  | A <sub>4</sub>  | CE               | I/O <sub>0</sub> | B |
|  | I/O <sub>9</sub>  | I/O <sub>10</sub> | A <sub>5</sub>  | A <sub>6</sub>  | I/O <sub>1</sub> | I/O <sub>2</sub> | C |
|  | V <sub>SS</sub>   | I/O <sub>11</sub> | A <sub>17</sub> | A <sub>7</sub>  | I/O <sub>3</sub> | V <sub>CC</sub>  | D |
|  | V <sub>CC</sub>   | I/O <sub>12</sub> | NC              | A <sub>16</sub> | I/O <sub>4</sub> | V <sub>SS</sub>  | E |
|  | I/O <sub>14</sub> | I/O <sub>13</sub> | A <sub>14</sub> | A <sub>15</sub> | I/O <sub>5</sub> | I/O <sub>6</sub> | F |
|  | I/O <sub>15</sub> | NC                | A <sub>12</sub> | A <sub>13</sub> | WE               | I/O <sub>7</sub> | G |
|  | NC                | A <sub>8</sub>    | A <sub>9</sub>  | A <sub>10</sub> | A <sub>11</sub>  | NC               | H |

## Product Portfolio

| Product     | Range      | V <sub>CC</sub> Range (V) |                    |     | Speed (ns) | Power Dissipation              |     |                      |     |                               |     |
|-------------|------------|---------------------------|--------------------|-----|------------|--------------------------------|-----|----------------------|-----|-------------------------------|-----|
|             |            |                           |                    |     |            | Operating I <sub>CC</sub> (mA) |     |                      |     | Standby I <sub>SB2</sub> (μA) |     |
|             |            |                           |                    |     |            | f = 1 MHz                      |     | f = f <sub>max</sub> |     |                               |     |
|             |            | Min                       | Typ <sup>[2]</sup> | Max |            | Typ <sup>[2]</sup>             | Max | Typ <sup>[2]</sup>   | Max | Typ <sup>[2]</sup>            | Max |
| CY62146GN30 | Industrial | 2.2                       | 3.0                | 3.6 | 45         | 3.5                            | 6   | 15                   | 20  | 3.5                           | 8.7 |
| CY62146GN   |            | 4.5                       | 5.0                | 5.5 | 45         |                                |     |                      |     |                               |     |

### Notes

- NC pins are not connected on the die.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature  
with power applied ..... –55 °C to + 125 °C

Supply voltage  
to ground potential ..... –0.3 V to + V<sub>CC</sub> + 0.5 V

DC voltage applied to outputs  
in High-Z state <sup>[3, 4]</sup> ..... –0.3 V to + V<sub>CC</sub> + 0.5 V

DC input voltage <sup>[3, 4]</sup> ..... –0.3 V to + V<sub>CC</sub> + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static Discharge Voltage  
(per MIL-STD-883, Method 3015) ..... >2001 V

Latch-up Current ..... >200 mA

## Operating Range

| Device      | Range      | Ambient Temperature | V <sub>CC</sub> <sup>[5]</sup>    |
|-------------|------------|---------------------|-----------------------------------|
| CY62146GN30 | Industrial | –40 °C to +85 °C    | 2.2 V to 3.6 V,<br>4.5 V to 5.5 V |

## Electrical Characteristics

Over the Operating Range

| Parameter                       | Description                                   | Test Conditions                                                                                                                                                                                            | 45 ns                                |                    |                       | Unit |
|---------------------------------|-----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|--------------------|-----------------------|------|
|                                 |                                               |                                                                                                                                                                                                            | Min                                  | Typ <sup>[6]</sup> | Max                   |      |
| V <sub>OH</sub>                 | Output high voltage                           | 2.2 V to 2.7 V V <sub>CC</sub> = Min, I <sub>OH</sub> = –0.1 mA                                                                                                                                            | 2                                    | –                  | –                     | V    |
|                                 |                                               | 2.7 V to 3.6 V V <sub>CC</sub> = Min, I <sub>OH</sub> = –1.0 mA                                                                                                                                            | 2.2                                  | –                  | –                     |      |
|                                 |                                               | 4.5 V to 5.5 V V <sub>CC</sub> = Min, I <sub>OH</sub> = –1.0 mA                                                                                                                                            | 2.4                                  | –                  | –                     |      |
|                                 |                                               | 4.5 V to 5.5 V V <sub>CC</sub> = Min, I <sub>OH</sub> = –0.1 mA                                                                                                                                            | V <sub>CC</sub> – 0.5 <sup>[7]</sup> | –                  | –                     |      |
| V <sub>OL</sub>                 | Output low voltage                            | 2.2 V to 2.7 V V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA                                                                                                                                             | –                                    | –                  | 0.4                   | V    |
|                                 |                                               | 2.7 V to 3.6 V V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA                                                                                                                                             | –                                    | –                  | 0.4                   |      |
|                                 |                                               | 4.5 V to 5.5 V V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA                                                                                                                                             | –                                    | –                  | 0.4                   |      |
| V <sub>IH</sub> <sup>[4]</sup>  | Input high voltage                            | 2.2 V to 2.7 V –                                                                                                                                                                                           | 2.0                                  | –                  | V <sub>CC</sub> + 0.3 | V    |
|                                 |                                               | 2.7 V to 3.6 V –                                                                                                                                                                                           | 2.0                                  | –                  | V <sub>CC</sub> + 0.3 |      |
|                                 |                                               | 4.5 V to 5.5 V –                                                                                                                                                                                           | 2.2                                  | –                  | V <sub>CC</sub> + 0.5 |      |
| V <sub>IL</sub> <sup>[3]</sup>  | Input LOW Voltage                             | 2.2 V to 2.7 V V <sub>CC</sub> = 2.2 V to 2.7 V                                                                                                                                                            | –0.3                                 | –                  | 0.6                   | V    |
|                                 |                                               | 2.7 V to 3.6 V V <sub>CC</sub> = 2.7 V to 3.6 V                                                                                                                                                            | –0.3                                 | –                  | 0.8                   |      |
|                                 |                                               | 4.5 V to 5.5 V –                                                                                                                                                                                           | –0.5                                 | –                  | 0.8                   |      |
| I <sub>IX</sub>                 | Input leakage current                         | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>                                                                                                                                                                     | –1                                   | –                  | +1                    | mA   |
| I <sub>OZ</sub>                 | Output leakage current                        | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output disabled                                                                                                                                                   | –1                                   | –                  | +1                    | mA   |
| I <sub>CC</sub>                 | V <sub>CC</sub> operating supply current      | f = f <sub>max</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = V <sub>CC(max)</sub> , I <sub>OUT</sub> = 0 mA                                                                                                  | –                                    | 15                 | 20                    | mA   |
|                                 |                                               | f = 1 MHz CMOS levels                                                                                                                                                                                      | –                                    | 3.5                | 6                     |      |
| I <sub>SB1</sub>                | Automatic CE power down current – CMOS inputs | CE > V <sub>CC</sub> – 0.2 V, V <sub>IN</sub> > V <sub>CC</sub> – 0.2 V or V <sub>IN</sub> < 0.2 V, f = f <sub>max</sub> (Address and data only),<br>f = 0 (OE, BHE, BLE and WE), V <sub>CC</sub> = 3.60 V | –                                    | 3.5                | 8.7                   | μA   |
| I <sub>SB2</sub> <sup>[8]</sup> | Automatic CE power down current – CMOS inputs | CE ≥ V <sub>CC</sub> – 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0, V <sub>CC</sub> = 3.60 V                                                                        | –                                    | 3.5                | 8.7                   | μA   |

### Notes

3. V<sub>IL(min)</sub> = –2.0 V for pulse durations less than 2 ns.

4. V<sub>IH(max)</sub> = V<sub>CC</sub> + 2.0 V for pulse durations less than 2 ns.

5. Full-device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> > 100 μs or stable at V<sub>CC(min)</sub> > 100 μs.

6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

7. This parameter is guaranteed by design and not tested.

8. Chip enable (CE) need to be tied to CMOS levels to meet the I<sub>SB1</sub> / I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

## Capacitance

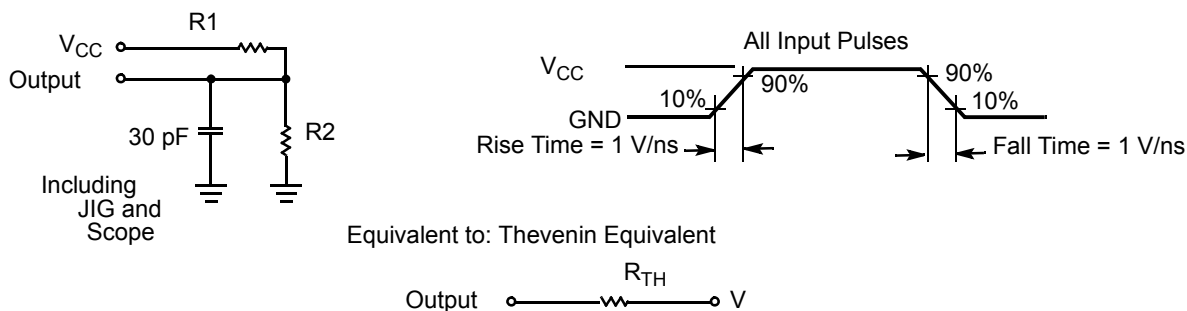
| Parameter <sup>[9]</sup> | Description        | Test Conditions                                                                         | Max | Unit |
|--------------------------|--------------------|-----------------------------------------------------------------------------------------|-----|------|
| $C_{IN}$                 | Input capacitance  | $T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(\text{typ})}$ | 10  | pF   |
| $C_{OUT}$                | Output capacitance |                                                                                         | 10  | pF   |

## Thermal Resistance

| Parameter <sup>[9]</sup> | Description                              | Test Conditions                                                         | TSOP II | Unit                 |
|--------------------------|------------------------------------------|-------------------------------------------------------------------------|---------|----------------------|
| $\Theta_{JA}$            | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 68.85   | $^{\circ}\text{C/W}$ |
| $\Theta_{JC}$            | Thermal resistance (junction to case)    |                                                                         | 15.97   | $^{\circ}\text{C/W}$ |

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms <sup>[10]</sup>



| Parameters | 2.50 V | 3.0 V | Unit     |
|------------|--------|-------|----------|
| R1         | 16667  | 1103  | $\Omega$ |
| R2         | 15385  | 1554  | $\Omega$ |
| $R_{TH}$   | 8000   | 645   | $\Omega$ |
| $V_{TH}$   | 1.20   | 1.75  | V        |

### Note

9. Tested initially and after any design or process changes that may affect these parameters.
10. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ .

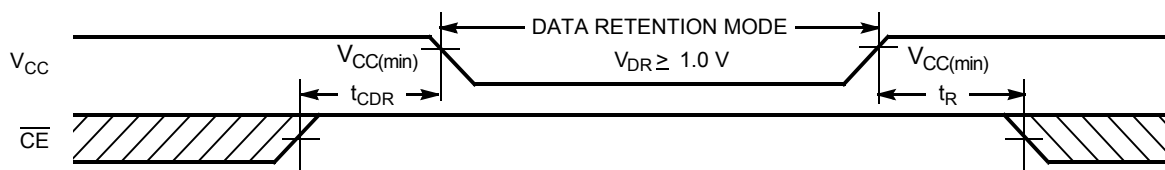
## Data Retention Characteristics

Over the Operating Range

| Parameter             | Description                          | Conditions                                                                                                                                  | Min | Typ | Max | Unit          |
|-----------------------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| $V_{DR}$              | $V_{CC}$ for data retention          |                                                                                                                                             | 1.0 | –   | –   | V             |
| $I_{CCDR}^{[11, 12]}$ | Data retention current               | $V_{CC} = 1.2\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | –   | –   | 13  | $\mu\text{A}$ |
| $t_{CDR}^{[13]}$      | Chip deselect to data retention time | –                                                                                                                                           | 0   | –   | –   | ns            |
| $t_R^{[14]}$          | Operation recovery time              | –                                                                                                                                           | 45  | –   | –   | ns            |

## Data Retention Waveform

Figure 4. Data Retention Waveform



### Notes

11. Chip enable (CE) needs to be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
12.  $I_{CCDR}$  is guaranteed only after device is first powered up to  $V_{CC(min)}$  and then brought down to  $V_{DR}$ .
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)}$  > 100  $\mu\text{s}$  or stable at  $V_{CC(min)}$  > 100  $\mu\text{s}$ .

## Switching Characteristics

Over the Operating Range

| Parameter <sup>[15, 16]</sup>   | Description                                                            | 45 ns |     | Unit |
|---------------------------------|------------------------------------------------------------------------|-------|-----|------|
|                                 |                                                                        | Min   | Max |      |
| Read Cycle                      |                                                                        |       |     |      |
| t <sub>RC</sub>                 | Read cycle time                                                        | 45    | –   | ns   |
| t <sub>AA</sub>                 | Address to data valid                                                  | –     | 45  | ns   |
| t <sub>OHA</sub>                | Data hold from address change                                          | 10    | –   | ns   |
| t <sub>ACE</sub>                | $\overline{CE}$ LOW to data valid                                      | –     | 45  | ns   |
| t <sub>DOE</sub>                | $\overline{OE}$ LOW to data valid                                      | –     | 22  | ns   |
| t <sub>LZOE</sub>               | $\overline{OE}$ LOW to Low-Z <sup>[17]</sup>                           | 5     | –   | ns   |
| t <sub>HZOE</sub>               | $\overline{OE}$ HIGH to High-Z <sup>[17, 18]</sup>                     | –     | 18  | ns   |
| t <sub>LZCE</sub>               | $\overline{CE}$ LOW to Low-Z <sup>[17]</sup>                           | 10    | –   | ns   |
| t <sub>HZCE</sub>               | $\overline{CE}$ HIGH to High-Z <sup>[17, 18]</sup>                     | –     | 18  | ns   |
| t <sub>PU</sub>                 | $\overline{CE}$ LOW to power up                                        | 0     | –   | ns   |
| t <sub>PD</sub>                 | $\overline{CE}$ HIGH to power down                                     | –     | 45  | ns   |
| t <sub>DBE</sub>                | $\overline{BLE}$ / $\overline{BHE}$ LOW to data valid                  | –     | 22  | ns   |
| t <sub>LZBE</sub>               | $\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z <sup>[17]</sup>       | 5     | –   | ns   |
| t <sub>HZBE</sub>               | $\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z <sup>[17, 18]</sup> | –     | 18  | ns   |
| Write Cycle <sup>[19, 20]</sup> |                                                                        |       |     |      |
| t <sub>WC</sub>                 | Write cycle time                                                       | 45    | –   | ns   |
| t <sub>SCE</sub>                | $\overline{CE}$ LOW to write end                                       | 35    | –   | ns   |
| t <sub>AW</sub>                 | Address setup to write end                                             | 35    | –   | ns   |
| t <sub>HA</sub>                 | Address hold from write end                                            | 0     | –   | ns   |
| t <sub>SA</sub>                 | Address setup to write start                                           | 0     | –   | ns   |
| t <sub>PWE</sub>                | $\overline{WE}$ pulse width                                            | 35    | –   | ns   |
| t <sub>BW</sub>                 | $\overline{BLE}$ / $\overline{BHE}$ LOW to write end                   | 35    | –   | ns   |
| t <sub>SD</sub>                 | Data setup to write end                                                | 25    | –   | ns   |
| t <sub>HD</sub>                 | Data hold from write end                                               | 0     | –   | ns   |
| t <sub>HZWE</sub>               | $\overline{WE}$ LOW to High-Z <sup>[17, 18]</sup>                      | –     | 18  | ns   |
| t <sub>LZWE</sub>               | $\overline{WE}$ HIGH to Low-Z <sup>[17]</sup>                          | 10    | –   | ns   |

### Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [Figure 3 on page 5](#).

16. These parameters are guaranteed by design.

17. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.

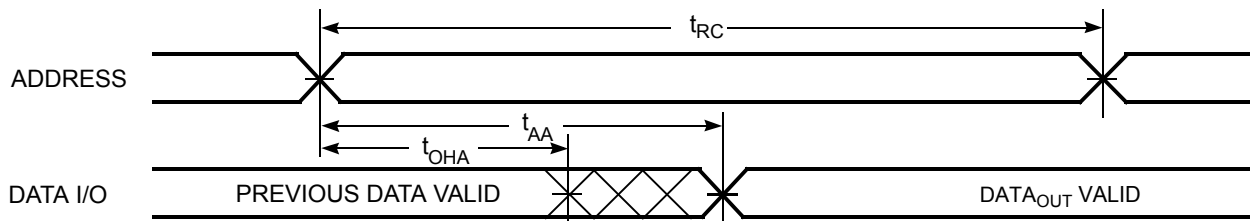
18.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.

19. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

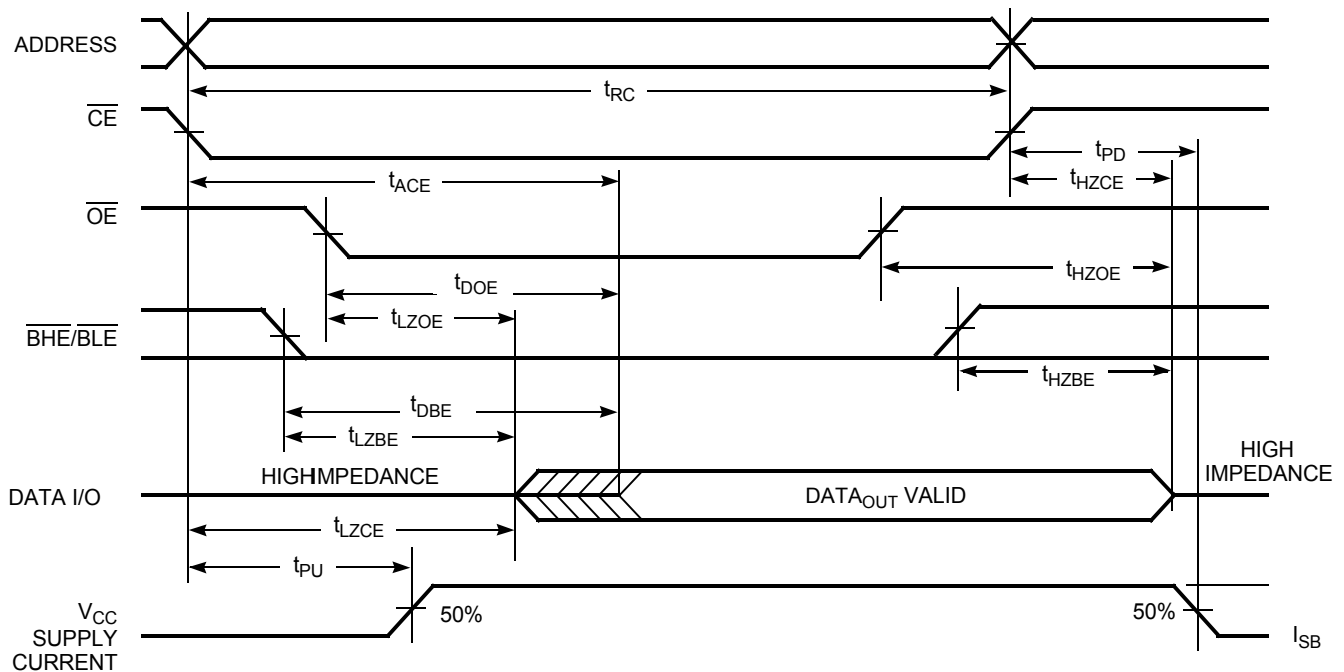
20. The minimum write pulse width for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

**Figure 5. Read Cycle 1 (Address Transition Controlled)** [21, 22]



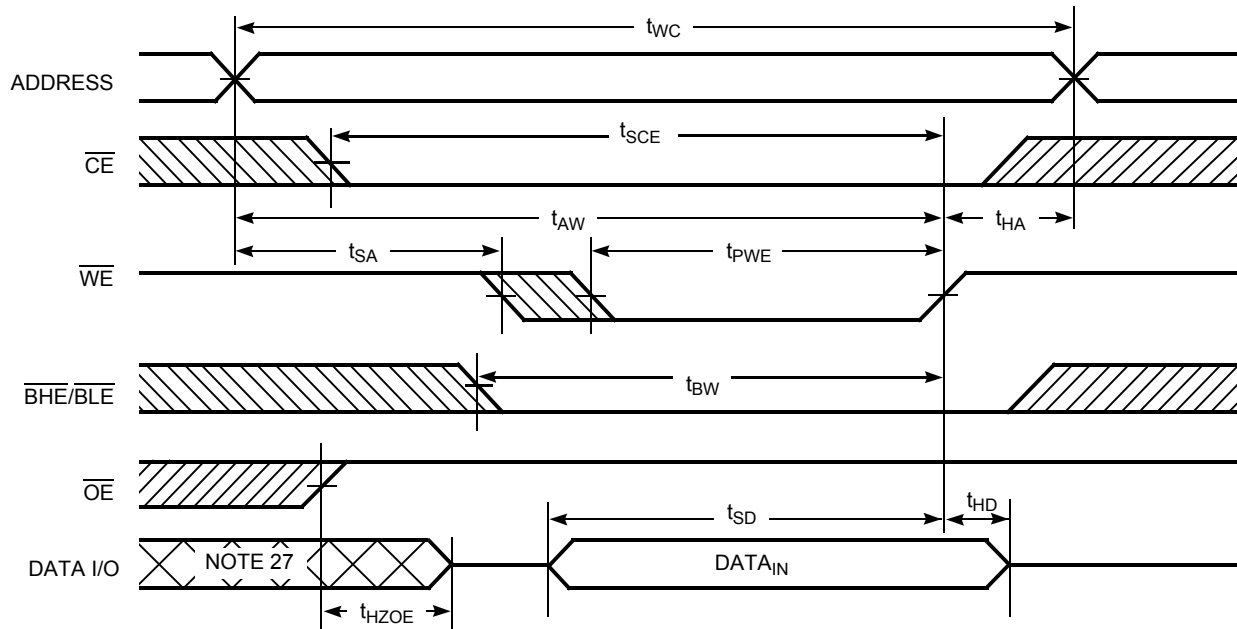
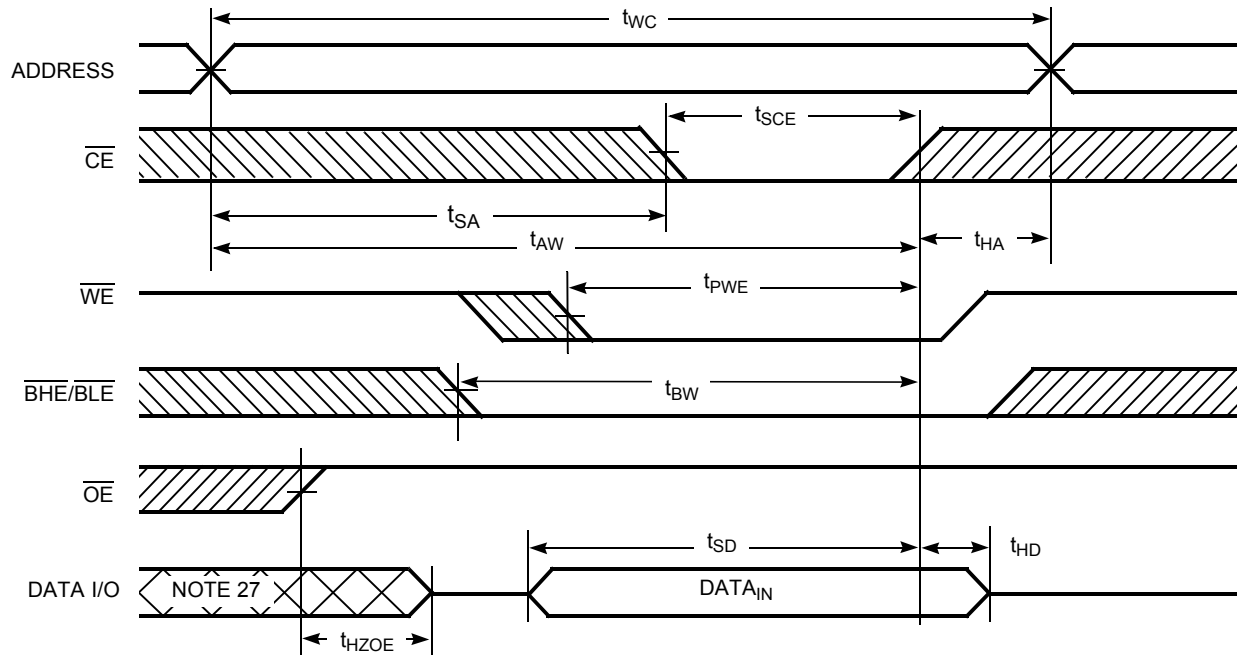
**Figure 6. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)** [22, 23]



### Notes

- 21. The device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}$  =  $V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}}$  =  $V_{\text{IL}}$ .
- 22.  $\overline{\text{WE}}$  is HIGH for read cycle.
- 23. Address valid before or similar to  $\overline{\text{CE}}$ .



**Switching Waveforms (continued)**
**Figure 7. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled) [24, 25, 26]**

**Figure 8. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled) [24, 25, 26]**

**Notes**

24. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{\text{IL}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

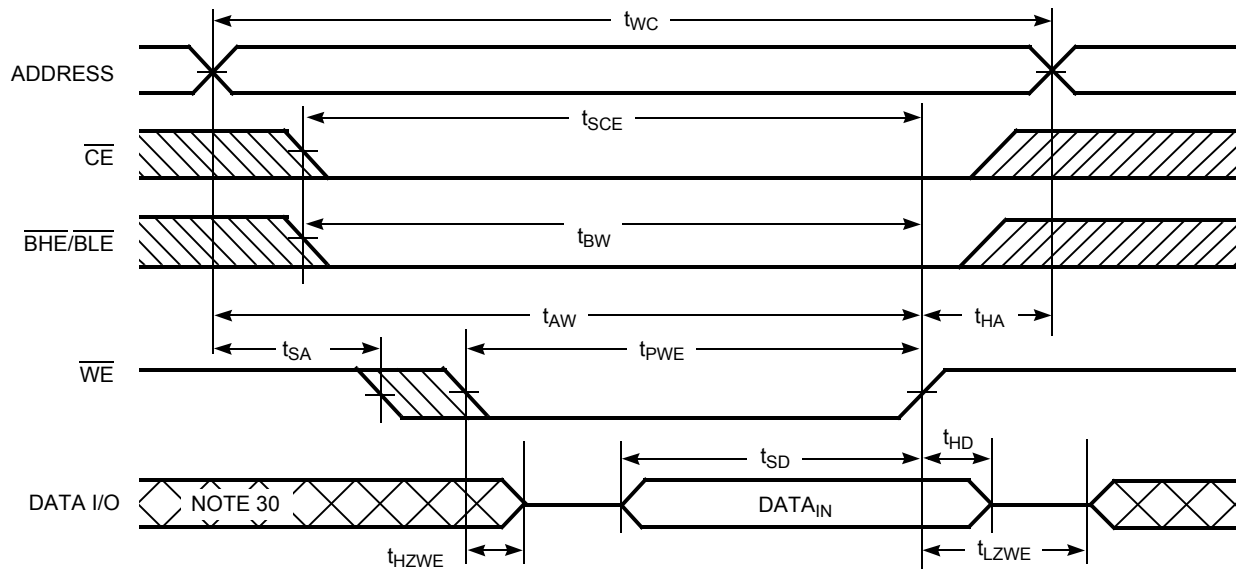
25. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .

26. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}} = V_{\text{IH}}$ , the output remains in a high impedance state.

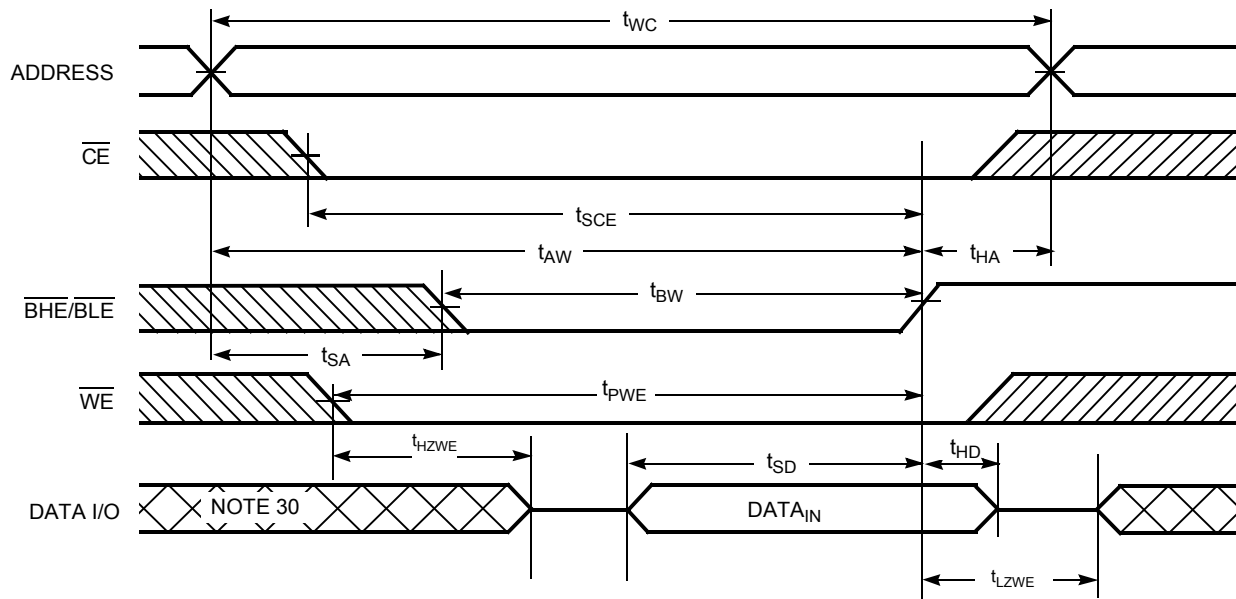
27. During this period, the I/Os are in output state and input signals must not be applied.

## Switching Waveforms (continued)

**Figure 9. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [28, 29]**



**Figure 10. Write Cycle No. 4 ( $\overline{\text{BHE/BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [28]**



### Notes

28. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}} = V_{\text{IH}}$ , the output remains in a high impedance state.

29. The minimum write pulse width for Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) should be sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

30. During this period, the I/Os are in output state and input signals must not be applied.

## Truth Table

| CE <sup>[31]</sup> | WE | OE | BHE | BLE | Inputs/Outputs                                                                                   | Mode                | Power                      |
|--------------------|----|----|-----|-----|--------------------------------------------------------------------------------------------------|---------------------|----------------------------|
| H                  | X  | X  | X   | X   | High-Z                                                                                           | Deselect/power-down | Standby (I <sub>SB</sub> ) |
| L                  | X  | X  | H   | H   | High-Z                                                                                           | Output disabled     | Active (I <sub>CC</sub> )  |
| L                  | H  | L  | L   | L   | Data out (I/O <sub>0</sub> –I/O <sub>15</sub> )                                                  | Read                | Active (I <sub>CC</sub> )  |
| L                  | H  | L  | H   | L   | Data out (I/O <sub>0</sub> –I/O <sub>7</sub> );<br>I/O <sub>8</sub> –I/O <sub>15</sub> in High-Z | Read                | Active (I <sub>CC</sub> )  |
| L                  | H  | L  | L   | H   | Data out (I/O <sub>8</sub> –I/O <sub>15</sub> );<br>I/O <sub>0</sub> –I/O <sub>7</sub> in High-Z | Read                | Active (I <sub>CC</sub> )  |
| L                  | H  | H  | X   | X   | High-Z                                                                                           | Output disabled     | Active (I <sub>CC</sub> )  |
| L                  | L  | X  | L   | L   | Data in (I/O <sub>0</sub> –I/O <sub>15</sub> )                                                   | Write               | Active (I <sub>CC</sub> )  |
| L                  | L  | X  | H   | L   | Data in (I/O <sub>0</sub> –I/O <sub>7</sub> );<br>I/O <sub>8</sub> –I/O <sub>15</sub> in High-Z  | Write               | Active (I <sub>CC</sub> )  |
| L                  | L  | X  | L   | H   | Data in (I/O <sub>8</sub> –I/O <sub>15</sub> );<br>I/O <sub>0</sub> –I/O <sub>7</sub> in High-Z  | Write               | Active (I <sub>CC</sub> )  |

### Note

31. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

## Ordering Information

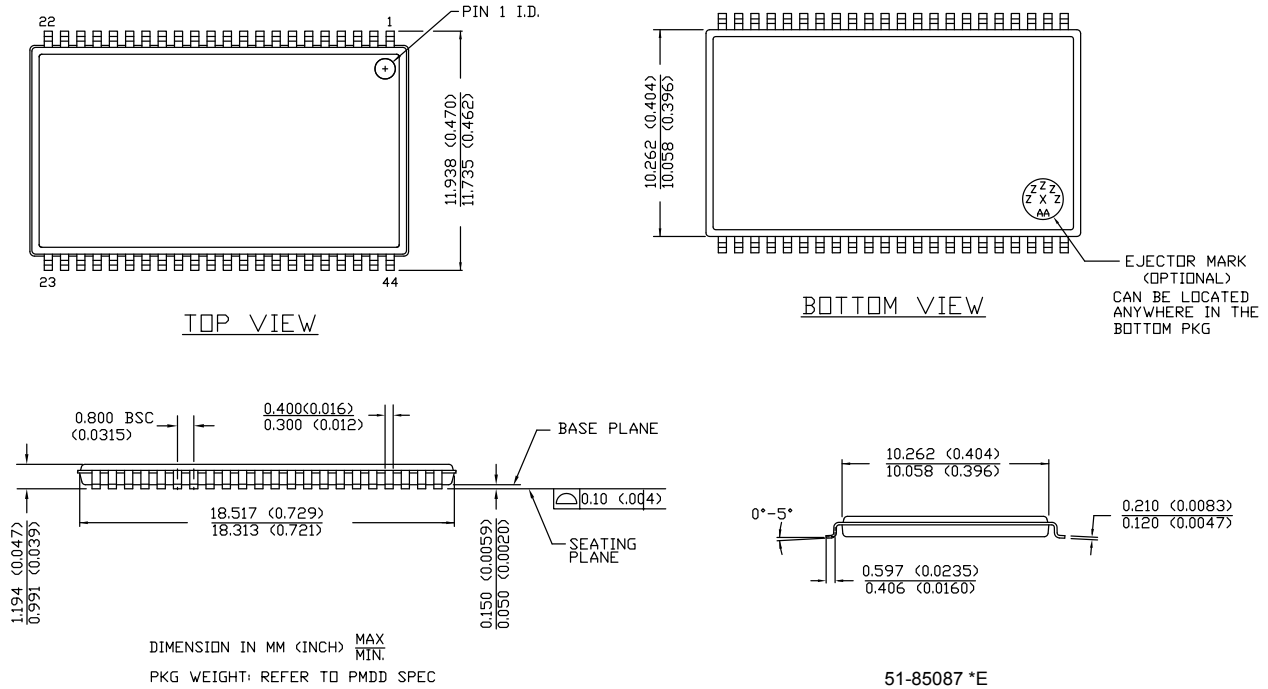
| Speed (ns) | Voltage Range (V) | Ordering Code      | Package Diagram | Package Type                           | Operating Range |
|------------|-------------------|--------------------|-----------------|----------------------------------------|-----------------|
| 45         | 2.2 V–3.6 V       | CY62146GN30-45ZSXI | 51-85087        | 44-pin TSOP II (Pb-free)               | Industrial      |
|            |                   | CY62146GN30-45BVXI | 51-85150        | 48-ball VFBGA (6 × 8 × 1 mm) (Pb-free) |                 |
|            | 4.5 V–5.5 V       | CY62146GN-45ZSXI   | 51-85087        | 44-pin TSOP II (Pb-free)               |                 |

## Ordering Code Definitions

|    |     |   |   |    |    |   |    |    |   |   |                                                             |
|----|-----|---|---|----|----|---|----|----|---|---|-------------------------------------------------------------|
| CY | 621 | 4 | 6 | GN | 30 | - | 45 | XX | X | X |                                                             |
|    |     |   |   |    |    |   |    |    |   |   | Temperature Grade: X = I                                    |
|    |     |   |   |    |    |   |    |    |   |   | I = Industrial                                              |
|    |     |   |   |    |    |   |    |    |   |   | Pb-free                                                     |
|    |     |   |   |    |    |   |    |    |   |   | Package Type: XX = ZS or BV                                 |
|    |     |   |   |    |    |   |    |    |   |   | ZS = TSOP II; BV = 48-Ball VFBGA                            |
|    |     |   |   |    |    |   |    |    |   |   | Speed Grade: 45 ns                                          |
|    |     |   |   |    |    |   |    |    |   |   | Voltage Range: 30 = 3 V typical, No Character = 5 V typical |
|    |     |   |   |    |    |   |    |    |   |   | Process Technology: GN = 65 nm Technology                   |
|    |     |   |   |    |    |   |    |    |   |   | Bus Width: 6 = × 16                                         |
|    |     |   |   |    |    |   |    |    |   |   | Density: 4 = 4-Mbit                                         |
|    |     |   |   |    |    |   |    |    |   |   | Family Code: 621 = MoBL SRAM family                         |
|    |     |   |   |    |    |   |    |    |   |   | Company ID: CY = Cypress                                    |

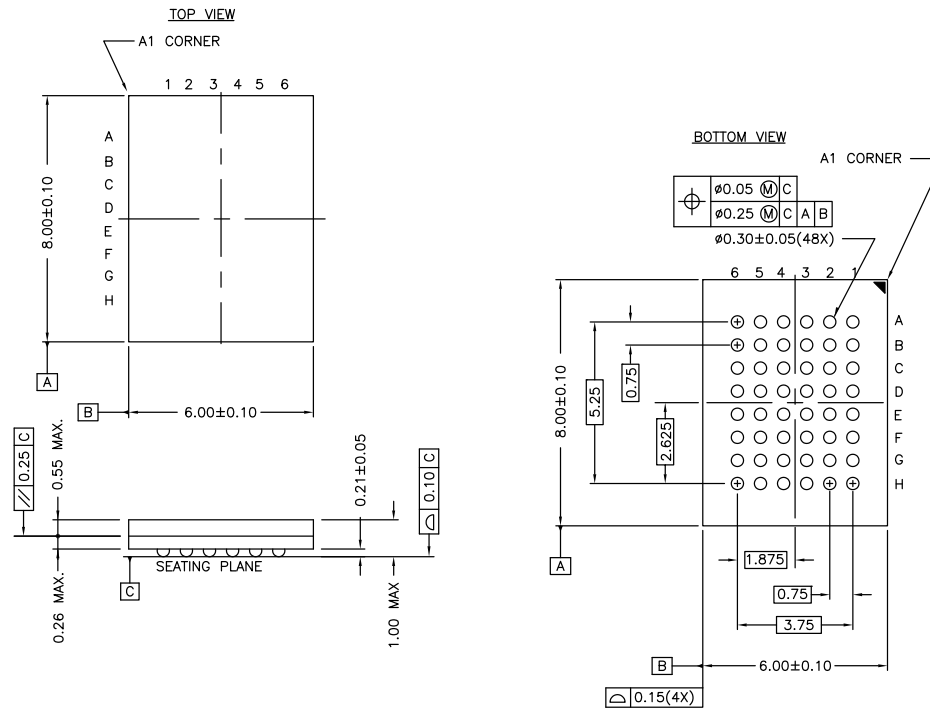
## Package Diagrams

**Figure 11. 44-pin TSOP Z44-II Package Outline, 51-85087**



**Package Diagrams** (continued)

**Figure 12. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150**



NOTE:  
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)  
posted on the Cypress web.

51-85150 \*H

## Acronyms

| Acronym                 | Description                             |
|-------------------------|-----------------------------------------|
| $\overline{\text{BHE}}$ | byte high enable                        |
| $\overline{\text{BLE}}$ | byte low enable                         |
| CMOS                    | complementary metal oxide semiconductor |
| $\overline{\text{CE}}$  | chip enable                             |
| I/O                     | input/output                            |
| $\overline{\text{OE}}$  | output enable                           |
| SRAM                    | static random access memory             |
| TSOP                    | thin small outline package              |
| VFBGA                   | very fine-pitch ball grid array         |
| $\overline{\text{WE}}$  | write enable                            |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | Degrees Celsius |
| MHz    | megahertz       |
| μA     | microamperes    |
| mA     | milliamperes    |
| ns     | nanoseconds     |
| Ω      | ohms            |
| pF     | picofarads      |
| V      | volts           |
| W      | watts           |

## Document History Page

| Document Title: CY62146GN MoBL®, 4-Mbit (256K × 16) Static RAM<br>Document Number: 001-95417 |         |                 |                 |                                                                                                                                                                                                                                                                         |
|----------------------------------------------------------------------------------------------|---------|-----------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                         | ECN No. | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                   |
| **                                                                                           | 5048897 | NILE            | 12/14/2015      | New data sheet.                                                                                                                                                                                                                                                         |
| *A                                                                                           | 5072822 | NILE            | 01/05/2016      | Added "4.5 V to 5.5 V" voltage range related information in all instances across the document.<br>Updated <a href="#">Ordering Information</a> :<br>Updated part numbers.                                                                                               |
| *B                                                                                           | 5092237 | NILE            | 01/21/2016      | Added 48-ball VFBGA package related information in all instances across the document.<br>Updated <a href="#">Ordering Information</a> :<br>Updated part numbers.<br>Updated <a href="#">Package Diagrams</a> :<br>Added spec 51-85150 *H ( <a href="#">Figure 12</a> ). |
| *C                                                                                           | 5142534 | NILE            | 02/18/2016      | Updated <a href="#">Ordering Code Definitions</a> under <a href="#">Ordering Information</a> (Replaced "GN = 90 nm" with "GN = 65 nm Technology").<br>Updated to new template.                                                                                          |



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