

CY62136FV30 MoBL[®] 2 Mbit (128K x 16) Static RAM

Features

- Very high speed: 45 ns
- Temperature ranges
 - □ Industrial: -40°C to +85°C □ Automotive-A: -40°C to +85°C □ Automotive-E: -40°C to +125°C
- Wide voltage range: 2.20V to 3.60V
- Pin compatible with CY62136V, CY62136CV30/CV33, and CY62136EV30
- Ultra low standby power
 - Typical standby current: 1 μA
 - D Maximum standby current: 5 μA (Industrial)
- Ultra low active power
- Typical active current: 1.6 mA at f = 1 MHz (45 ns speed)
- Easy memory expansion with CE and OE features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 48-ball VFBGA and 44-pin TSOP II packages

Functional Description

The CY62136FV30 is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life[™] (MoBL[®]) in portable applications such as cellular telephones. The device also has an

automatic power down feature that significantly reduces power consumption by 90 percent when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected (\overline{CE} HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when:

- Deselected (CE HIGH)
- Outputs are disabled (OE HIGH)
- Both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH)
- Write operation is active (CE LOW and WE LOW)

Write to the device by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₆). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₆).

Read from the device by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the "Truth Table" on page 9 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.



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Product Portfolio

						Power Dissipation						
Product	Panga	V _{CC} Range (V)			Speed	Operating I _{CC} (mA)				Standby I _{SB2}		
Product	Kange				(ns) $f = 1 \text{ MHz}$ $f = f_{\text{max}}$		f = 1 MHz		f _{max}	(μ	Ă)	
		Min	Typ ^[1]	Мах		Typ ^[1]	Typ ^[1] Max		Мах	Typ ^[1]	Мах	
CY62136FV30LL	Industrial/Auto-A	2.2	3.0	3.6	45	1.6 2.5		13	18	1	5	
	Auto-E	2.2	3.0	3.6	55	2	3	15	25	1	20	

Pin Configuration

Figure 1. 48-Ball VFBGA Pinout ^[2, 3]



Figure 2. 44-Pin TSOP II^[2]

			1	
A_4		44		A_5
A_3	□ 2	43		A ₆
A_2	□ 3	42		A ₇
A ₁	4	41		OE
A ₀	5	40		BHE
CE	6	39		BLE
IO_0	7	38		IO15
IO ₁	8 🗆	37		1014
10_2	9	36		10 ₁₃
103	10	35		1012
V _{CC}	11	34	Б	Vee
V _{SS}	12	33		Vcc
IO_4	13	32		10 ₁₁
IO_5	14	31		10 ₁₀
IO_6	□15	30		109
10 ₇	□ 16	29		10_8
WE	L 17	28		NC
A ₁₆	□ 18	27		A ₈
A ₁₅	L 19	26		A ₉
A ₁₄	20	25		A ₁₀
A ₁₃	21	24		A ₁₁
A ₁₂	22	23	р	NC

Notes

Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.
 NC pins are not connected on the die.
 Pins D3, H1, G2, and H6 in the VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb, respectively.



CY62136FV30 MoBL[®]

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature	–65°C to + 150°C
Ambient Temperature with Power Applied	–55°C to + 125°C
Supply Voltage to Ground Potential	–0.3V to 3.9V (V _{CC(max)} + 0.3V)
DC Voltage Applied to Output in High Z State ^[4, 5]	ts –0.3V to 3.9V (V _{CC(max)} + 0.3V)

DC Input Voltage ^[4, 5] –0.3V to 3.9V	$(V_{CC(max)} + 0.3V)$
Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015)	> 2001V
Latch up Current	> 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[6]	
CY62136FV30LL	Ind'l/Auto-A	–40°C to +85°C	2.2V to 3.6V	
	Auto-E	–40°C to +125°C		

Electrical Characteristics

Over the Operating Range

			-45 (I	ndustri	al/Auto-A)					
Parameter	Description	Test Co	Test Conditions		Typ ^[1]	Max	Min	Typ ^[1]	Max	Unit
V _{OH}	Output HIGH Voltage	2.2 <u>≤</u> V _{CC} <u>≤</u> 2.7	I _{OH} = -0.1 mA	2.0			2.0			V
		2.7 <u><</u> V _{CC} <u><</u> 3.6	I _{OH} = -1.0 mA	2.4			2.4			V
V _{OL}	Output LOW Voltage	2.2 <u>≤</u> V _{CC} <u>≤</u> 2.7	I _{OL} = 0.1 mA			0.4			0.4	V
		2.7 <u>≤</u> V _{CC} <u>≤</u> 3.6	I _{OL} = 2.1mA			0.4			0.4	V
V _{IH}	Input HIGH Voltage	2.2 <u>≤</u> V _{CC} <u>≤</u> 2.7		1.8		V _{CC} +0.3	1.8		V _{CC} + 0.3	V
		2.7 <u><</u> V _{CC} <u><</u> 3.6		2.2		V _{CC} +0.3	2.2		$V_{CC} + 0.3$	V
V _{IL}	Input LOW Voltage	$2.2 \leq V_{CC} \leq 2.7$		-0.3		0.6	-0.3		0.6	V
		2.7 <u><</u> V _{CC} <u><</u> 3.6		-0.3		0.8	-0.3		0.8	V
I _{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		-1		+1	-4		+4	μA
I _{OZ}	Output Leakage	$GND \leq V_O \leq V_{CC}, O$	utput Disabled	-1		+1	-4		+4	μA
	Current									
I _{CC}	V _{CC} Operating Supply	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$		13	18		15	25	mA
	Current	f = 1 MHz	I _{OUT} = 0 mA CMOS Levels		1.6	2.5		2	3	
I _{SB1}	Automatic CE Power	CE <u>></u> V _{CC} – 0.2V,	I.		1	5		1	20	μA
	Down Current — CMOS	$V_{IN} \ge V_{CC} - 0.2V$, V	∕ _{IN} <u><</u> 0.2V,							
	Inputs	f = f _{max} (Address a	nd Data Only),							
		f = 0 (OE, WE, BHI	E, and BLE),							
		$V_{CC} = 3.60V$								
I _{SB2} ^[7]	Automatic CE Power	$CE \ge V_{CC} - 0.2V$,			1	5		1	20	μA
	Down Current — CMOS	$V_{\rm IN} \ge V_{\rm CC} - 0.2V$ o	or V _{IN} <u><</u> 0.2V,							
	Inputs	$t = 0, V_{CC} = 3.60V$								ĺ

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Description Test Conditions			
C _{IN}	Input Capacitance	$T_A = 25^{\circ}C, f = 1 \text{ MHz},$	10	pF	
C _{OUT}	Output Capacitance	$V_{CC} = V_{CC(typ)}$	10	pF	

Notes

V_{IL(min)} = -2.0V for pulse durations less than 20 ns.
 V_{IL(max)}=V_{CC}+0.75V for pulse durations less than 20 ns.
 V_{IL(max)}=V_{CC}+0.75V for pulse durations less than 20 ns.
 Full device AC operation assumes a minimum of 10<u>0 µ</u>s ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
 Full device AC operation assumes a minimum of 10<u>0 µ</u>s ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
 Only chip enable (CE) and byte enables (BHE and BLE) are tied to CMOS levels to meet the I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.



Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	VFBGA	TSOP II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still air, soldered on a 3 × 4.5 inch, two layer printed circuit board	75	77	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		10	13	°C/W

Figure 3. AC Test Loads and Waveforms



Parameters	2.5V (2.2V to 2.7V)	3.0V (2.7V to 3.6V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Тур [1]	Мах	Unit	
V _{DR}	V _{CC} for Data Retention			1.5			V
I _{CCDR} ^[7]	Data Retention Current	$V_{CC} = 1.5V, \overline{CE} \ge V_{CC} - 0.2V,$	Industrial/Auto-A			4	μA
		$V_{IN} \ge V_{CC} - 0.2V \text{ or } V_{IN} \le 0.2V$	Auto-E			12	
t _{CDR} ^[8]	Chip Deselect to Data Retention Time			0			ns
t _R ^[9]	Operation Recovery Time			t _{RC}			ns

Figure 4. Data Retention Waveform ^[10]



Notes

8. Tested initially and after any design or process changes that may affect these parameters.
 9. <u>Full device</u> operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.
 10. BHE.BLE is the AND of both BHE and BLE. Deselect the chip by either disabling chip enable signals or by disabling both BHE and BLE.



Switching Characteristics

Over the Operating Range [11, 12]

Doromotor	Description	-45 (Indus	trial/Auto-A)	-55 (A	Unit	
Farameter	Description	Min	Max	Min	Мах	Onit
Read Cycle						
t _{RC}	Read Cycle Time	45		55		ns
t _{AA}	Address to Data Valid		45		55	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	CE LOW to Data Valid		45		55	ns
t _{DOE}	OE LOW to Data Valid		22		25	ns
t _{LZOE}	OE LOW to Low Z ^[13]	5		5		ns
t _{HZOE}	OE HIGH to High Z [13, 14]		18		20	ns
t _{LZCE}	CE LOW to Low Z ^[13]	10		10		ns
t _{HZCE}	CE HIGH to High Z ^[13, 14]		18		20	ns
t _{PU}	CE LOW to Power Up	0		0		ns
t _{PD}	CE HIGH to Power Down		45		55	ns
t _{DBE}	BLE/BHE LOW to Data Valid		22		25	ns
t _{LZBE}	BLE/BHE LOW to Low Z ^[13]	5		5		ns
t _{HZBE}	BLE/BHE HIGH to High Z ^[13, 14]		18		20	ns
Write Cycle ^[1]	5]					
t _{WC}	Write Cycle Time	45		55		ns
t _{SCE}	CE LOW to Write End	35		40		ns
t _{AW}	Address Setup to Write End	35		40		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Setup to Write Start	0		0		ns
t _{PWE}	WE Pulse Width	35		40		ns
t _{BW}	BLE/BHE LOW to Write End	35		40		ns
t _{SD}	Data Setup to Write End	25		25		ns
t _{HD}	Data Hold From Write End	0		0		ns
t _{HZWE}	WE LOW to High Z ^[13, 14]		18		20	ns
t _{LZWE}	WE HIGH to Low Z ^[13]	10		10		ns

Notes

14. t_{HZOE}, t_{HZOE}, t_{HZDE}, and t_{HZWE} transitions are measured when the <u>outputs</u> enter <u>a high</u> impedance state.
 15. The internal write time of the memory is defined by the overlap of WE, CE = V_{IL}, BHE and/or BLE = V_{IL}. All signals are ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.

Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of V_{CC(typ}/2, input pulse levels of 0 to V_{CC(typ}), and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" on page 4.
 AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. Please see application note AN13842 for further clarification

^{13.} At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZOE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.



Switching Waveforms



Figure 6. Read Cycle No. 2: DE Controlled ^[17, 18]



Notes

- 16. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{|L}$, \overline{BHE} and $\overline{BLE} = V_{|L}$. 17. \overline{WE} is HIGH for read cycle.
- 18. Address valid before or similar to \overline{CE} and \overline{BHE} , \overline{BLE} transition LOW.



Switching Waveforms (continued)



Figure 7. Write Cycle No 1: WE Controlled ^[15, 19, 20]

Notes 19. Data IO is high impedance if $\overline{OE} = V_{IH}$. 20. If CE goes HIGH simultaneously with WE = V_{IH} , the output remains in a high impedance state. 21. During this period, the IOs are in output state. Do not apply input signals.



Switching Waveforms (continued)



Figure 9. Write Cycle 3: $\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW ^[20]

Figure 10. Write Cycle 4: BHE/BLE Controlled, OE LOW [20]





Truth Table

CE	WE	OE	BHE	BLE	Inputs or Outputs	Mode	Power
Н	Х	Х	Х	Х	High Z	Deselect or Power Down	Standby (I _{SB})
Х	Х	Х	Н	Н	High Z	Deselect or Power Down	Standby (I _{SB})
L	Н	L	L	L	Data Out (I/O ₀ –I/O ₁₅)	Read	Active (I _{CC})
L	Н	L	Н	L	Data Out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Read	Active (I _{CC})
L	Н	L	L	Н	Data Out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Read	Active (I _{CC})
L	Н	Н	L	L	High Z	Output Disabled	Active (I _{CC})
L	Н	Н	Н	L	High Z	Output Disabled	Active (I _{CC})
L	Н	Н	L	Н	High Z	Output Disabled	Active (I _{CC})
L	L	Х	L	L	Data In (I/O ₀ –I/O ₁₅)	Write	Active (I _{CC})
L	L	Х	Н	L	Data In (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Write	Active (I _{CC})
L	L	Х	L	Н	Data In (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Write	Active (I _{CC})



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62136FV30LL-45BVXI	51-85150	48-Ball VFBGA (Pb-Free)	Industrial
	CY62136FV30LL-45ZSXI	51-85087	44-Pin TSOP II (Pb-Free)	
	CY62136FV30LL-45ZSXA	51-85087	44-Pin TSOP II (Pb-Free)	Automotive-A
55	CY62136FV30LL-55ZSXE	51-85087	44-Pin TSOP II (Pb-Free)	Automotive-E

Contact your local Cypress sales representative for availability of these parts.

TOP VIEW

Package Diagrams

Figure 11. 48-Ball VFBGA (6 x 8 x 1 mm)







51-85150-*D



Package Diagrams (continued)

Figure 12. 44-Pin TSOP II

dimension in MM (inch) Max Min



0.597 (0.0235)



51-85087-*A



Document History Page

Document Title: CY62136FV30 MoBL [®] 2 Mbit (128K x 16) Static RAM Document Number: 001-08402							
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change			
**	467351	See ECN	NXR	New datasheet			
*A	797956	See ECN	VKN	Converted from preliminary to final Changed I _{SB1(typ)} and I _{SB1(max)} specification from 0.5 μ A to 1.0 μ A and 2.5 μ A to 5.0 μ A, respectively Changed I _{SB2(typ)} and I _{SB2(max)} specification from 0.5 μ A to 1.0 μ A and 2.5 μ A to 5.0 μ A, respectively Changed I _{CCDR(typ)} and I _{CCDR(max)} specification from 0.5 μ A to 1.0 μ A and 2.5 μ A to 4.0 μ A, respectively Changed I _{CCDR(typ)} and I _{CCDR(max)} specification from 0.5 μ A to 1.0 μ A and 2.5 μ A to 4.0 μ A, respectively Changed I _{CC(max)} specification from 2.25 μ A to 2.5 μ A			
*B	869500	See ECN	VKN	Added Automotive information Updated Ordering information table Added footnote 12 related to t _{ACE}			
*C	901800	See ECN	VKN	Added footnote 9 related to ${\sf I}_{SB2}$ and ${\sf I}_{CCDR}$ Made footnote 13 applicable to AC parameters from t_{ACE}			
*D	1371124	See ECN	VKN/AESA	Converted Automotive information from preliminary to final Changed I _{IX} min spec from $-1 \mu A$ to $-4 \mu A$ and I _{IX} max spec from $+1 \mu A$ to $+4 \mu A$ Changed I _{OZ} min spec from $-1 \mu A$ to $-4 \mu A$ and I _{OZ} max spec from $+1 \mu A$ to $+4 \mu A$ Changed t _{DBE} spec from 55 ns to 25 ns for automotive part			
*E	2594937	10/22/08	NXR/PYRS	Added Automotive-A information Changed t _{LZBE} from 10 ns to 5 ns for -55.			
*F	2675375	03/17/2009	VKN/PYRS	Corrected typo on page 2 (Corrected I_{SB2} unit to μA from mA)			

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Page 12 of 12

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