



# Laser Printer System Frequency Synthesizer

## Features

- Maximized EMI suppression using Cypress's Spread Spectrum technology
- Reduces measured EMI by as much as 10 dB
- Four skew-controlled copies of CPU output
- Four skew-controlled copies of SDRAM output
- One copy of 14.31818-MHz Reference output
- One copy of 48-MHz USB clock (not spread)
- Selectable SSFTG modulation width
- Available in 28-pin SSOP (209 mil)

## Key Specifications

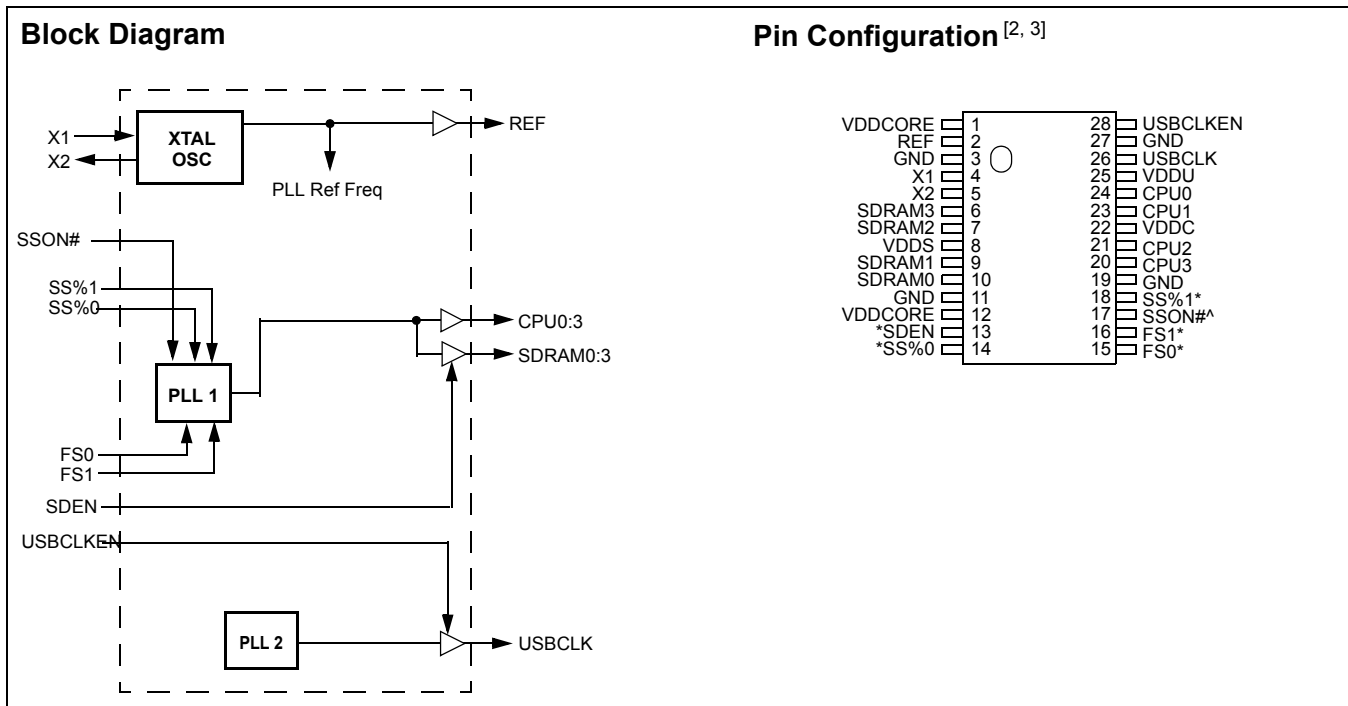
Supply Voltage:  
 VDDCORE: ..... 3.3V±10%  
 VDDC: ..... 3.3V±10% or 2.5V±5%  
 VDDS: ..... 3.3V±10% or 2.5V±5%  
 VDDU: ..... 3.3V±10% or 2.5V±5%  
 CPU Clock Cycle to Cycle Jitter: ..... 250 ps  
 USBCLK Long term Jitter: ..... ± 500 ps  
 CPU0:3 Clock Skew: ..... 250 ps  
 CPU, SDRAM Output on Resistance: ..... 15Ω  
 Logic inputs have 250K-ohm pull-up resistors

Table 1. Pin Selectable Frequency<sup>[1]</sup>

FS1	FS0	CPU(0:3), SDRAM(0:3)	USBCLK
0	0	133.3 MHz	48 MHz
0	1	100 MHz	48 MHz
1	0	66.6 MHz	48 MHz
1	1	50 MHz	48 MHz

Table 2. Spread Characteristics.

SSON#	SS%1	SS%0	CPU(0:3), SDRAM(0:3)
0	0	0	-0.5%
0	0	1	-1.0%
0	1	0	-2.5%
0	1	1	-3.75%
1	0	0	0 (off)\
1	0	1	0 (off)
1	1	0	0 (off)
1	1	1	0 (off)



- Notes:
1. All clock output loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
  2. Signals marked with [\*] have internal pull-up resistors
  3. Signal marked with [^] has internal pull-down resistors.

**Pin Definitions**

Pin Name	Pin No.	Pin Type	Pin Description
CPU0:3	24, 23, 21, 20	O	<b>CPU Clock Outputs:</b> These four outputs run at a frequency set by FS0:1. The width of the Spread Spectrum Modulation is enabled by pin SSON#, and selected by pins SS%0:1.
SDRAM0:3	10, 9, 7, 6	O	<b>SDRAM Outputs:</b> These four SDRAM clock outputs run synchronously to the CPU clock. Modulation and frequency follow the CPU outputs.
FS0:1	15, 16	I	<b>Frequency Selection Inputs:</b> Selects CPU clock frequency as shown in <i>Table 1</i> .
SS%0:1	14, 18	I	<b>Modulation Width Selection Inputs:</b> These inputs select the width of the Spread Spectrum feature when it is enabled by SSON#.
USBCLK	26	O	<b>USB Output:</b> Timing signal running at 48.0080 MHz when a 14.31818-MHz frequency is provided as the reference. (167 ppm accuracy to 48 MHz, the output is equal to the reference times 57/17.)
SSON#	17	I	<b>CPU Spread Spectrum Enable Input:</b> When this pin is pulled LOW, outputs CPU0:3 and SDRAM0:3 will have the Spread Spectrum Feature enabled.
USBCLKEN	28	I	<b>USB Disable Input:</b> When this pin is pulled LOW, output USBCLK will be disabled to a LOW state.
REF	2	O	<b>Reference Output:</b> This output will be equal in frequency to the reference signal provided at X1/X2.
SDEN	13	I	<b>SDRAM Bank Disable Input:</b> When this pin is pulled LOW, outputs SDRAM0:3 will be disabled to a LOW state.
X1	4	I	<b>Crystal Connection or External Reference Frequency Input:</b> Connect to either a 14.318-MHz crystal or other reference signal.
X2	5	I	<b>Crystal Connection:</b> An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
VDDCORE	1, 12	P	<b>Power Connection:</b> Core Power supply. Connect to 3.3V supply.
VDDU	25	P	<b>Power Connection:</b> Power supply for the USB output. Connect to 3.3V or 2.5V supply.
VDDC	22	P	<b>Power Connection:</b> Power supply for the CPU outputs. Connect to 3.3V or 2.5V supply.
VDDS	8	P	<b>Power Connection:</b> Power supply for the SDRAM outputs. Connect to 3.3V or 2.5V supply.
GND	3,11, 19, 27	G	<b>Ground Connections:</b> Connect all ground pins to the common system ground plane.

## Spread Spectrum Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 1*.

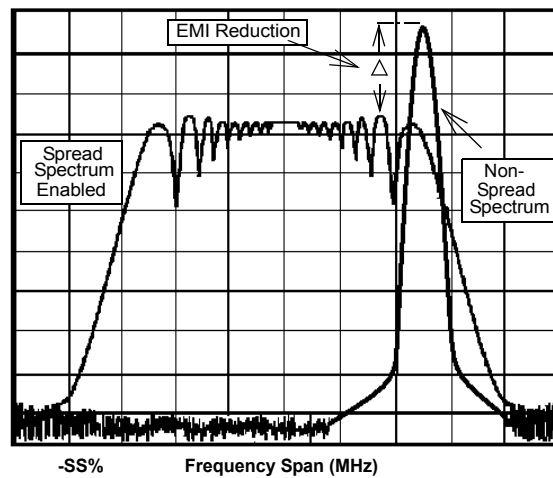
As shown in *Figure 1*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9 \cdot \log_{10}(P) + 9 \cdot \log_{10}(F)$$

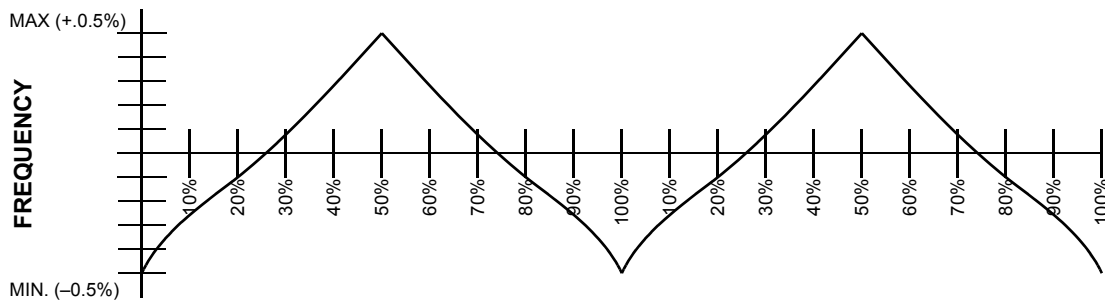
Where  $P$  is the percentage of deviation and  $F$  is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 2*. This waveform, as discussed in “Spread Spectrum Clock Generation for the Reduction of Radiated Emissions” by Bush, Fessler, and Hardin, produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is  $\pm 0.5\%$  of the center frequency. *Figure 2* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for bits 1–0 in data byte 0 of the SMBus data stream.



**Figure 1. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation**



**Figure 2. Typical Modulation Profile**

**Absolute Maximum Ratings<sup>[4]</sup>**

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress

rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
$V_{DD}, V_{IN}$	Voltage on any pin with respect to GND	-0.5 to +7.0	V
$T_{STG}$	Storage Temperature	-65 to +150	°C
$T_A$	Operating Temperature	-55 to +125	°C
$T_B$	Ambient Temperature under Bias	0 to +70	°C
$ESD_{PROT}$	Input ESD Protection	2 (min.)	kV

**DC Electrical Characteristics:**

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 10\%$

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
<b>Supply Current</b>						
$I_{DDQ3}$	Supply Current (3.3V)	CPUCLK = 100 MHz Outputs Loaded <sup>[4]</sup>			400	mA
$I_{DDQ2}$	Supply Current (2.5V)	CPUCLK = 100 MHz Outputs Loaded <sup>[4]</sup>			400	mA
<b>Logic Inputs<sup>[5]</sup></b>						
$V_{IL}$	Input Low Voltage		GND-3		0.8	V
$V_{IH}$	Input High Voltage		2.0		$V_{DD} + .3$	V
$I_{IL}$	Input Low Current <sup>[6]</sup>				-25	μA
$I_{IH}$	Input High Current <sup>[6]</sup>				10	μA
<b>Crystal Oscillator</b>						
$V_{TH}$	X1 Input Threshold Voltage <sup>[1]</sup>			1.5		V
$C_{LOAD}$	Load Capacitance, Imposed on External Crystal <sup>[7]</sup>			14		pF
$C_{IN,X1}$	X1 Input Capacitance <sup>[8]</sup>	Pin X2 unconnected		28		pF
<b>Pin Capacitance/Inductance</b>						
$C_{IN}$	Input Pin Capacitance	Except X1 and X2			5	pF
$C_{OUT}$	Output Pin Capacitance				6	pF
$L_{IN}$	Input Pin Inductance				7	nH

**Notes:**

- Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
- CY24242 logic inputs have internal pull-up resistors.
- X1 input threshold voltage (typical) is  $V_{DDQ}/2$ .
- The CY24242 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14 pF; this includes typical stray capacitance of short PCB traces to crystal.
- X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

**AC Electrical Characteristics**
 $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ ,  $V_{DD} = V_{DDQ3} = 3.3\text{V} \pm 10\%$ ,  $f_{XTL} = 14.31818\text{ MHz}$ 

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

**CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20 pF,  $V_{DDC} = 3.3\text{V}$ )**

Parameter	Description	Test Condition/Comments	CPU = 66 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_P$	Period	Measured on rising edge at 1.5V	15	–	15.5	10	–	10.5	ns
$t_H$	High Time	Duration of clock cycle above 2.4V	5.2	–	–	3.0	–	–	ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	5	–	–	2.8	–	–	ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.4	–	3.2	0.4	–	3.2	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.4	–	3.2	0.4	–	3.2	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45	–	55	45	–	55	%
$t_{JC}$	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.	–	–	250	–	–	250	ps
$t_{SK}$	Output Skew	Measured on rising edge at 1.5V	–	–	250	–	–	250	ps
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.	–	–	3	–	–	3	ms
$Z_o$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	–	20	–	–	20	–	$\Omega$

**SDRAM Clock Outputs, SDRAM0:3 (Lump Capacitance Test Load = 30 pF,  $V_{DDC} = 3.3\text{V}$ )**

Parameter	Description	Test Condition/Comments	CPU = 66 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_P$	Period	Measured on rising edge at 1.5V	15	–	15.5	10	–	10.5	ns
$t_H$	High Time	Duration of clock cycle above 2.4V	5.2	–	–	3.0	–	–	ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	5	–	–	2.8	–	–	ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.4	–	3.2	0.4	–	3.2	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.4	–	3.2	0.4	–	3.2	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.5V	45	–	55	45	–	55	%
$t_{JC}$	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.	–	–	250	–	–	250	ps
$t_{SK}$	Output Skew	Measured on rising edge at 1.5V	–	100	300	–	100	350	ps
$t_{SK}$	CPU to SDRAM Clock Skew	Covers all CPU/SDRAM outputs. Measured on rising edge at 1.5V.	–	–	350	–	–	350	ps
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.	–	–	3	–	–	3	ms
$Z_o$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	–	20	–	–	20	–	$\Omega$

**REF Clock Outputs (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/Comments	CPU = 66/100MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency equal to the reference provided at pins X1, X2	14.318			MHz
t <sub>R</sub>	Output Rise Edge Rate		0.5	–	2	V/ns
t <sub>F</sub>	Output Fall Edge Rate		0.5	–	2	V/ns
t <sub>D</sub>	Duty Cycle	Measured on rising and falling edge at 1.5V	45	–	55	%
f <sub>ST</sub>	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.	–	–	3	ms
Z <sub>O</sub>	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	–	40	–	Ω

**USBCLK Clock Output (Lump Capacitance Test Load = 20 pF, V<sub>DDC</sub> = 3.3V)**

Parameter	Description	Test Condition/Comments	CPU = 66/100 MHz			Unit
			Min.	Typ.	Max.	
t <sub>R</sub>	Output Rise Edge Rate		0.5	–	2	V/ns
t <sub>F</sub>	Output Fall Edge Rate		0.5	–	2	V/ns
t <sub>D</sub>	Duty Cycle	Measured on rising and falling edge at 1.5V	45	–	55	%
t <sub>JL</sub>	Jitter, Long term	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.	–	–	500	
t <sub>JC</sub>	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.	–	–	400	
f <sub>ST</sub>	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.	–	–	3	ms
Z <sub>O</sub>	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	–	40	–	Ω

**Absolute Maximum Ratings**

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress

rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V <sub>DD</sub> , V <sub>IN</sub>	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T <sub>STG</sub>	Storage Temperature	–65 to +150	°C
T <sub>A</sub>	Operating Temperature	–55 to +125	°C
T <sub>B</sub>	Ambient Temperature under Bias	0 to +70	°C
ESD <sub>PROT</sub>	Input ESD Protection	2 (min.)	kV

**AC Electrical Characteristics**
 $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ ,  $V_{DD} = V_{DDQ3} = 2.5\text{V} \pm 5\%$ ,  $f_{XTL} = 14.31818\text{ MHz}$ 

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

**CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20 pF,  $V_{DDC} = 2.5\text{V}$ )**

Parameter	Description	Test Condition/Comments	CPU = 66 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_P$	Period	Measured on rising edge at 1.25V	15	–	15.5	10	–	10.5	ns
$t_H$	High Time	Duration of clock cycle above 2.0V	5.2	–	–	3.0	–	–	ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	5	–	–	2.8	–	–	ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.0V	0.4	–	3.2	0.4	–	3.2	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.0V to 0.4V	0.4	–	3.2	0.4	–	3.2	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.25V	45	–	55	45	–	55	%
$t_{JC}$	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.	–	–	250	–	–	250	ps
$t_{SK}$	Output Skew	Measured on rising edge at 1.25V	–	–	250	–	–	250	ps
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.	–	–	3	–	–	3	ms
$Z_o$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	–	20	–	–	20	–	$\Omega$

**SDRAM Clock Outputs, SDRAM0:3 (Lump Capacitance Test Load = 30 pF,  $V_{DDC} = 2.5\text{V}$ )**

Parameter	Description	Test Condition/Comments	CPU = 66 MHz			CPU = 100 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_P$	Period	Measured on rising edge at 1.25V	15	–	15.5	10	–	10.5	ns
$t_H$	High Time	Duration of clock cycle above 2.0V	5.2	–	–	3.0	–	–	ns
$t_L$	Low Time	Duration of clock cycle below 0.4V	5	–	–	2.8	–	–	ns
$t_R$	Output Rise Edge Rate	Measured from 0.4V to 2.0V	0.4	–	3.2	0.4	–	3.2	V/ns
$t_F$	Output Fall Edge Rate	Measured from 2.0V to 0.4V	0.4	–	3.2	0.4	–	3.2	V/ns
$t_D$	Duty Cycle	Measured on rising and falling edge at 1.25V	45	–	55	45	–	55	%
$t_{JC}$	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.	–	–	250	–	–	250	ps
$t_{SK}$	Output Skew	Measured on rising edge at 1.25V	–	250	300	–	250	350	ps
$f_{ST}$	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.	–	–	3	–	–	3	ms
$Z_o$	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	–	20	–	–	20	–	$\Omega$

**REF Clock Outputs (Lump Capacitance Test Load = 20 pF)**

Parameter	Description	Test Condition/Comments	CPU = 66/100 MHz			Unit
			Min.	Typ.	Max.	
f	Frequency, Actual	Frequency equal to the reference provided at pins X1, X2	14.318			MHz
t <sub>R</sub>	Output Rise Edge Rate	Measured from 0.4V to 2.0	0.5	–	2	V/ns
t <sub>F</sub>	Output Fall Edge Rate	Measured from 2.0V to 0.4V	0.5	–	2	V/ns
t <sub>D</sub>	Duty Cycle	Measured on rising and falling edge at 1.25V	45	–	55	%
f <sub>ST</sub>	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.	–	–	3	ms
Z <sub>o</sub>	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	–	40	–	Ω

**USBCLK Clock Output (Lump Capacitance Test Load = 20 pF, V<sub>DDC</sub> =2.5V)**

Parameter	Description	Test Condition/Comments	CPU = 66/100 MHz			Unit
			Min.	Typ.	Max.	
t <sub>R</sub>	Output Rise Edge Rate	Measured from 0.4V to 2.0	0.5	–	2	V/ns
t <sub>F</sub>	Output Fall Edge Rate	Measured from 2.0V to 0.4V	0.5	–	2	V/ns
t <sub>D</sub>	Duty Cycle	Measured on rising and falling edge at 1.25V	45	–	55	%
t <sub>JL</sub>	Jitter, Long term	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.	–	–	500	
t <sub>JC</sub>	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.	–	–	400	
f <sub>ST</sub>	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.	–	–	3	ms
Z <sub>o</sub>	AC Output Impedance	Average value during switching transition. Used for determining series termination value.	–	40	–	Ω

**Ordering Information**

Ordering Code	Package Type	Temperature Grade
<b>Standard</b>		
CY24242PVC	28-pin SSOP (300 mils)	C (Commercial 0 - 70°)
CY24242PVCT	28-pin SSOP (300 mils) - Tape and Reel	C (Commercial 0 - 70°)
<b>Lead-free</b>		
CY24242OXC	28-pin SSOP (300 mils)	C (Commercial 0 - 70°)
CY24242OXCT	28-pin SSOP (300 mils) - Tape and Reel	C (Commercial 0 - 70°)





**Document History Page**

<b>Document Title: CY24242 Laser Printer Frequency Synthesizer</b>				
<b>Document Number: 38-07268</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	110533	10/08/01	SZV	Change from Spec number: 38-01133 to 38-07268
*A	122866	12/20/02	RBI	Added power-up requirements to maximum ratings information.
*B	310556	See ECN	RGL	Added Lead-free devices