EVK-HADES1210

Version: 1.0

HADES® v2 High Temperature Isolated Gate Driver Evaluation Kit - Product Brief

General description

EVK-HADES1210 Evaluation Kit implements a power half-bridge based on the HADES v2 isolated gate driver and two CISSOID's NEPTUNE, a 10A/1200V SiC MOSFET.
It includes an evaluation board allowing to implement immediately a power converter or a motor drive, and is designed for bus voltage up to 1200V and with application current up to 10A. The two channels can be controlled independently of each other or use a locally generated non-overlap delay.
The Reference Design is based on the 2nd generation HADES chipset which consists of 3 devices: a Primary device CHT-HADES2P, a secondary device CHT-HADES2S and CHT-ELARA 80V quad-diode. It includes an isolated power supply built around CHT-HADES2P PWM controller.
The Evaluation Board EVK-HADES2 can be used for immediate testing with SiC MOSFET devices. The board is populated with CISSOID integrated circuits in ceramic package guaranteed for -55°C to +225°C. The board is based on a polyimide PCB (rated 200°C). The passive components and the desaturation diode allow operation up to 175°C, with possible short excursions to 225°C for testing. The evaluation board is delivered with a full documentation package including the electrical schematic, the bill of materials including active and passive components, and Gerber files.

Applications

- High reliability markets like automotive, aerospace, railway, Oil & Gas
- Motor drivers : downhole, electrical cars, railway, industrial pumps, …
- DC-DC converters and SMPS : battery chargers, …
- Inverters : solar inverters, smart grid, EV and HEV, 3 phases inverters
- Power conversion : uninterruptible power supplies, wind turbine, …

Features

- Board size: 68mm * 54mm
- CISSOID active components rated from -55° to +225°C (Tj)
- 200°C Polyimide PCB
- Board qualified for 175°C ambient
  - Short excursions to 225°C for testing allowed
- Isolated High-side and Low-side gate drivers
- Isolated DC-DC Converter supplying floating drivers
- High Temperature 10A/1200V SiC MOSFET switches
- DC Bus voltage: 600V Typ. (designed for 1200V max)
- Isolation (primary – secondary):
  - 2,500VAC @50Hz (for 1mn)
  - >100MΩ @ 500VDC
- Common mode transient immunity: 30kV/µs Typ. (designed for 50kV/µs)
- Delay time (PWM to VOUT): 200ns typ.
- Gate voltage: 20V/-5V nominal
- MOSFET gate rise time:40ns typ.
- MOSFET gate fall time: 40ns typ.
- DC-DC Converter switching frequency: 180kHz Typ.
- Single power supply: [12-15V] ±10%
- Interfacing voltage (digital I/Os): 15V ±10%
- Under voltage lockout (UVLO)
- Independent PWM inputs for HS and LS drivers or single PWM input with on-board non-overlapping
- Desaturation protection
- Isolated fault outputs
- **Application Note available** on request on our website

Evaluation Board

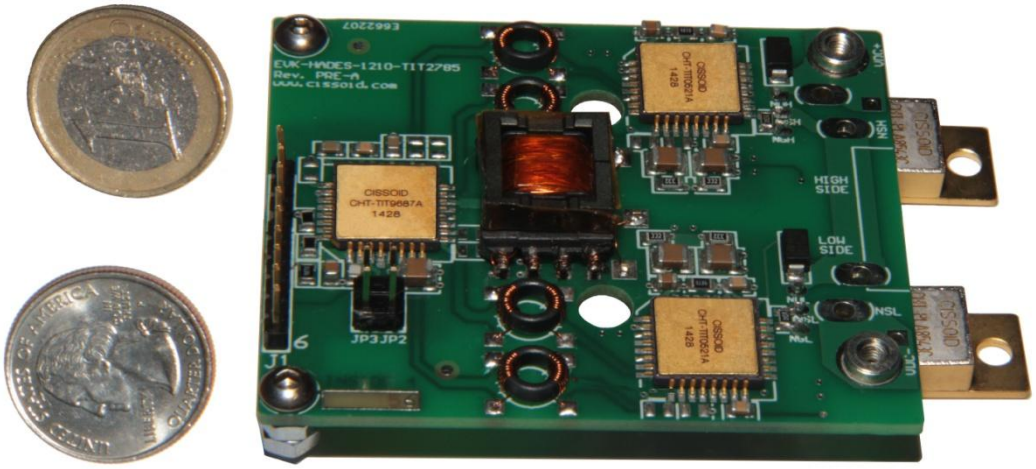


Figure 1. EVK-HADES1210 Evaluation Board (68mm * 54mm)

High level block diagram

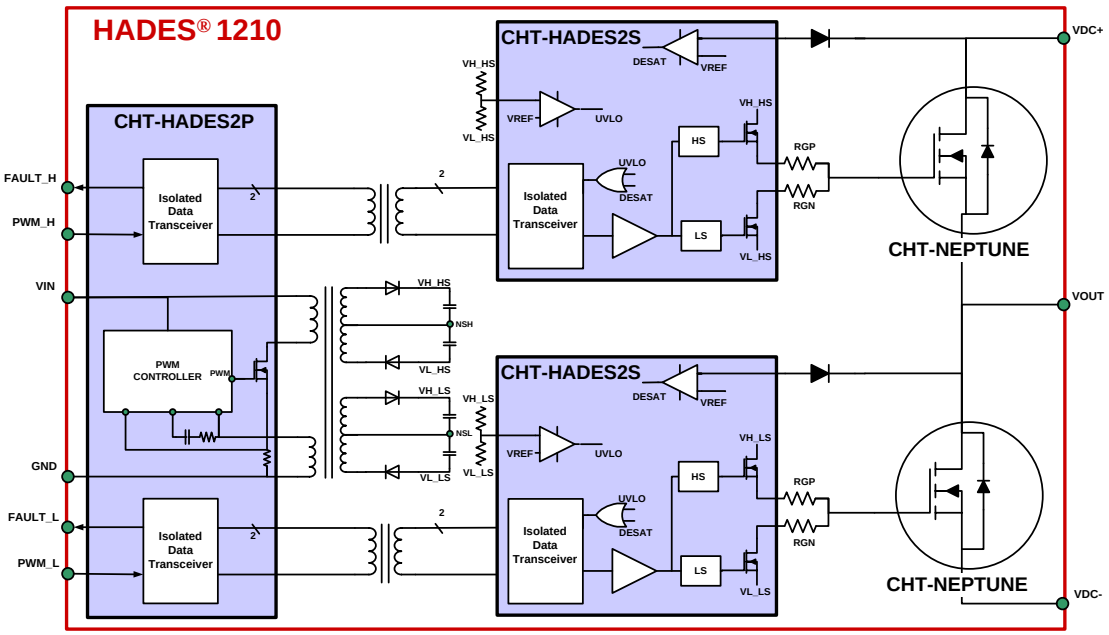


Figure 2: EVK-HADES1210 High Level Block Diagram

EVK-HADES1210 implements 4 main functions

- Two isolated gate drivers
- An isolated switched-mode power supply
- Local Non-Overlapping Management block
- Two 10A 1200V power switches

The two isolated gate drivers are identical; they are based on the highly integrated 2nd generation HADES chipset (HADES2S at secondary side and HADES2P at primary side) and each of them provides following functionalities:

- Up to 12A peak gate drive current
- Monitoring and fault reporting of the gate driver power supplies (UVLO) (threshold is programmable via on-board resistors)
- Cycle-by-cycle Desaturation monitoring and fault reporting (DESAT) (immediate FET turn-off in case of desaturation detection); threshold is programmable via on-board resistors and blanking time is programmable via a capacitor
- Fully isolated PWM and FAULT signals between EVK-HADES1210 external connections and gate driver signals
- Support for Active Miller Clamp protecting the power MOSFET from parasitic turn-on (function not populated on the PCB)
- Optimized propagation delay between control signal and power MOSFET gate (typ 200 ns)

The isolated switched mode power supply is a regulated flyback DC-DC converter providing both isolated gate drivers with the positive and negative supply voltages required to drive the different types of FETs. The DC-DC converter function is fully integrated in CHT-HADES2P device. It provides as well high voltage isolation between the 2 channels and high dV/dt immunity. The converter also generates a 5V supply for the control interface at the primary side.
The DC-DC converter features a cycle-by-cycle current monitoring loop (shunt based measurement) with a current limit set at 1000mA typ. and a regulation based on a rectified third winding output fed back to the PWM controller.

The Local Non-Overlapping Management block enables EVK-HADES1210 to work in 2 different modes:

- The Local mode where two internal non-overlapped PWM signals are generated from a single external PWM (PWM_H) input signal. The non-overlapping delay is implemented through a on-board capacitor and so can easily be adapted.
- The Direct mode where the two internal PWM signals are a direct copy of the PWM_H/PWM_L inputs signals. Required non-overlapping must then controlled externally to EVK-HADES1210.

The two 10A 1200V power switches are implemented with CHT-NEPTUNE devices which can be used up to 225°C junction temperature, enabling reduction of cooling system size.

Evaluation Kit Deliverables

The Evaluation Kit includes the following deliverables

- A detailed Application Note
- The evaluation board
- The complete electrical schematic
- The bill of materials (BOM) including active and passive components
- The layout as Gerber files

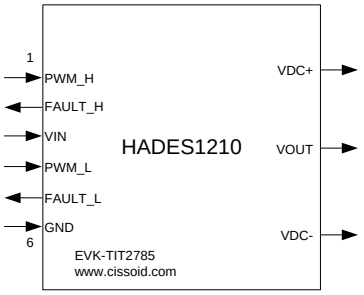
The **Application Note is available on request** on CISSOID Website.

Document References

- CHT-HADES2P - High Temperature Gate Driver Primary Side IC: DC-DC Controller & Isolated Signal Transceivers - Datasheet
- CHT-HADES2S - High Temperature Gate Driver - Secondary Side IC:Driver & Protection Functions - Datasheet
- CHT-ELARA - 80V High Temperature Quad Diode - Datasheet
- CHT-NEPTUNE – 1200V/10A Silicon Carbide MOSFET – Datasheet

IO Description

PWM_H	High-side PWM control signal
FAULT_H	High-side fault
VIN	Positive supply
PMW_L	Low-side PWM control signal
FAULT_L	Low-side fault
GND	Ground
VDC+	Positive power DC bus voltage
OUT	Output to high-side gate
VDC-	Negative power DC bus voltage



VIN	**Positive supply** All other power supplies for driving the gate of the FETs are internally generated by the on-board DC-DC converter
GND	**Ground** Reference ground for the supply and the digital IOs.
PWM_H	**Input control signal for the high-side driver** The signal controls the state of the high-side FET. PWM_H=15V turns the high-side FET on. PWM_H=0V turns the high-side FET off. When in Local mode (selection by jumper), this signal control both low-side and high-side channels in opposite states with some internally defined non-overlapping delay.
FAULT_H	**High-side channel fault output** This signal combines: - The high-side secondary Desaturation fault - The high-side secondary UVLO fault - The primary fault. In case of fault, FAULT_H is set to “0V” for a duration equal to internal timer defined at EVK board level by capacitors; those timer values can be adapted by changing the capacitor value. In normal operation, FAULT_H=15V. In case of fault, FAULT_H =0V.
PWM_L	**Input control signal for the low-side driver** The signal controls the state of the low-side FET. PWM_L=15V turns the low-side FET on. PWM_L=0V turns the low-side FET off. When in Local mode (selection by jumper), this PWM_L signal has no effect, the low-side FET being control by PWM_H and the local non-overlap function.
FAULT_L	**Low-side channel fault output** This signal combines: - The low-side secondary Desaturation fault - The low-side secondary UVLO fault - The primary fault. In case of fault, FAULT_L is set to “0V” for a duration equal to internal timer defined at EVK board level by capacitors; those timer values can be adapted by changing the capacitor value. In normal operation, FAULT_L=15V. In case of fault, FAULT_L =0V.
VDC+	**Power positive DC BUS signal**
VOUT	**Half-Bridge power mid-point output**
VDC-	**Power negative DC BUS signal**

Absolute Maximum Ratings

Stressing the board above these absolute maximum ratings could present permanent damage. Exposure to this maximum rating for extended periods may affect the board reliability. These ratings are considered individually (not in combination). If not specified, voltages are related to GND

Parameter	Min.	Max.	Units
(VIN-GND)	-0.5	16.5	V
Voltage on PWM_L, PWM_H, FAULT_L, FAULT_H (wrt to GND)	-0.5	16.5	V
"VDC+" – "VDC-"		600	V
VOUT	-0.5	600	V
Steady Operating Temperature	-55	175	°C

Electrical Characteristics

Unless otherwise stated: T_j=25°C. **Bold underlined** values indicate values valid over the whole temperature range (-55°C < T_a < +175°C).

Parameter	Condition	Min	Typ	Max	Units
External Power Supply					
External Power Supply VDD	Versus GND	13.5		16.5	V
I_{AVG}(VIN)	VIN=15V, PWM_L=0, PWM_H=0 No fault situation Direct Mode		90		mA
	VIN=15V; 100 kHz; 50% Duty-Cycle No fault situation Direct Mode		164		mA
Internal Secondary supplies					
Low-side channel positive supply Voltage (VDD_L)	To NS_L -55°C ≤T_a ≤ 175°C		20.3		V
Low-side channel negative supply Voltage (VSS_L)	To NS_L -55°C ≤T_a ≤ 175°C		-5.13		V
High-side channel positive supply Voltage (VDD_H)	To NS_H -55°C ≤T_a ≤ 175°C		19.9		V
High-side channel negative supply Voltage (VSS_H)	To NS_H -55°C ≤T_a ≤ 175°C		-5.1		V

Isolation					
Inter channel Isolation I_{H2L}	NS_H To NS_L -55°C ≤T_a ≤ 175°C	2.5			kV
Low-side channel isolation I_{L2P}	NS_L To GND -55°C ≤T_a ≤ 175°C	50			V
High-side channel isolation I_{H2P}	NS_H to GND -55°C ≤T_a ≤ 175°C	2.5			kV
Maximum supported dV/dt	NS_H to NS_L NS_H to GND (guaranteed by design)			50	kV/µs

Electrical Characteristics

Unless otherwise stated: T_j=25°C. **Bold underlined** values indicate values valid over the whole temperature range (-55°C < T_a < +175°C).

Parameter	Condition	Min	Typ	Max	Units
PWM_L/PWM_H inputs					
HIGH voltage threshold for digital inputs	Applies to PWM_L/PWM_H Percentage of VDDIO JP1="1-2": VDDIO = VIN JP1="3-2": VDDIO = 5V		66		%
LOW voltage threshold for digital inputs			33		%
Hysteresis			33		%
Input impedance	Applies to PWM_L/PWM_H	**47**			kΩ
FAULT_L/FAULT_H open drain outputs					
On resistance	Applies to **FAULT_L/FAULT_H**			**25**	Ω
Internal pull-up resistor			10		kΩ
Output Fall Time (90% to 10%)	On 50 pF external capacitor External pull-up: 300 Ohm to VIN		36		ns
Non-overlap delay (NOV_D)					
Non Overlap delay HIGH => LOW	In Local Mode Measured at power switch gate		400		ns
Non Overlap delay LOW => HIGH			350		ns
Half-Bridge power mid-point (VOUT)					
Rise time	Cfr Inductive switching tests section for details about test conditions		40		ns
Fall time			40		ns
PWM data path					
PWM frequency				**200**	kHz
Duty cycle		**0**		**100**	%
PWM_L/PWM_H spike filter delay	If activated		500		ns
Propagation delay (PWM_L/PWM_H →OUT) (50% to 10%)	Spike filter not active Direct Mode		180		ns
Propagation delay (PWM_L/PWM_H →OUT) (50% to 10%)	Local Mode		600		ns
Fault latching time					
Timer value (Primary and Secondary faults)			14		ms
Timer variation		-30		+25	%

Under-voltage Lockout on VIN (UVLO_P)					
UVLO_P High Threshold			9.75		V
UVLO_P Low Threshold			8.2		V
Delay from UVLO_P detection to FAULT_L/FAULT_H @ fault level			200		ns
Under-voltage Lockout on (VDD_L-VSS_L)/ (VDD_H-VSS_H) (UVLO_S)					
UVLO_S High Threshold			21.7		V
UVLO_S Low Threshold			17.3		V
Delay from UVLO_S detection to FAULT_L/FAULT_H @ fault level			600		ns
Desaturation detection (DESAT_H, DESAT_L)					
DESAT_H/DESAT_L Threshold	DESAT_L/DESAT_H wrt to NS_L/NS_H		7.26		V
DESAT Blanking time			500		ns
Delay from DESAT_H/DESAT_L detection to FAULT_L/FAULT_H @ fault level			600		ns

Typical Performance Characteristics

Double Pulse Inductive switching tests

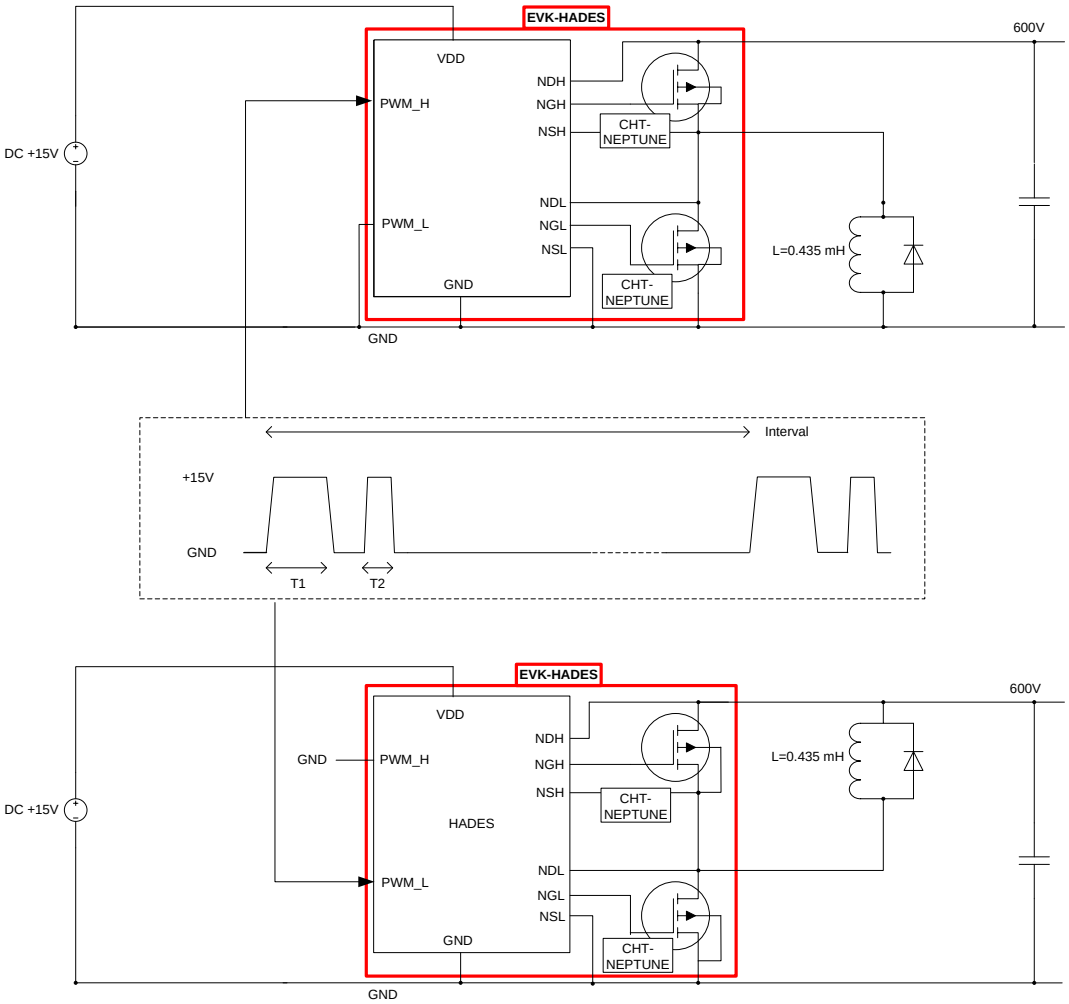


Figure 3: Application circuits for clamped inductive switching tests (top drawing: high-side test setup; bottom drawing: low-side test setup)

Typical Performance Characteristics (cnt'd)

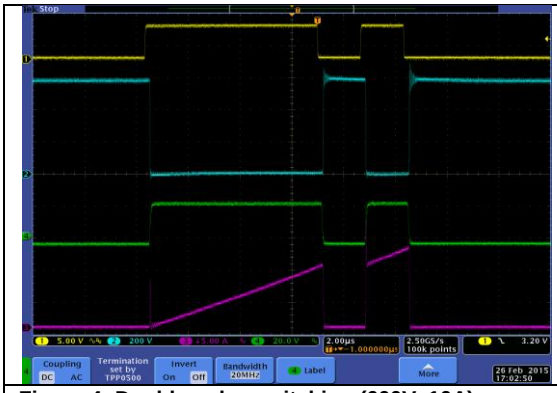


Figure 4: Double pulse switching (600V, 10A)
CH1=PWM_L, CH2=VOUT, CH3=I_{NDL}, CH4=NGL

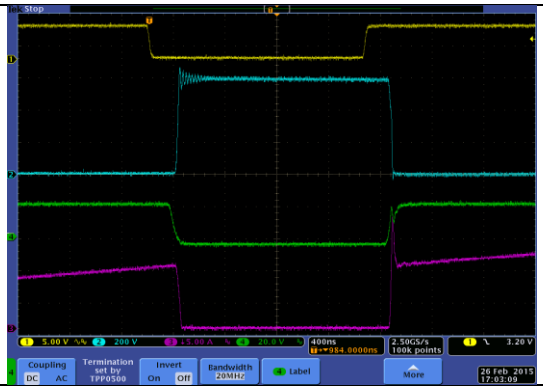


Figure 5: Double pulse switching (600V, 10A)
CH1=PWM_L, CH2=VOUT, CH3=I_{NDL}, CH4=NGL

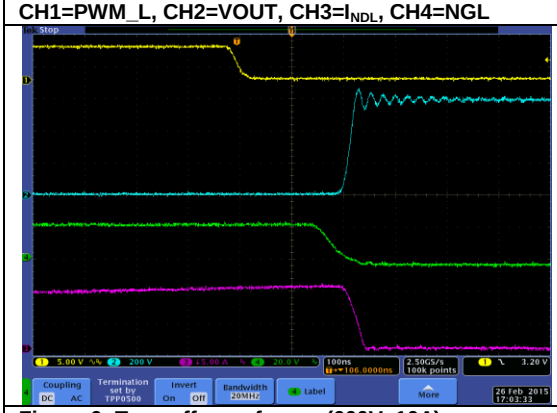


Figure 6: Turn-off waveforms. (600V, 10A)
CH1=PWM_L, CH2=VOUT, CH3=I_{NDL}, CH4=NGL

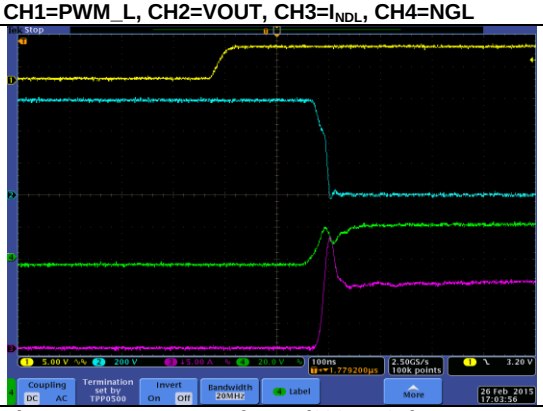


Figure 7: Turn-on waveform . (600V, 10A)
CH1=PWM_L, CH2=VOUT, CH3=I_{NDL}, CH4=NGL

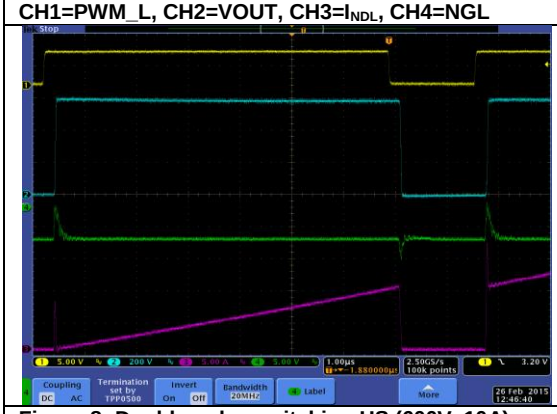


Figure 8: Double pulse switching HS (600V, 10A)
CH1=PWM_H, CH2=VOUT, CH3=I_{NSH}, CH4=NGL

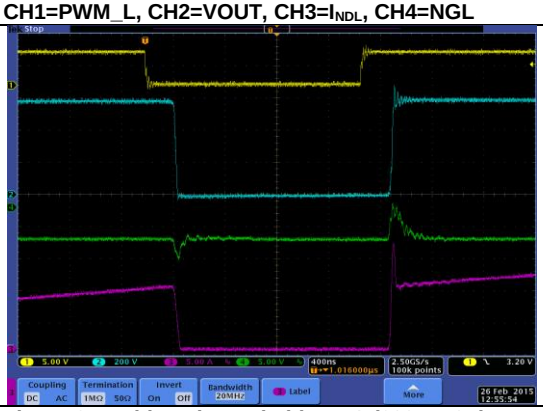


Figure 9 Double pulse switching HS (600V, 10A)
CH1=PWM_H, CH2=VOUT, CH3=I_{NSH}, CH4=NGL

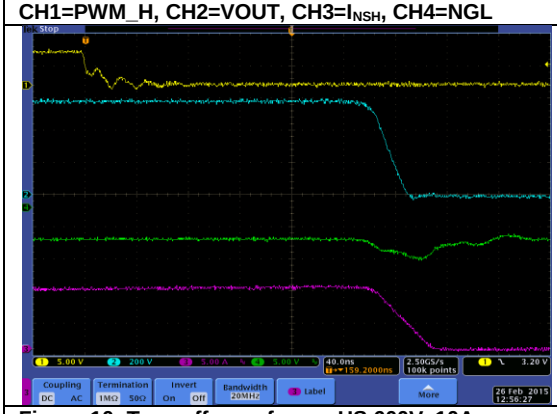


Figure 10: Turn-off waveforms. HS 600V, 10A.
CH1=PWM_H, CH2=VOUT, CH3=I_{NSH}, CH4=NGL

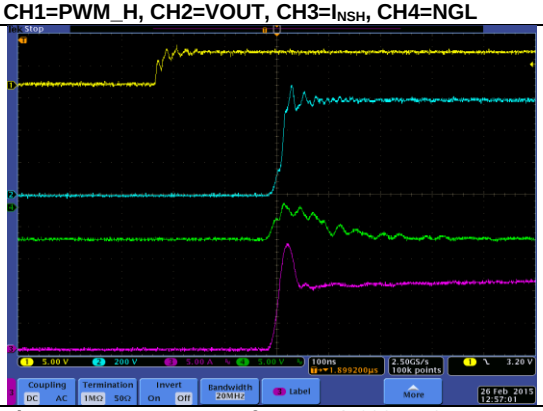


Figure 11: Turn-on waveforms. HS 600V, 10A.
CH1=PWM_H, CH2=VOUT, CH3=I_{NSH}, CH4=NGL

Typical Performance Characteristics (cnt'd)

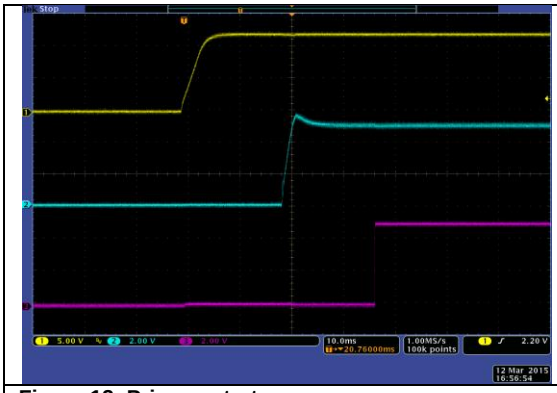


Figure 12: Primary start-up
CH1= VIN, CH2=AUX_REC, CH3=DOUTx

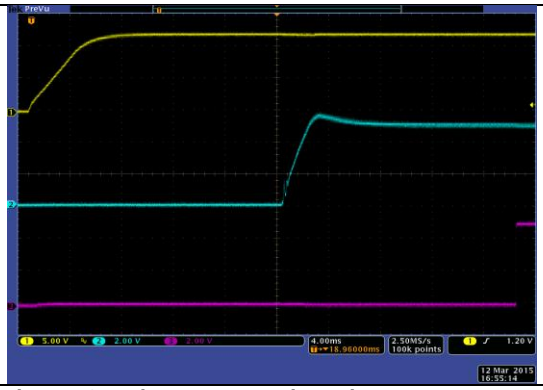


Figure 13 : Primary start-up (zoom)
CH1= VIN, CH2=AUX_REC, CH3=DOUTx

Typical Performance Characteristics (cnt'd)

Switching tests in a 3KW Buck DC-DC Converter

- PWM signals: 100kHz, 50% duty cycle
- DC bus voltage = 600V
- Output voltage = 300V
- Output current = 10A
- Local non-overlap: 400 ns

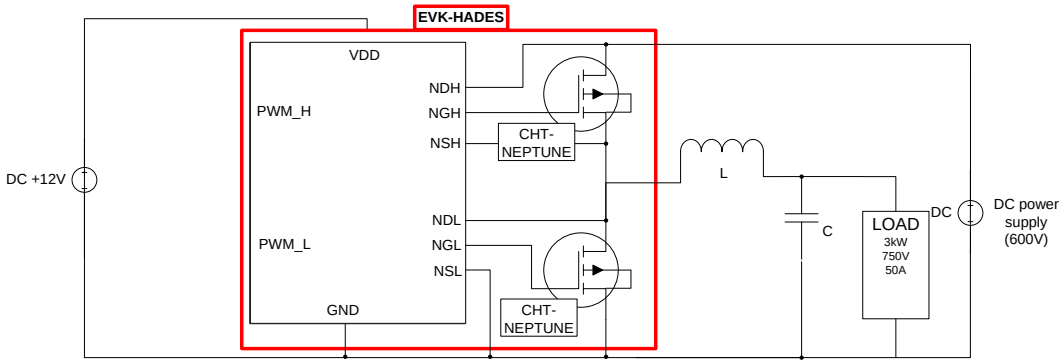


Figure 14: Buck DC-DC converter

Figure 15: DC-DC operation at 100 kHz

(CH1: PWM_L, CH3: half-bridge output voltage, CH4: Iload)

Ordering Information

Product Name	Ordering Reference	Package	Marking
EVK-HADES1210	EVK-TIT2785A	NA	EVK-TIT2785

Contact & Ordering

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