EVK-HADES®

Version: 1.0

Half-Bridge Isolated Gate-Driver for High-Reliability and High-Temperature Applications

Reference Design & Evaluation Board

Application Note

General description

HADES® is CISSOID' complete half-bridge gate driver Reference Design for extended lifetime, high reliability and high temperature applications. The design has been optimized to drive the newest generation of wide-bandgap devices such as SiC and GaN power switches (e.g. MOSFETs,JFETs, etc.). The HADES® Evaluation Board EVK-TIT0636B is a turnkey isolated gate driver board that can be used immediately to drive normally-Off power JFETs (P/N SJEP120R100) from Semisouth Laboratories.

Overall, HADES® combined with the power JFETs can quickly implement the core of the power converter, supporting a bus voltage up to 600V / 1200V and gate currents up to ±2A. The two channels can be controlled independently of each other or used in a half-bridge configuration. EVK-HADES® board in combination with power switches can form a complete 1-leg inverter solution for immediate evaluation.

The Reference Design is based on the chipset CHT-THEMIS/CHT-ATLAS and CHT-RHEA. The solution also includes an isolated power supply built with CHT-MAGMA PWM controller. For applications that require gate currents greater than ±2A, designers can modify HADES® reference design and build their own board by adding up to 4 four additional CHT-ATLAS circuits per channel (high-side and low side) in order to sink / source up to ±10A to the gate of the power switch devices.

The Evaluation Board is populated with CISSOID integrated circuits in ceramic package and metal can forms (CSOIC16/CSOIC28 and TO18), guaranteed for -55°C to +225°C. The board is based on a polyimide PCB (rated 200°C). The passive components and the desaturation diode allow operation up to 175°C, with possible short excursions to 225°C for testing. The evaluation board is delivered with the complete electrical schematic, the bill of materials including active and passive components, the Gerber files.

Features

- CISSOID Active components guaranteed for -55° to +225°C (Tj)
- 200°C Polyimide PCB
- Board qualified for 175°C ambient
  - Short excursions to 225°C for testing allowed
- High-side and Low-side gate driver
- DC Bus voltage: 600V Typ.[1] (designed for 1200V max)
- Gate output current ±2A
- Isolation (primary – secondary):
  - 2,500VAC @50Hz (for 1mn)
  - >100MΩ @ 500VDC
- Common mode transient immunity:
  - 30kV/µs Typ. [1] (designed for 50kV/µs)
- Delay time (PWM to NGH/NGL)): 200ns typ.
- Gate voltage: +16V / -16V nominal
- Rise time (on a 1nF):20ns Typ.
- Fall time (on a 1nF): 20ns typ.
- Switching frequency: 150kHz Typ.
- Single power supply: +12V ±10%
- Interfacing voltage (digital I/Os): 5V ±10%
- Under voltage lockout (UVLO)
- Independent PWM inputs for HS and LS drivers or single PWM input with on-board non-overlapping
- Active Miller clamping
- Desaturation protection
- Isolated fault outputs

Applications

- General purpose Isolated MOSFET/JFET gate drives
- Motor drives
- Battery chargers
- Power Conversion:
  - AC-DC converters
  - DC-DC converters
  - DC-AC inverters

For:

- Renewable energies
- Smart grid
- HEV / EV
- Railways & Transportation
- Industrial Motor Drives
- Aerospace
- Oil & Gas down-hole tools

[1] Typical values are tested values while the max design values were untested.

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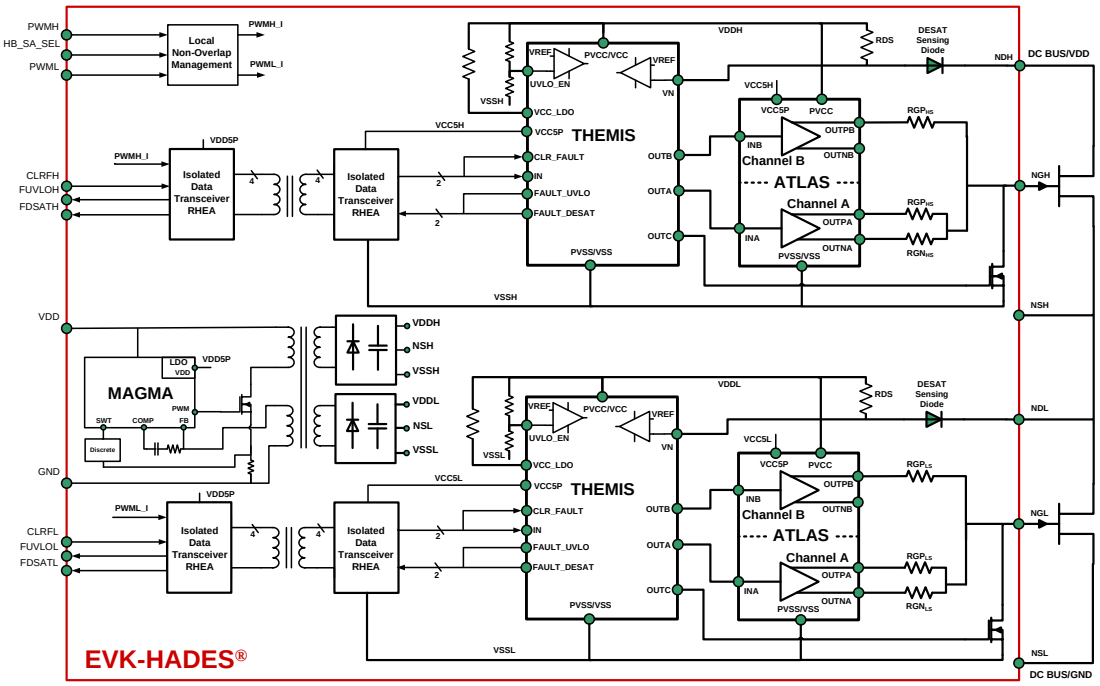


Figure 1: EVK-HADES High Level Block Diagram

EVK-HADES implements 4 main functions, 2 isolated gate drivers, an isolated switched mode power supply and a Local Non-Overlapping Management block.

The 2 isolated gate drivers are identical; they are based on the CISSOID TITAN chipset (CHT-RHEA, CHT-THEMIS, CHT-ATLAS) and each of them provides following functionalities:

- 2A peak gate drive current
- Monitoring and fault reporting of the gate driver power supplies (UVLO) (threshold is programmable via on-board resistances)
- Cycle-by-cycle Desaturation monitoring and fault reporting (DESAT) (immediate FET turn-off in case of desaturation detection); blanking time is programmable via a capacitance
- Fully isolated control (PWM, Clear_Fault) and fault (Fault_Desat, Fault_Uvlo) signals between EVK-HADES external connections and gate driver signals
- Active Miller Clamp function protecting the power FET from parasitic turn-on; an external high temperature 40V MOSFET driven by CHT-THEMIS OUTC output signal is clamping the gate just after Power MOSFET turn-off.
- Optimized propagation delay between control signal and power FET gate (typ 200 ns)

The isolated switched mode power supply is a regulated fly back DC-DC converter providing both isolated gate drivers with the positive and negative supply voltages required to drive the

different types of FETs. It is based on the CISSOID CHT-MAGMA PWM controller. It provides as well high voltage isolation between the 2 channels and high dV/dt immunity. The converter also generates a 5V supply for the control interface at the primary side.
The DC/DC converter features a cycle-by-cycle current monitoring loop (shunt based measurement) with a current limit set at 600mA and a voltage regulation based on a rectified third winding output fed back to the PWM controller.
Considering the large variety of FET devices and their associated control voltage requirements, the EVK-HADES power supply design is adaptable to the various voltage levels with minimal changes (typically component change in the feedback loop and transformer design changes).

The Local Non-Overlapping Management block enables EVK-HADES to work in 2 different modes:

- The Half-Bridge mode (HS_SA_SEL = 5V) where 2 internal non-overlapped PWM signals are generated from a single external PWM input signal. The non-overlapping delay is implemented through an RC network and so can easily be adapted by changing eg the value of the capacitance
- The Direct mode (HS_SA_SEL = 0V) where the 2 internal PWM signals are a direct copy of the PWMH/PWML inputs signals. Required non-overlapping must then controlled externally to EVK-HADES.

Document References

CHT-THEMIS: Power Transistor Driver Controller
Datasheet: http://www.cissoid.com/images/stories/pdf/Datasheets/CHT-THEMIS.pdf

CHT-ATLAS: Dual Channel Power Transistor Driver
Datasheet: http://www.cissoid.com/images/stories/pdf/Datasheets/CHT-ATLAS.pdf

EVK-THEMIS-ATLAS: Power Transistor Driver Evaluation Kit
Datasheet: http://www.cissoid.com/images/stories/pdf/ApplicationNotes/EVK-THEMIS-ATLAS-Application%20Note.pdf

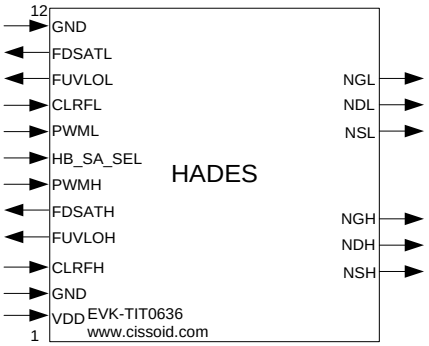
CHT-RHEA: 2Mbps, Dual-Channel Isolated Transceiver
Datasheet: http://www.cissoid.com/images/stories/pdf/Datasheets/cht-rhea.pdf

EVK-RHEA: Evaluation Kit : 4 channels, 2MBps Isolated Data link
Datasheet: http://www.cissoid.com/images/stories/pdf/ApplicationNotes/EVK-RHEA-Evaluation%20Board-AN.pdf

CHT-MAGMA: PWM Controller
Datasheet: http://www.cissoid.com/images/stories/pdf/Datasheets/cht-magma.pdf

IO Description

VDD	Positive supply
GND	Ground
CLRFH	HS clear fault
FUVLOH	HS under-voltage lock-out fault
FDSATH	HS desaturation fault
PWMH	High-side control signal
HB_SA_SEL	HB single control signal mode
PMWL	Low-side control signal
CLRFL	LS clear fault
FUVLOL	LS under-voltage lock-out fault
FDSATL	LS desaturation fault
GND	Ground
NSH	High-side source connection
NDH	High-side drain connection
NGH	Output to high-side gate
NSL	Low-side source connection
NDL	Low-side drain connection
NGL	Output to low-side gate



VDD	**Positive supply** All other power supplies for driving the gate of the FETs are internally generated by the on-board DC-DC converter
GND	**Ground** Reference ground for the supply and the digital IOs.
CLRFH	**High-side channel fault reset input** CLRFH transition from 0V to 5V resets fault flag in the high-side channel (FDSATH)
FUVLOH	**High-side channel under-voltage fault output** The same function as FUVLOL but for the high-side channel
FDSATH	**High-side channel desaturation fault output** Same function as FDSATL but in the high-side channel
PWMH	**Input control signal for the high-side driver** The signal controls the state of the high-side FET. PWMH=5V turns the high-side FET on. PWMH=0V turns the high-side FET off. When signal HB_SA_SEL=5V, this PWMH signal has no effect, the high-side FET being control by PWML.
HB_SA_SEL	**Direct or Half-Bridge Mode input** In direct mode HB_SA_SEL=0V, the two channels are controlled by independent control signals PWML, PWMH. In Half-Bridge mode, both channels are controlled into opposite states by a same PWML with internally defined non-overlapping between high and low side.
PWML	**Input control signal for the low-side driver** The signal controls the state of the low-side FET. PWMH=5V turns the low-side FET on. PWMH=0V turns the low-side FET off. When signal HB_SA_SEL=5V, this signal control both low-side and high-side channels in opposite states with some internally defined non-overlapping delay.
CLRFL	**Low-side channel fault reset input** CLRFL transition from 0V to 5V resets the desaturation fault flag in the low-side channel (FDSATL)
FUVLOL	**Low-side channel under-voltage fault output** The DC-DC converter provides the low-side channel with positive and negative supply voltages for proper drive of the power FET. The channel returns an under-voltage fault when internal channel supply is below the under-voltage lock-out threshold. In normal operation, FUVLOL=5V. In case of fault, FUVLOL=0V.
FDSATL	**Low-side channel desaturation fault output** When the low-side FET is in ON-state, its drain voltage is monitored for desaturation detection. In normal operation FDSATL=5V. In case of fault FDSATL=0V
NDH, NGH, NSH	**Drain, gate and source connections of the high-side FET**
NDL, NGL, NSL	**Drain, gate and source connections of the low-side FET**

Absolute Maximum Ratings

Stressing the EVK above these absolute maximum ratings could present permanent damage. Exposure to this maximum rating for extended periods may affect the EVK reliability. These ratings are considered individually (not in combination). If not specified, voltages are related to GND

Parameter	Min.	Max.	Units
(VDD-GND)	-0.5	15	V
Voltage on PWML, PWMH, HB_SA_SEL, CLRFH, CLRFL (wrt to GND)	-0.5	5.5	V
Steady Operating Temperature	-55	175	°C

The user should carefully read the "Start-up procedures" section before powering up EVK-HADES to avoid any board damage.

Electrical Characteristics

Unless otherwise stated: T_j=25°C. **Bold underlined** values indicate values valid over the whole temperature range (-55°C < T_a < +175°C).

Power Supplies

Parameter	Condition	Min	Typ	Max	Units
External power supply					
External Supply Voltage VDD	To GND	10.8	12	13.2	V
Quiescent external supply current IDD_q	VDD=12V, Low-side OFF, high side OFF		240		mA
Dynamic external supply current IDD_d	VDD=12V Capacitive load (1nF) on NGH/NGL, 50% duty cycle, 100kHz		290		mA

Parameter	Condition	Min	Typ	Max	Units
Internal power supply (SiC JFET version)					
Low-side channel positive supply Voltage VDDL	To NSL -55°C ≤T_a ≤ 175°C		+16		V
Low-side channel negative supply Voltage VSSL	To NSL -55°C ≤T_a ≤ 175°C		-16		V
High-side channel positive supply Voltage VDDH	To NSH -55°C ≤T_a ≤ 175°C		+16		V
High-side channel negative supply Voltage VSSH	To NSH -55°C ≤T_a ≤ 175°C		-16		V
Digital 5V supply for the IOs VDD5P	To GND -55°C ≤T_a ≤ 175°C	4.5	5	5.5	V

Parameter	Condition	Min	Typ	Max	Units
Isolation					
Inter channel Isolation I_{H2L}	NSH To NSL -55°C ≤T_a ≤ 175°C	1.2			kV
Low-side channel isolation I_{L2P}	NSL To GND -55°C ≤T_a ≤ 175°C	50			V
High-side channel isolation I_{H2P}	NSH to GND -55°C ≤T_a ≤ 175°C	1.2			kV
Maximum dV/dt	NSH to NSL NSH to GND (guaranteed by design)			50	kV/µs

Output

Parameter	Condition	Min	Typ	Max	Units
Output Voltage (SiC JFET version)					
Channel driver output voltage VOUTL (VOUTH)	NGL (FET_G_H) To NSL (NSH) -55°C ≤T_a ≤ 175°C	-16		+16	V
Channel driver output peak current IOUTL (IOUTH)	**On-board gate resistance = 3.3Ω** Pure capacitive load, no FET connected -55°C ≤T_a ≤ 175°C			2	A
Output voltage rise time T_{ro}	T_a=25°C **On-board gate resistance = 3.3Ω** Pure capacitive load=1nF, no FET connected		20		ns
Output voltage fall time T_{fo}	T_a=25°C **On-board gate resistance = 3.3Ω** Pure capacitive load=1nF, no FET connected		20		ns

Digital IOs

Parameter	Condition	Min	Typ	Max	Units
Input voltage range $\mathbf{V_{di}}$	To GND -55°C ≤T_a ≤ 175°C	0		5	V
Minimum HIGH level input voltage $\mathbf{V_{IH}}$	To GND -55°C ≤T_a ≤ 175°C	3.85			V
Maximum LOW level input voltage $\mathbf{V_{IL}}$	To GND -55°C ≤T_a ≤ 175°C			1.4	V
Minimum HIGH level output voltage $\mathbf{V_{OH}}$	To GND; Output source current < 8mA -55°C ≤T_a ≤ 175°C	4.4			V
Maximum LOW level output voltage $\mathbf{V_{OL}}$	To GND; Output sink current < 8mA -55°C ≤T_a ≤ 175°C			0.63	V
Output rise/fall time $\mathbf{T_{rfo}}$	50pF load capacitance		3		ns

Timing

Parameter	Condition	Min	Typ	Max	Units
Propagation delay PWML to G_FETL in direct control mode T_{dpdl}	Direct control mode (HB_SA_SEL=0) Driving SemiSouth SJEP120R100 (600V, 10A) (50%→ 50%) -55°C ≤T_a ≤ 175°C			200	ns
Propagation delay PWMH to G_FETH in direct control mode T_{dpdh}	Direct control mode (HB_SA_SEL=0) Driving SemiSouth SJEP120R100 (600V, 10A) (50%→ 50%) -55°C ≤T_a ≤ 175°C			200	ns
Non-overlapping time in HB control mode T_{nov}	HB control mode (HB_SA_SEL=5V) -55°C ≤T_a ≤ 175°C Default value, can be adjusted by changing RC time constant		400		ns
Propagation delay PWML to G_FETL in HB control mode T_{dhdl}	HB control mode (HB_SA_SEL=5V) Driving SemiSouth SJEP120R100 (600V, 10A) (50%→ 50%) -55°C ≤T_a ≤ 175°C		600		ns
Propagation delay PWMH to G_FETH in HB control mode T_{dhdh}	HB control mode (HB_SA_SEL=5V) Driving SemiSouth SJEP120R100 (600V, 10A) (50%→ 50%) -55°C ≤T_a ≤ 175°C		600		ns
Active Miller Clamp delay T_{amc}	T_a=25°C		313		ns
Desaturation blanking time T_{bl}	T_a=25°C		626		ns

Typical Performance Characteristics

Power supply performance

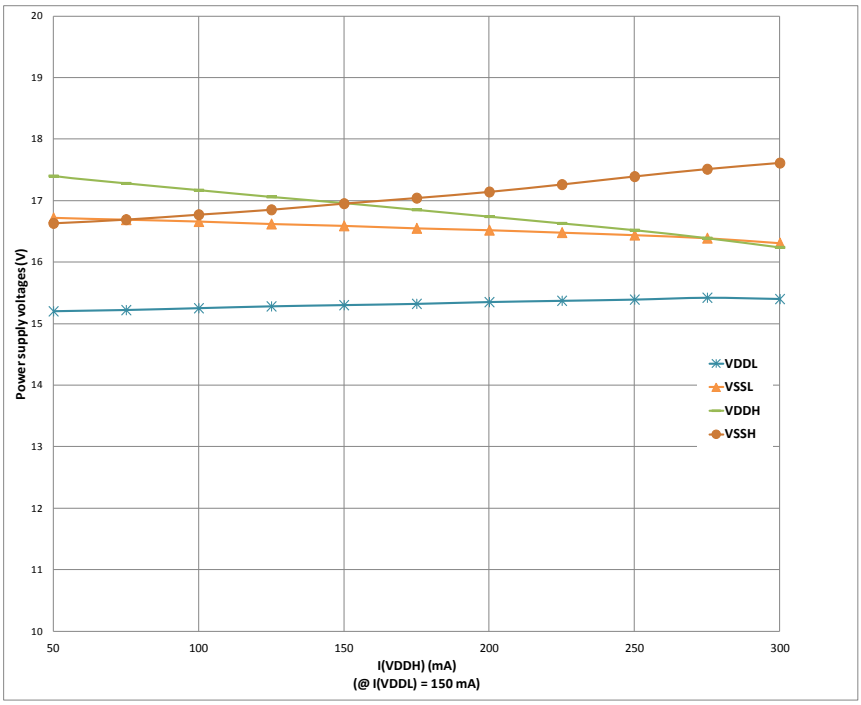


Figure 2: Channel supply voltages

Inductive switching tests

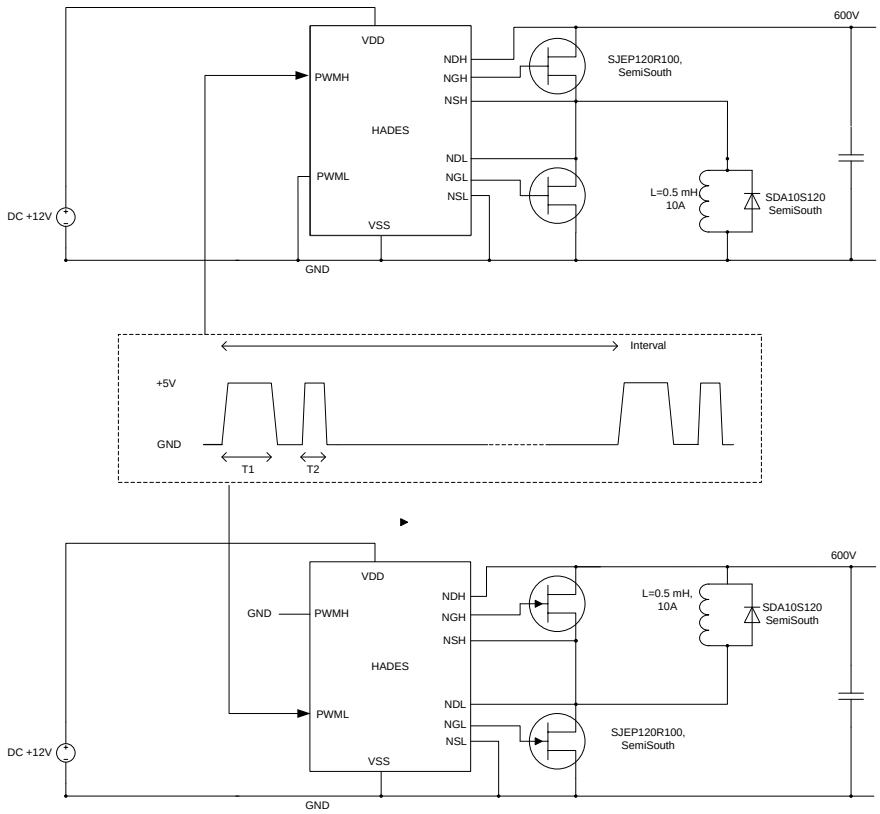


Figure 3: Application circuits for clamped inductive switching tests (top drawing: high-side test setup; bottom drawing: low-side test setup)

Test Conditions

- Driving SemiSouth SJEP120R100
- 0.5 mH Inductor
- SemiSouth SDA10S120 freewheeling diode
- 600V high voltage
- CLRFH = CLRFL = GND
- VDD=12V

Gate driver switching waveforms

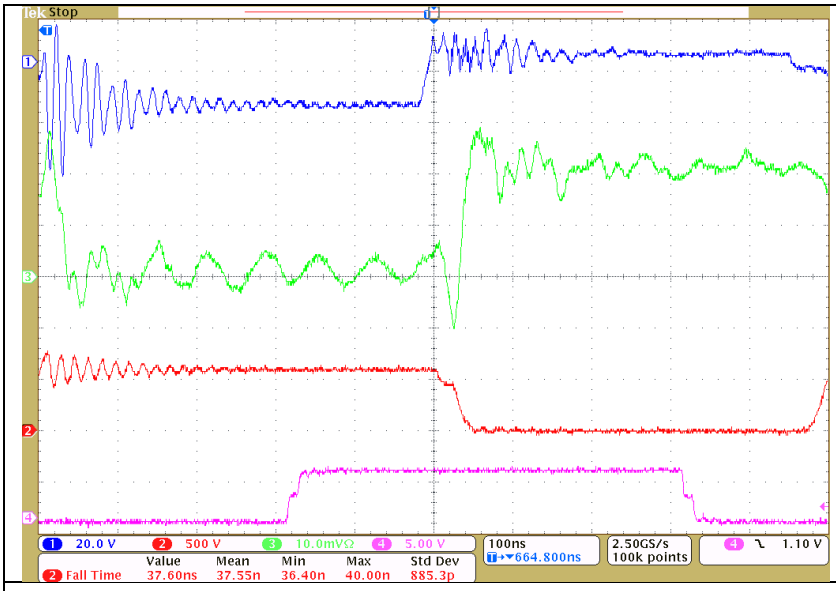


Figure 4: Low-side turn-on waveforms (600V, 10A)
CH1=NGL voltage (20V/div),CH2= NDL current (5A/div)
CH3=NDL voltage vs. NSL (500V/div),CH4= PWM voltage (5V/div)

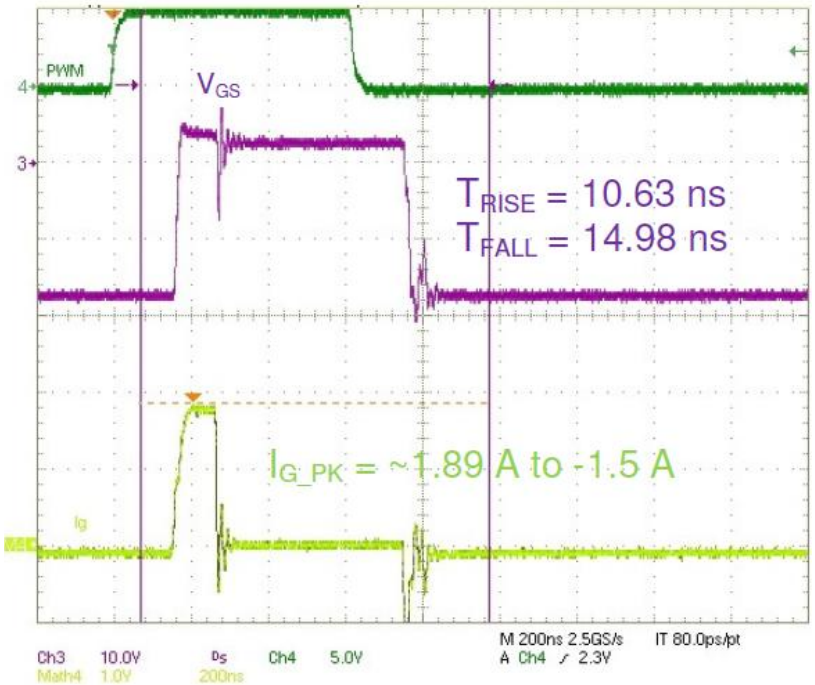


Figure 5: Details on low-side turn-on waveforms

Turn-on and turn-off transients of the half bridge

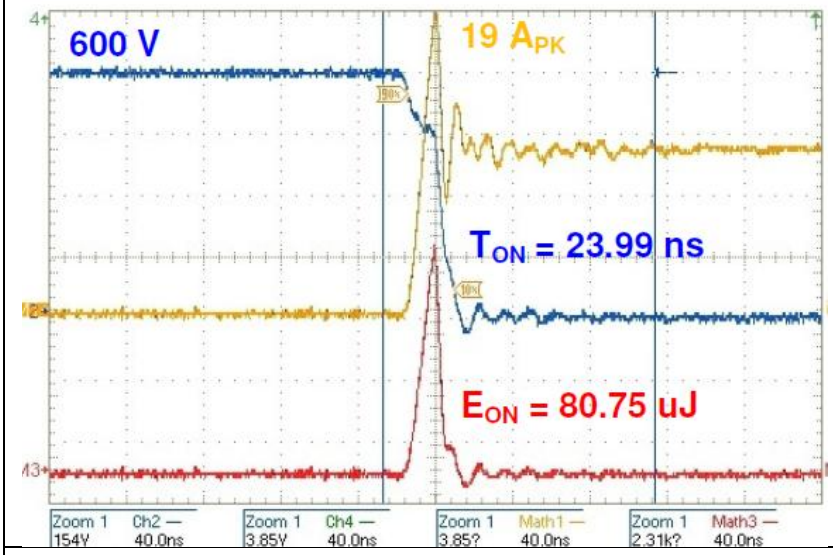


Figure 6: Turn-on energy loss (low-side). 600V, 10A

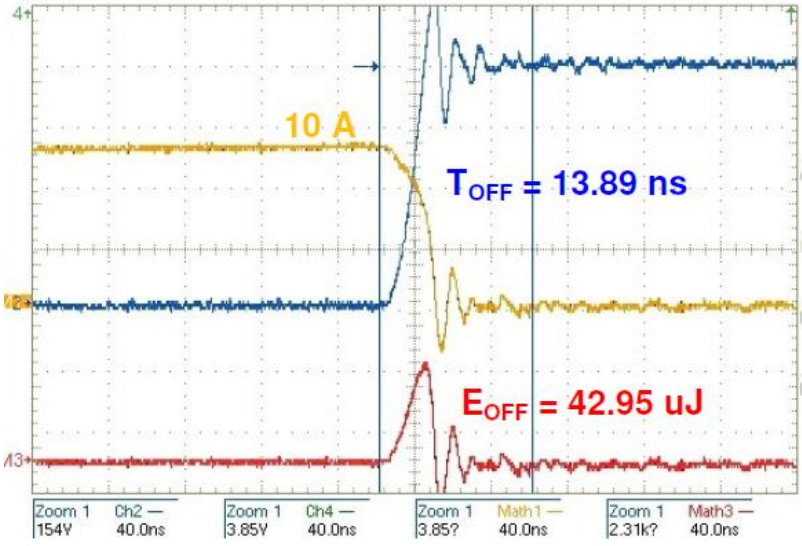


Figure 7: Turn-off energy loss (low-side). 600V, 10A

Circuit Functionality

Description

CHT-HADES is a two channel gate driver based on Cissoid chipset CHT-RHEA, CHT-THEMIS and CHT-ATLAS for high temperature, high reliability power FET gate drive. Those are used in combination with a specific isolated DC-DC converter designed around CHT-MAGMA.

The system is able to drive Normally-Off JFET power devices.

The isolation of the control signals is achieved via pulse transformers driven by CHT-RHEA.

CHT-ATLAS offers the high current gate drive with the appropriate gate levels generated by the DC-DC converter.

CHT-THEMIS handles the control signals it receives from CHT-RHEA and drives CHT-ATLAS accordingly. CHT-THEMIS offers desaturation fault detection/protection and under-voltage lock-out. It also features active Miller clamping.

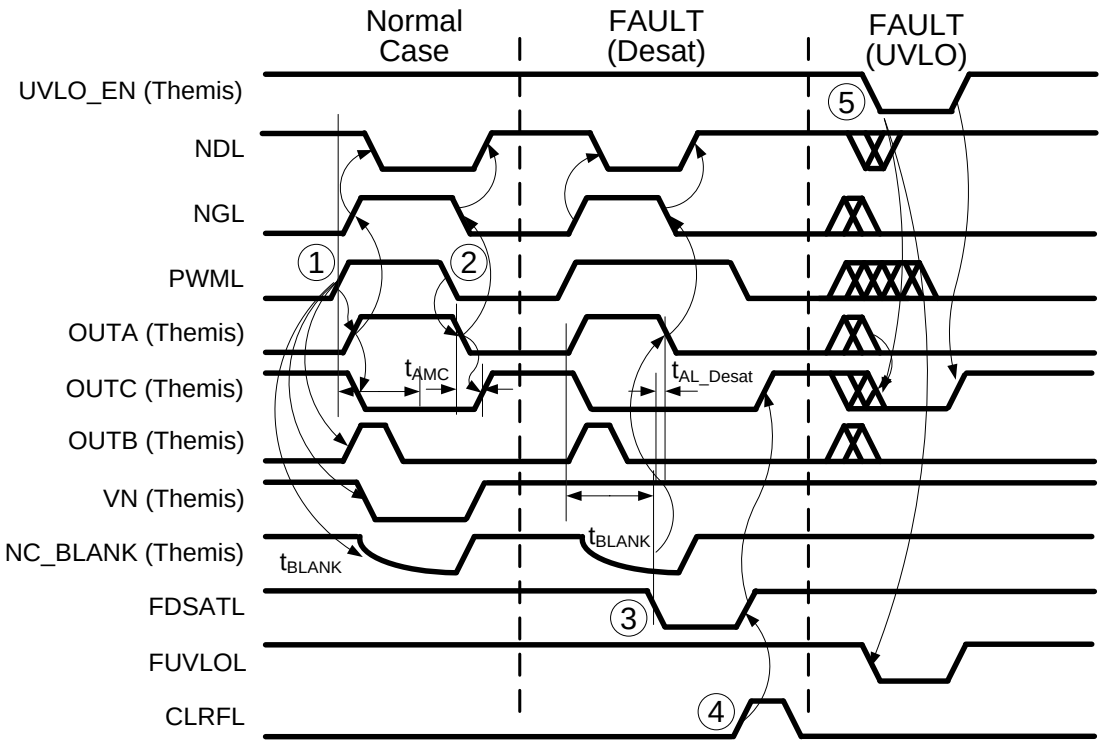


Figure 8: Timing diagram HADES low-side driver behaviour

Dynamic behavior

Figure 8 illustrates the HADES low-side driver dynamic behavior in normal operation and fault conditions.

In Normal operation,

on PWML rising edge (1), rising edge is generated on OUTA (after propagation delay through CHT-RHEA and CHT-THEMIS) and then, rising edge is generated on NGL (after propagation delay through CHT-ATLAS); a short pulse is generated on OUTB to turn on the JFET; finally a falling edge is generated on OUTC to deactivate the Active Miller Clamp transistor.
After rising edge on NGL, the power device is turned ON and NDL node is going to “0” state (voltage equals to Ron * current flowing through the power device). VN node is also pulled down and after blanking time (t_{BLANK}), no DESAT fault is detected and FDSATL remains high.
After the short pulse generated by OUTB signal, a constant current is maintained through the JFET gate.

on PWML falling edge (2), falling edge is generated on OUTA (after propagation delay through CHT-RHEA and CHT-THEMIS) and then, falling edge is generated on NGL (after propagation delay through CHT-ATLAS); a rising edge is generated on OUTC after t_{AMC} delay to activate the Active Miller Clamp transistor.
After falling edge on NGL, the power device is turned OFF.

In DESAT fault situation,

on PWML rising edge (3), rising edge is generated on OUTA (after propagation delay through CHT-RHEA and CHT-THEMIS) and then, rising edge is generated on NGL (after propagation delay through CHT-ATLAS); a short pulse is generated on OUTB to turn on the JFET; finally a falling edge is generated on OUTC to desactivate the Active Miller Clamp transistor.
After rising edge on NGL, the power device is turned ON; as a consequence of a DESAT fault, NDL and VN nodes are not going to their normal "0" state. Thanks to the DESAT comparator, CHT-THEMIS detects this fault situation and turns off OUTA (and consequently NGL); power device is turned off. FDSATL signal is pulled down
A positive edge on CLRF (4) will clear the DESAT fault and enable again the transmission of PWML signal towards NGL.

In UVLO fault situation,

UVLO status is monitored inside CHT-THEMIS. When UVLO comparator (5) detects an under voltage situation, OUTA, OUTB and OUTC signals are tied to "0" state and FUVLOL signal is pulled down.
As soon as power supplies are above their UVLO threshold, FUVLOL is pulled up and normal operation is resumed inside CHT-THEMIS.
More details on the dynamic behaviour can be found in the CHT-THEMIS datasheet (http://www.cissoid.com/images/stories/pdf/Datasheets/CHT-THEMIS.pdf)

On-board isolated power supply

The on-board isolated power supply is a regulated flyback DC-DC converter providing both channels with the positive and negative supply voltages required to drive the power FETs. It offers high voltage isolation between the channels and high dV/dt sustainability. The converter also generates a 5V supply for the control interface at the primary side.
The DC/DC converter features 2 regulation loops:

- a cycle-by-cycle current monitoring loop (shunt based measurement); current limit is set at 600mA
- a voltage regulation based on a rectified third winding output.

For the JFET, VDDL/H and VSSL/H are +15V with respect to NSL/H.

Isolated control signals

CHT-HADES has independent PWM input signal, fault detection outputs and fault reset inputs in each channel.

Two instances of CHT-RHEA handle the transfer of the control signal between the interface and the isolated gate drive channels. The isolation is done by means of one pulse transformer on each data-line which provides outstanding reliability performance and ability to operate at high temperature.

The data transfer is designed in such a way that energy is transferred through the pulse transformers in normal operation (no fault). Whatever defect interrupting the energy transfer therefore sets a fault flag indicating whether under-voltage lock-out or desaturation detection.

Generation of PWM/PWMN signals

CHT-HADES offers 2 modes of operation:

- PWML and PWMH are generated independently outside CHT-HADES. In this case, proper non overlapping must be generated externally from HADES.
- PWML and PWMH are generated out of one input signal (PWML) and proper non overlapping timing is managed locally on CHT-HADES

The choice between those 2 modes of operation is made through the use of the control signal HB_SA_SEL.

Drivers Under-voltage lock-out

The supply voltages delivered to the channels by the DC-DC converters are monitored in each channel and compared to 2 thresholds.

V_{UHV} : the device operates as soon as the supply voltage (*VDDH/L-VSSH/L*) exceeds that threshold value.

V_{UVL}: the device stops operating when the supply voltage (*VDDH/L-VSSH/L*) drops below that threshold value.

The difference between those two thresholds defines the hysteresis.

Referring to Figure 22: Schematic: High side gate drive for the under-voltage lock-out component:

$$V_{UVL} = \frac{RUL1 + RUL3}{RUL3}\left(Vref - VSSH/L\right) = \frac{RUL1 + RUL3}{RUL3} 2.5 \pm 5\%$$

$$V_{UVH} = \frac{RUL1 + RUL3 // RULH}{RUL3 // RULH} 2.5 \pm 5\%$$

Choosing RUL3 and the 2 thresholds, RUL1 and RULH are calculated by:

$$RUL1 = RUL3 \frac{\left(V_{UVL} - 2.5\right)}{2.5}$$

$$RULH = \frac{2.5\,RUL1\;\;RUL3}{RUL3\,V_{UVH} - 2.5\left(RUL1 + RUL3\right)}$$

The under-voltage lock-out thresholds are the following for the different board versions:

	JFET (VSSH/L = -15V)
V_{UVH}	18V
V_{UVL}	17V
RUL3	19.6kΩ
RUL1	115kΩ
RULH	294kΩ

Desaturation Detection

Referring to Figure 22: Schematic: High side gate drive, the desaturation detection circuit is the following.

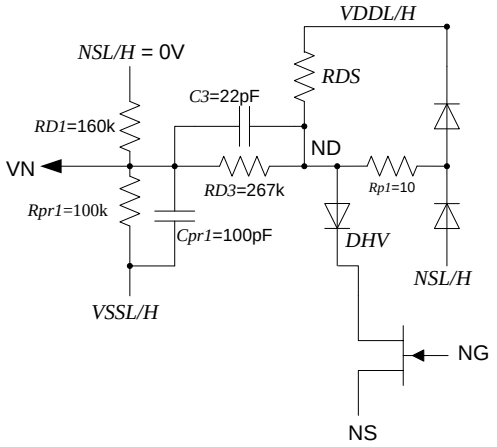


Figure 9: Desaturation detection circuit.

When the power FET device is conducting, a current for sensing de-saturation flows from *VDDL/H* through the power FET channel via resistor *RDS*.

In order to make the de-saturation threshold V(ND) independent from the supply voltage, *Rpr1*, *RD1* and *RD3* must be linked by the relationship *Rpr1 = RD1 // RD3*.
Choosing the drain de-saturation threshold voltage (sensed after the de-saturation diode DHV2) *V(ND)* = 6.6V and *Rp1r* = 100kΩ, component *RD1* and *RD3* can be dimensioned by the following rules

$$RD3 = \frac{Rpr1\,RD1}{RD1 - Rpr1}$$

$$RD1 = \frac{Rpr1\,\left(V(NS) - V(ND)\right)}{2\,Vref - V(VSS) - V(ND)}$$

With $Vref = \frac{V(ND) + V(VSS)}{2} + Iref\;\;Rref$

and $Iref\;\;Rref \approx 1.25V$

$$RD1 = \frac{Rpr1\,(V(ND) - V(NS))}{V(ND) - V(NS) - 2\,Iref\;Rref}$$

= 160 kΩ

$$RD3 = Rpr1\frac{(V(ND) - V(NS))}{2\,Iref\;Rref}$$

= 267 kΩ

Because of the independence from the supply voltage, the desaturation threshold remains unchanged as long as $VSSH/L$ is less than -2.7V.

Capacitors $Cpr1$ and $C3$ have been placed across resistors $Rp1r$ and $RD3$ in order to form a perfect voltage divider from ND to VN.

$$RD3 \cdot C3 = (Rpr1 // RD1) \cdot Cpr1$$

At large dV/dT, it is possible that the voltage at node ND drops below the actual drain voltage. The recovery is achieved through resistance RDS which could be made smaller in order to speed it up (at the expense of larger power dissipation).

Capacitor *Cbl* defines the so-called blanking time which is the delay allowing for settling of the voltage at the drain of the power transistor before actually detecting de-saturation at turn-on:

$$t_{BLANK} = 13333\;CBL$$

With *CBL* = 47pF, the blanking time is 626ns.

When a desaturation fault is detected by CHT-THEMIS, the fault signal is directly transmitted to the interface (the propagation delay of CHT-RHEA must be taken into account) while the FET is turned off with a delay of about 200ns.

JFET turn-on pulse

CHT-THEMIS offers the feature to control the length of the JFET turn-on pulse. This is done by selecting the value of xxx according to the following formula:

$$t_{PULSE} = 3333 * C_{PULSE}$$

In this implementation, a turn-on pulse width of 100ns has been chosen and so the value of the capacitance is 33pF. The measured turn-on pulse width value is slightly higher (140ns) than the planned 100ns.

Active Miller Clamp

The purpose of the Active Miller Clamping (AMC) feature is to avoid parasitic cross-conduction (positive kick on VGS) or punch-through (negative kick on VGS) during different switching phases in FET bridge arms (high/low side switches) in the context of power inverter application (see Figure 10).
Cross-conduction effect can happen with all types of FET devices while punch-through effect is more related to JFET devices.
These 2 effects are due to drain-to-gate coupling through the Miller capacitance of the FETs. They are further enhanced with the gate resistance which is necessary to kill the ringing effect due to parasitic inductances. The AMC provides a low impedance path, without series resistance, to maintain the gate voltage at its desired value to turn OFF the JFET properly with reduced risk of cross-conduction/punch-through. Figure 10 shows the cross-conduction and punch-through effects in a power inverter arm delivering positive current to an inductive load. In this case, the AMC feature in the low side driver provides a solution to significantly reduce the risk of cross-conduction/punch-through effects. Similarly, the same effects can be observed at the high side in the case of a power inverter arm delivering negative current.
For proper operation, the AMC delay (t_{AMC}) must be carefully adjusted and smaller than the non-overlapping delay between low and high side PWM inputs. This is made possible thanks to the external capacitor C_{AMC}.

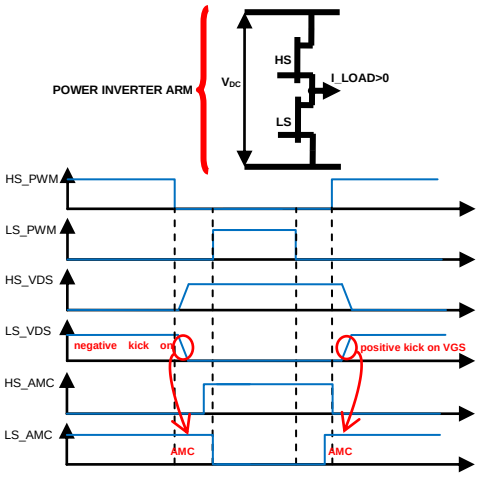


Figure 10. Cross-conduction and punch-through effects in a power inverter arm delivering positive current to an inductive load.

The active Miller clamp feature is controlled by CHT-THEMIS which controls the gate of a NMOS (CHT-MOON) to firmly tie node NGL/H to VSSL/H.

At turn-on of the power FET, the active Miller clamp NMOS is immediately turned off.

At turn-off of the power transistor, the Active Miller Clamp NMOS is activated after some delay defined by capacitor *Camc*.

$$t_{AMC}=6666\ Camc$$

With *Camc*=47pF, t_{AMC} delay is 313ns.

Data transmission transformer design

The data transmission transformer is part of the DATAFAB Zip file enclosed in the delivery.

Power supply transformer design

The power supply transformer is part of the DATAFAB Zip file enclosed in the delivery.

HADES board power dissipation

Current consumption of the HADES board for Normally-Off depends on the following system parameters:

- RGate used during turn-on pulse (R_g)
- Switching frequency (F_s)
- Duration of turn-on pulse (T_{on})
- JFET gate forward current (I_{gf})
- JFET total gate charge (Q_g)

$$Iin = 240mA_{typ} + 30mA_{typ} * Act$$
$$+ 0.0036 * Act * Qg * Fs$$
$$+ 1.78 * (Igf + 0.004 * Ton * Fs)$$

Where:

- Iin is the input current (wrt to Vin = 12V)
- Act is a Boolean (0: PWML/PWMH = 0, 1: PWML/PWMH alternating at Fs frequency)

The duty cycle of the PWML/PWMH signals has almost no influence on the current consumption of the HADES board (assuming that PWML and PWMH duty cycles are complementary).

To stay within specifications of the internal secondary voltages, the maximum Iin current is 700 mA.

Start-up procedures

Stand-Alone start-up

Before plugging the EVK-HADES in an application (DC/DC, 3-phase motor,…), CISSOID recommends that the EVK is being first tested in a configuration without any load (no power device, no external capacitance).
In this configuration, NSH/NSL nodes need to be connected to GND and NDH/NDL need to be connected respectively to NSH/NSL (to avoid desaturation detection).

VDD/GND should be connected to an external 12V power supply.

At power-up, with HB_SA_SEL = LOW (no external connected required since on-board pull-down is present on this signal and on PWML/PWMH), EVK-HADES will be in idle state:

- Current consumption should be around 156 mA
- NGH/NGL node should have a “0” level (-5V).

Then, still with HB_SA_SEL=LOW, independent external digital signals can be applied to PWMH/PWML; NGH/NGL waveforms should be identical (with a delay corresponding to the EVK-HADES propagation delay) to respectively PWMH/PWML with a voltage swing of ~25V.
Activation of HB_SA_SEL will generate internal non-overlapped signals from PWML; this can be verified by probing NGH/NGL signals.

Desaturation functionality can be checked by leaving NDH/NDL floating.

Once those checks have been done, EVK-HADES can be inserted in the customer application.

Application using EVK-HADES in Direct mode

In the Direct mode (HB_SA_SEL = LOW), PWML and PWMH are controlled independently of each other by external equipments.

User should take care of generating proper non-overlapping between PWML and PWMH; CISSOID recommends to start testing with min 1µs non-overlapping (this value can be then optimized based on measurement results).

Assuming an inductive load connected to the power FETs, user should apply an PWMH turn-on time compatible with the current drive capability of the high side power FET (to avoid blow-up of the power device).

Application using EVK-HADES in Half-Bridge mode

In Half-Bridge mode (HB_SA_SEL = 5V), PWML input is transformed internally in 2 non-overlapped signals (PWML_I, PWMH_I).

Following start-up sequence must be strictly respected to avoid potential damage of the high-side power device:

1. First power up board (verify current consumption) with PWML/PWMH/HB_SA_SEL signals set to LOW
2. Then, set PWML to HIGH (100% DC)
3. Then, put HB_SA_SEL to HIGH; PWML_I/PWMH_I signals will be respectively at HIGH/LOW levels.
4. Finally, start gradually to decrease the PWML duty cycle to reach target value for the application.

Other recommendations

As power dissipation in the power FETs (due to switching losses) increases linearly with the PWM frequency, it is recommended to

1. start testing with low switching frequency,
2. to measure the system losses and
3. to check if the thermal resistance of the power devices is compatible with the losses generated by each power device

before increasing the switching frequency to the target value.

On the power board hosting power JFET, CISSOID recommends to put a resistor between NG and NS to turn-off the JFET in case of gate driver failure.

Typical application

A buck DC-DC converter shown by Figure 11 has been built and tested as a typical application case.

Figure 12 shows the load voltage and current waveforms and the half-bridge output voltage.

Figure 13 shows a detailed view on the falling edge of the half-bridge output voltage.

Figure 12 shows a detailed view on the rising edge of the half-bridge output voltage.

Test conditions:
- Temperature = 25°C
- PWM signals: 100kHz, 50% duty cycle.
- DC bus voltage = 600V
- Output voltage = 300V
- Output current = 10A
- Load resistance = 30Ω
- HB_SA_SEL = 5V
- Local non-overlap: 400 ns

Passive components:
- C=50uF
- L=0.47mH/80mΩ
- Load = 30 Ohm, 3kW

Power transistors:
- SemiSouth SJEP120R100

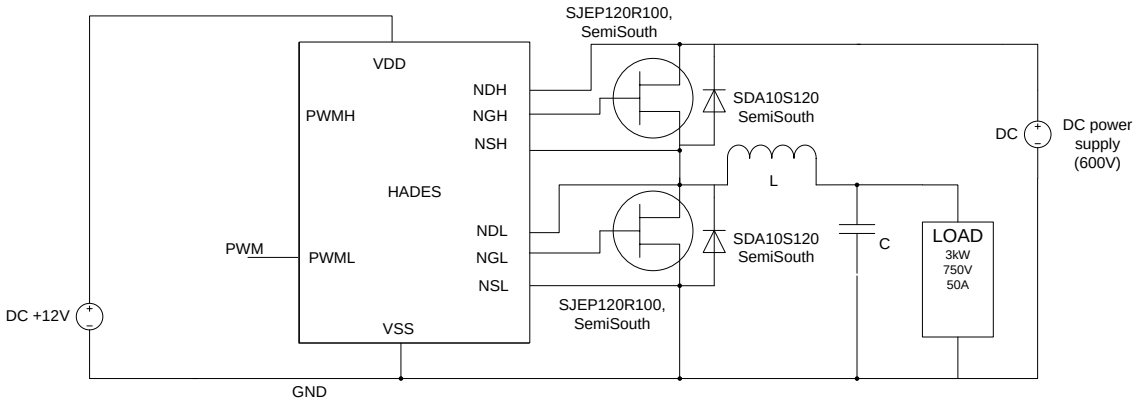


Figure 11: Buck DC/DC converter

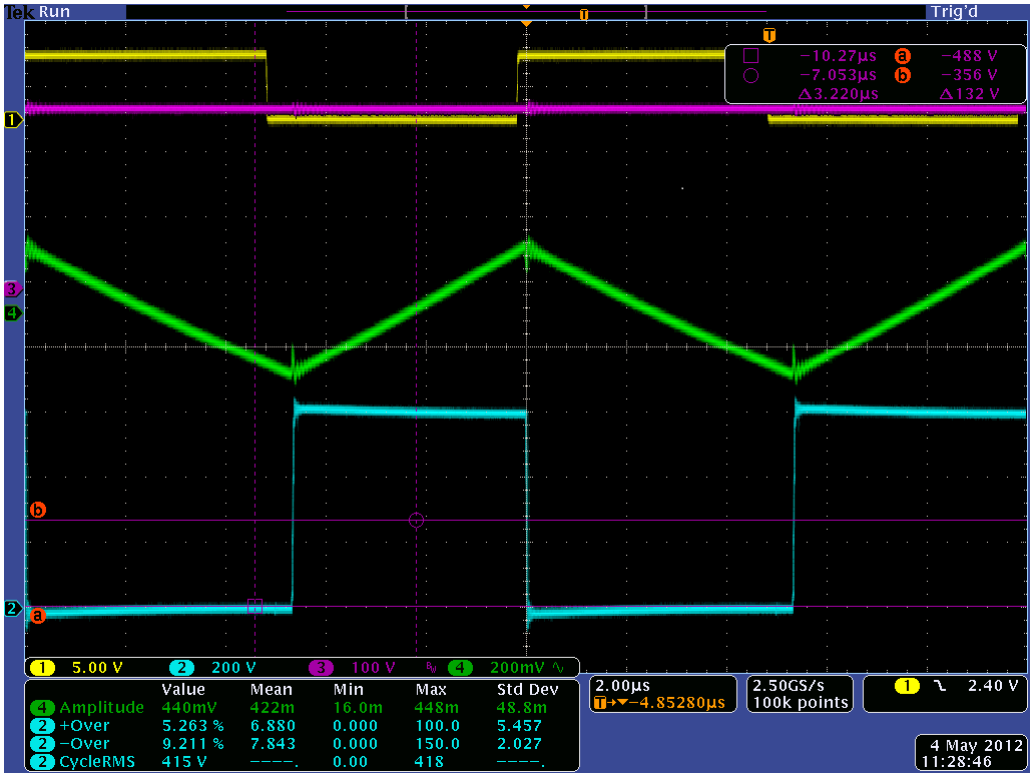


Figure 12: DC/DC operation at 100 kHz

(CH1: PWML, CH2: half-bridge output voltage, CH4: Iload [2A/div;AC])

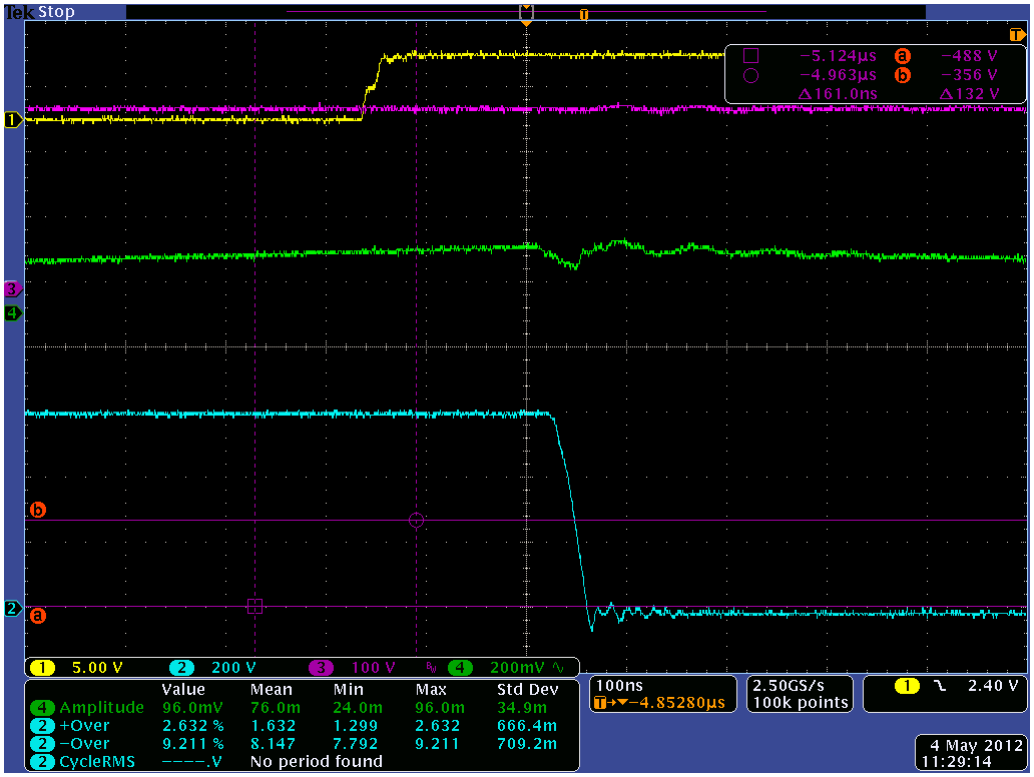


Figure 13: Detailed view on HB falling edge

(CH1: PWML, CH2: half-bridge output voltage, CH4: Iload [2A/div;AC])

(delay between PWML rising edge and HB falling edge is the sum of the HADES propagation delay and high-side JFET turn-off time)

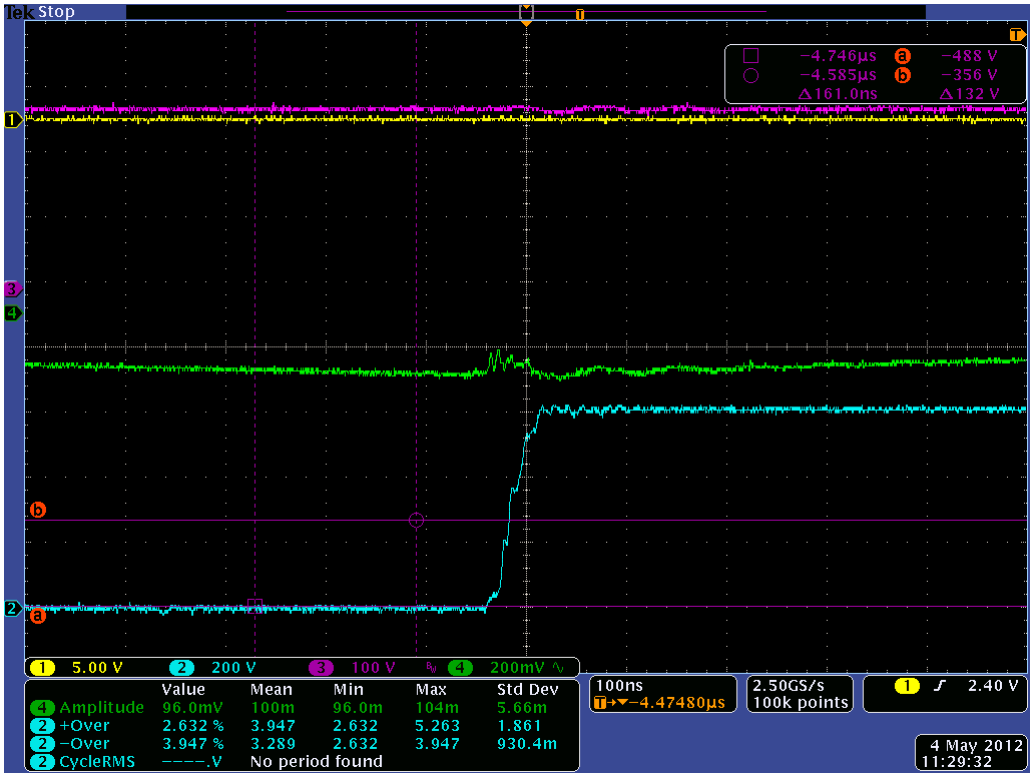


Figure 14: Detailed view on HB rising edge

(CH1: PWML, CH2: half-bridge output voltage, CH4: Iload [2A/div;AC])

(delay between PWML falling edge and HB rising edge is the sum of the local non-overlap [400ns], HADES propagation delay and high-side JFET turn-on time)

Board Mechanical Drawing

Physical dimensions: 108 mm (L) * 100 mm (H)

Figure 15:PCB Top side view

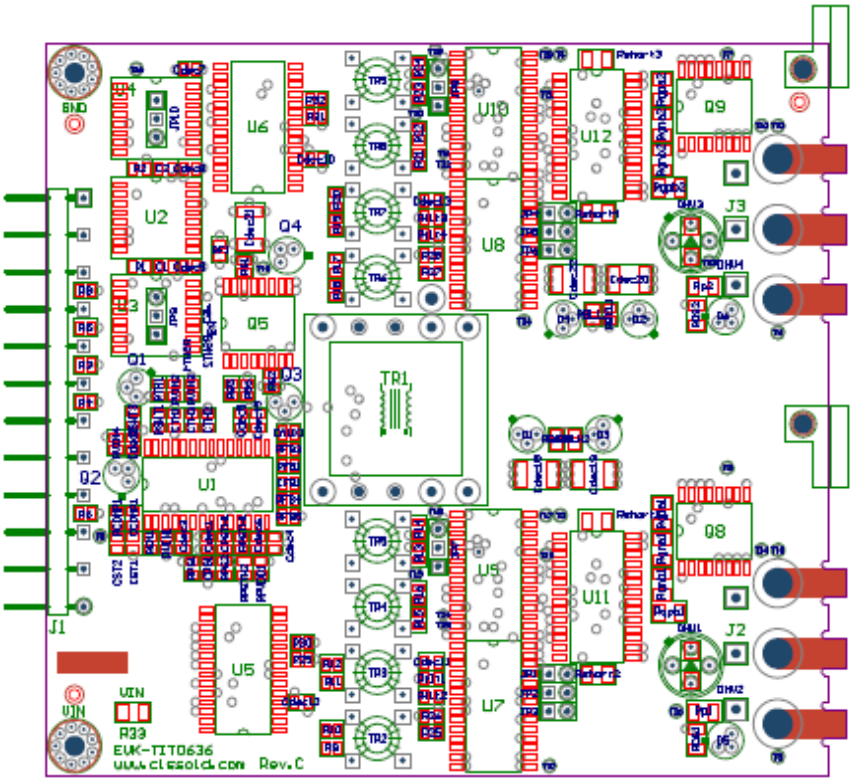
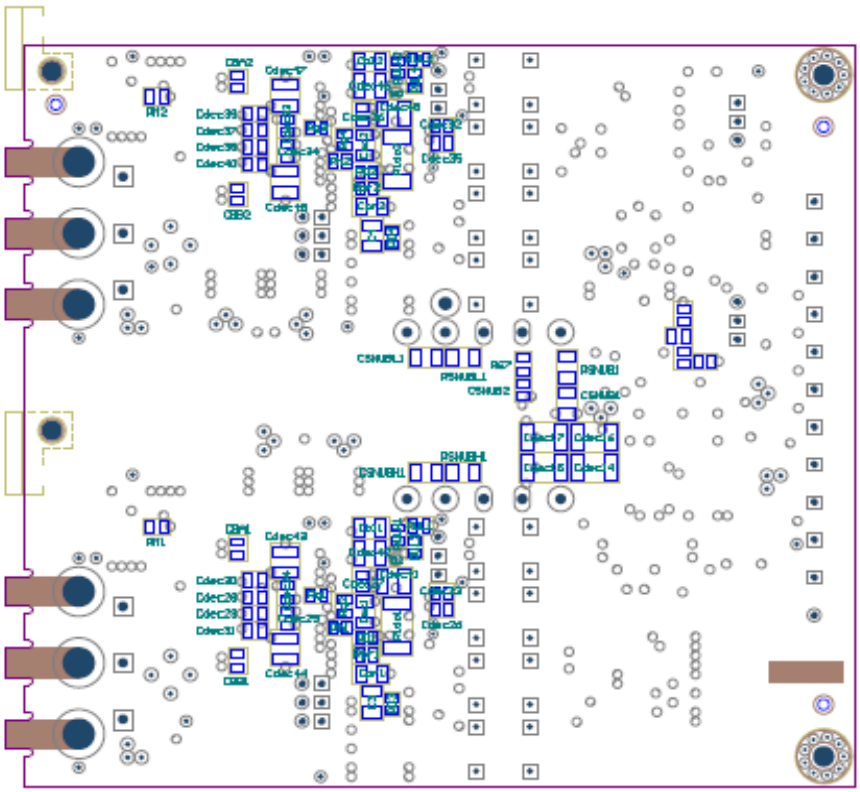


Figure 16: PCB Bottom side view



Board Electrical Schematic

Figure 17: Schematic: Top level

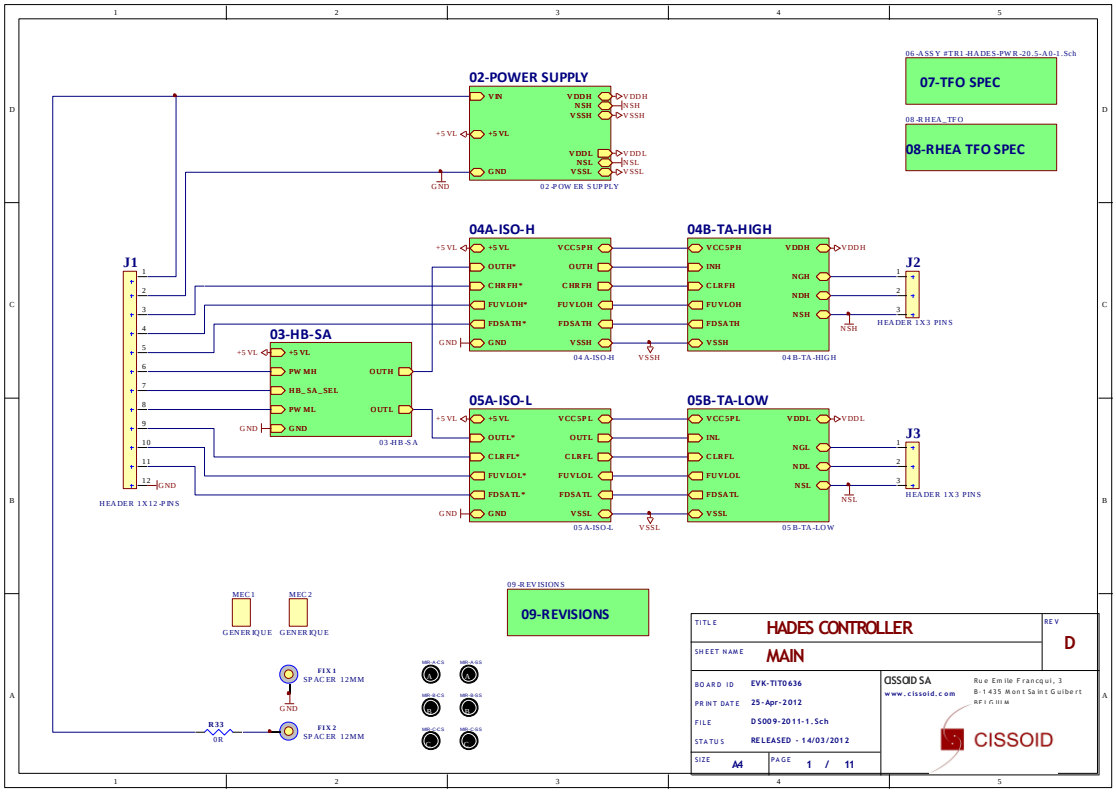


Figure 18: Schematic: PWM non-overlapping management

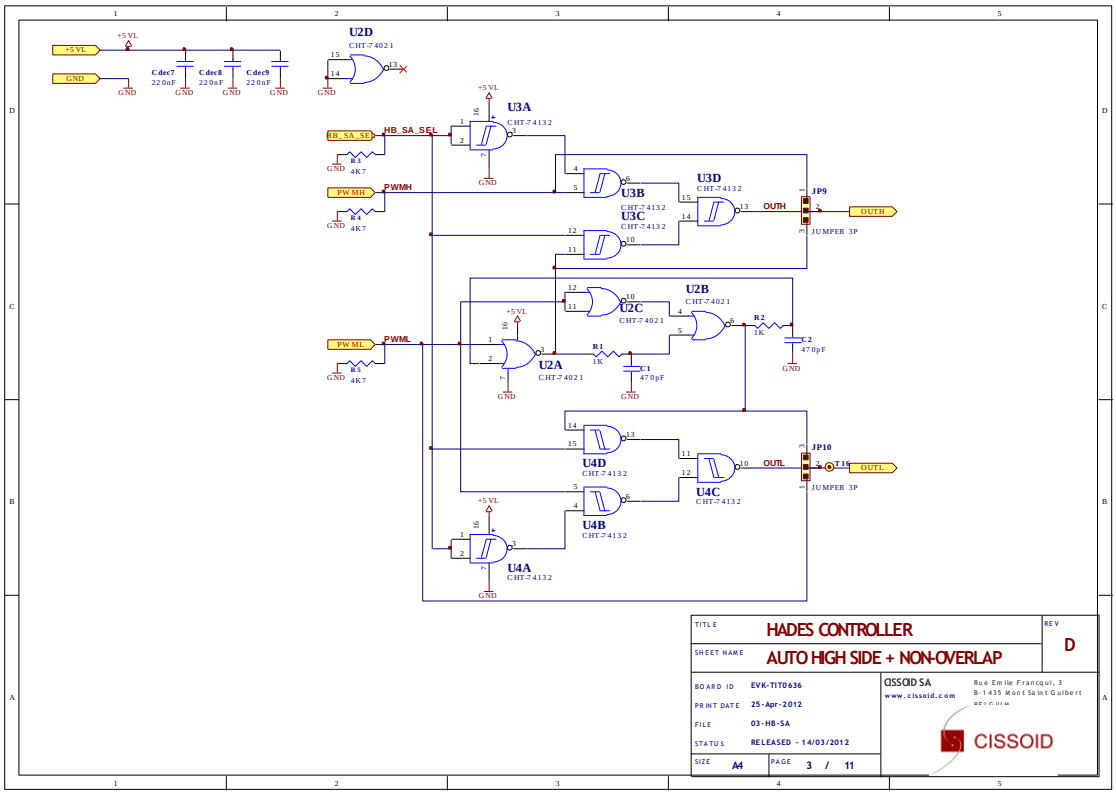


Figure 19: Schematic: Low side isolated data transmission

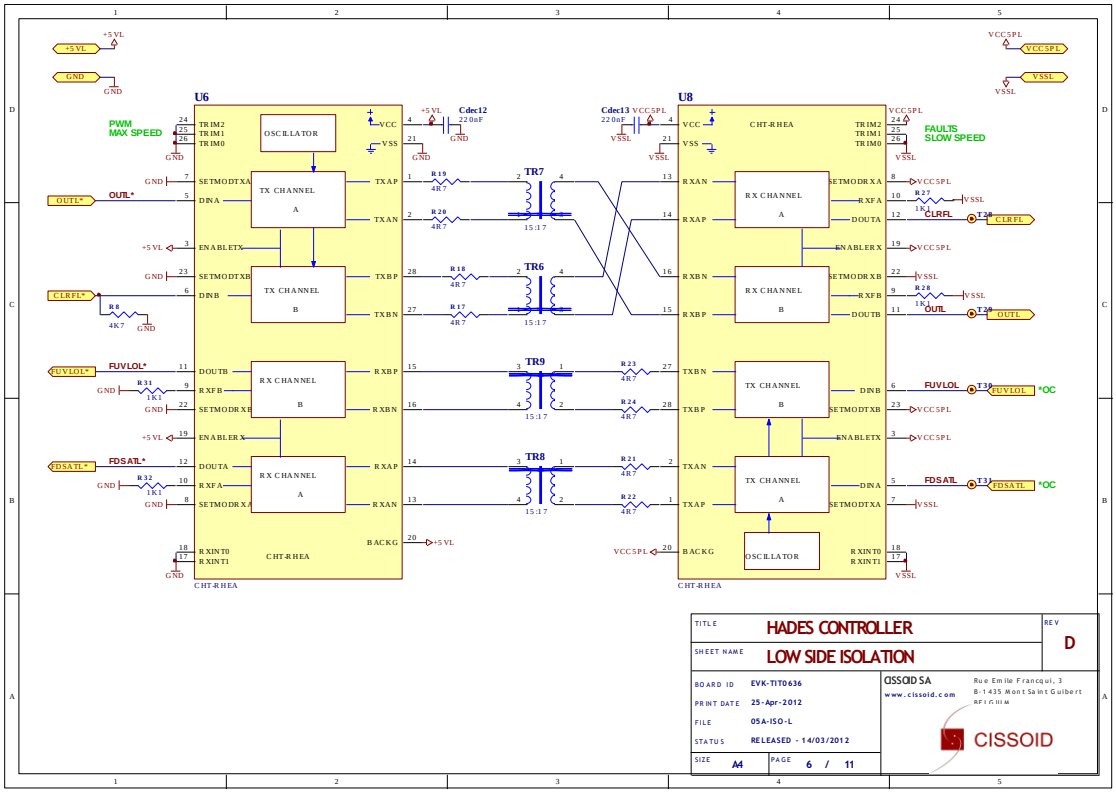


Figure 20: Schematic: Low side date drive

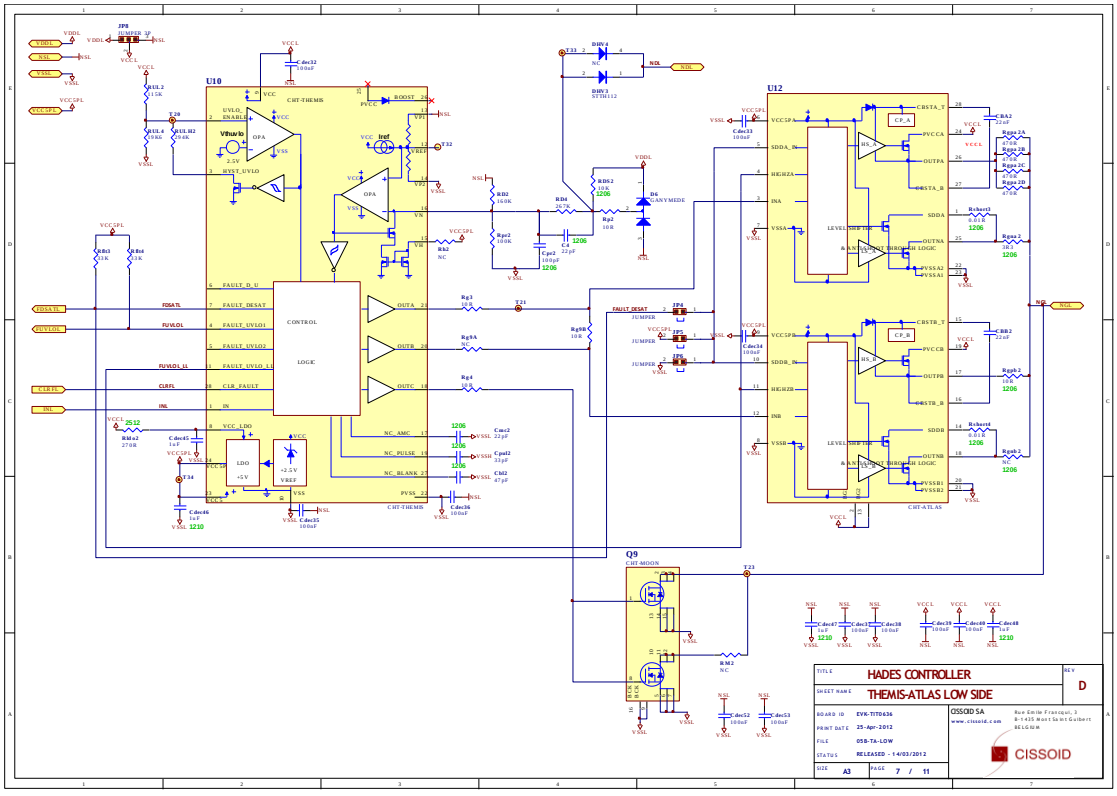


Figure 21: Schematic: High side isolated data transmission

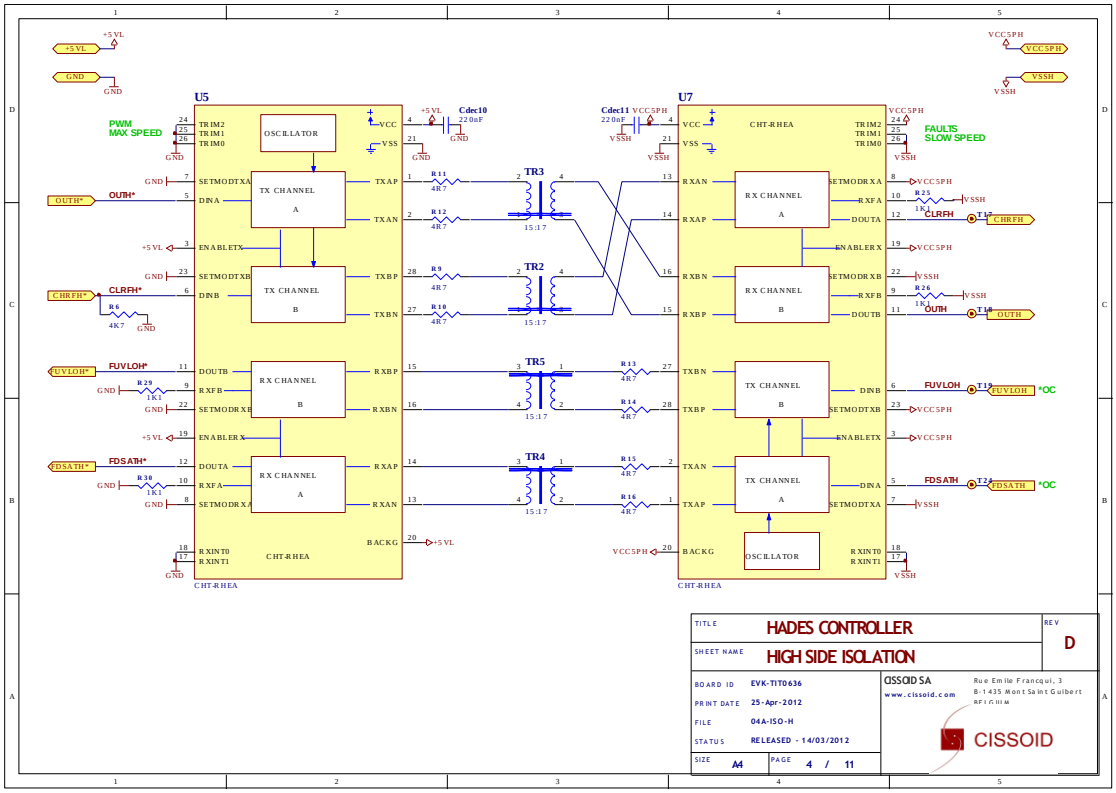
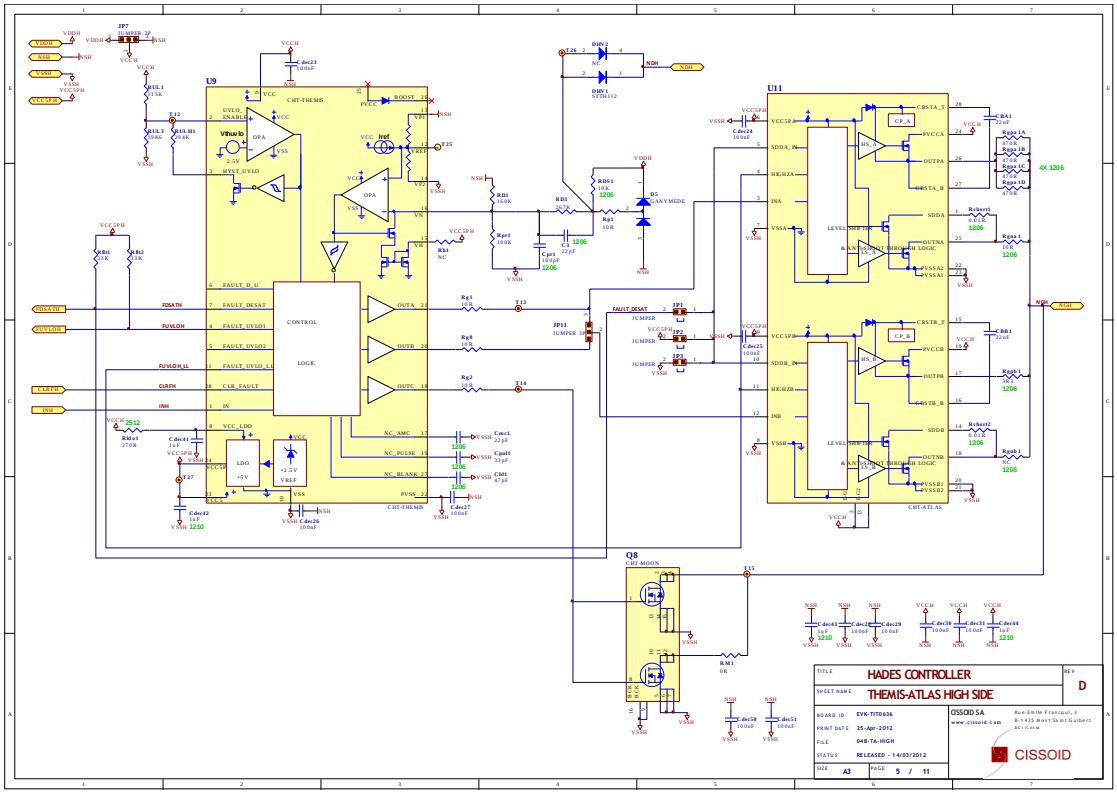


Figure 22: Schematic: High side gate drive



Board Configuration

Jumpers

Jumper identification	"Normally-Off" JFET
JP1	With the part CHT-TIT3345B, JP1 and JP2 should be left open and JP3 should be shorted. With the part CHT-TIT3345D, JP3 should be left open, while JP2 should be shorted if Soft-Shutdown function is not used; if Soft-Shutdown function is used, JP1 should be shorted.
JP2	
JP3	
JP4	With the part CHT-TIT3345B, JP4 and JP5 should be left open and JP6 should be shorted. With the part CHT-TIT3345D, JP6 should be left open, while JP5 should be shorted of Soft-Shutdown function is not used; if Soft-Shutdown function is used, JP4 should be shorted.
JP5	
JP6	
JP7	If jumper pos1 and pos2 are shorted, connects high-side gate drive positive supply (VCCH) to VDDH (15V)
JP8	If jumper pos1 and pos2 are shorted, connects low-side gate drive positive supply (VCCL) to VDDL (15V).
JP9	Allows to bypass the components U2/U3/U4 (generating the local non-overlap); jumper is located under U3 component. JP9 and JP10 must be set to the same position.
JP10	Allows to bypass the components U2/U3/U4 (generating the local non-overlap); jumper is located under U4 component. JP9 and JP10 must be set to the same position.

Component variants

Power dissipation by Themis: Rldo1 and Rldo2

In each channel, the supply current for CHT-RHEA is provided by the voltage regulator built inside CHT-THEMIS. CHT-THEMIS supply voltage is ranging from 30V (driving Semisouth JFETs) to 25V (driving CREE MOSFETs for instance). In order to reduce the power dissipated inside CHT-THEMIS regulator, a resistor is inserted in each channel (Rldo1, Rldo2) into the supply line to CHT-THEMIS regulator. The resistor can be adapted to the chosen supply voltage (i.e. the gate drive voltage). Various resistors have been considered depending on the application. The different cases are listed in the following table for a current consumption out of the CHT-THEMIS LDO of 45 mA.

SiC device	Supply voltages	Rldo1/2	Power dissipation in THEMIS	Power dissipation in Rldo1/2
SemiSouth Normally-Off JFET	VCC=+15V, VSS=-15V	270Ω	0.83W	0.54W

Desaturation Sense Diode

Two types of diodes have been considered in the board design; both footprints have been drawn at the same PCB locations.

DHV2, DHV4 are Cissoid CHT-IO high-voltage diodes qualified for 225°C operating temperature (no yet released).

DHV1, DHV3 are high-voltage diodes STTH112 (STMicroelectronis) which operate up to 175°C. Those diodes will be mounted on Hades until CHT-IO is released.

UVLO threshold

Both channels feature an under-voltage lock-out. The supply voltage between VCCH/L and VSSH/L is monitored and the channel is enabled only above some supply voltage threshold.

The threshold is defined by voltage dividers formed by resistors RUL1-RUL3 in the high-side channel and RUL2-RUL4 in the low-side channel. The function has some hysteresis so that two thresholds (UVLO_HIGH and UVLO_LOW) are actually defined with respect to VSS.

Two typical cases have been pre-defined changing RUL1 and RUL2 only although the threshold can easily be adjusted at will.

Supply voltages	**UVLO_High Threshold wrt to VSS**	**UVLO_Low Threshold wrt to VSS**	**RUL1/2**
VCC=+15V, VSS=-15V	18V	17V	115 kΩ

Bill of Material

Quantity	Value	Designators	Description	Manufacturer	Part Number
RESISTORS					
0	0.01R	Rshort1, Rshort2, Rshort3, Rshort4	RESISTOR, 1206 1% 0.01R	YAGEO (PHYCOMP)	RL1206FR-7W0R01L
2	1R5	RS1, RS2	RESISTOR, 0805, 1R5, 1% 250mW 200PPM	PANASONIC	ERJ6BQF1R5V
1	0R	RFB5	RESISTOR, 0805 0R0,0.1W	MULTICOMP	MC 0.1W 0805 0R
1	0R	R33	RESISTOR, 0OHM, 0.125W, 5%	MULTICOMP	MC 0.125W 1206 0R
1	2R2	RF1	RESISTOR, 2,2OHM, 0.125W, 1%	YAGEO (PHYCOMP)	2390401722O8
1	3R3	Rgna1, Rgna2	RESISTOR, 3.3OHM, 1W, 5%	BOURNS	CRM2010-JW-3R3ELF
0	NC	RCOMP1, RVIN3, RM1, RM2, Rh1, Rh2	-	-	-
5	100K	RFB1, RPG1, RPGTH1, Rpr1, Rpr2	RESISTOR, 100K, 0805 1% 0.25W	MULTICOMP	MCHP05W4F1003T5E
2	10K	RFB3, RFB4	RESISTOR, 0805, 10K	TE CONNECTIVITY / NEOHM	CPF0805B10KE1
2	10K	RDS1, RDS2	RESISTOR, 10KR , 1%, 0.25W	VISHAY DRALORIC	CRCW120610K0FKEA
7	10R	RPVDD1, Rg1, Rg2, Rg3, Rg4, Rg8, Rg9	RESISTOR, 0805, 10R 0.1% 15PPM	TE CONNECTIVITY / HOLSWORTHY BOURNS	RP73D2A10RBTG CRT1206-BY-10R0ELF
7	10R	RRgnb1, Rgnb2, Rgbp1, Rgbp2, Rp1, Rp2, RSNUB1	RESISTOR, 1206, 10R 0.1% 15PPM	TE CONNECTIVITY / HOLSWORTHY	RP73D2B10RBTG
2	115K	RUL1, RUL2	RESISTOR, 115K, 0805 0.1% 25PPM 0.1W	PANASONIC MULTICOMP	ERA6AEB1153V MCTC0525B1153T5E
2	160K	RD1, RD2	RESISTOR, 160K, 0805 0.1% 25PPM 0.1W	PANASONIC	ERA6AEB164V
2	19K6	RUL3, RUL4	RESISTOR, 0805, 19K6 0.1% 15PPM	TE CONNECTIVITY / HOLSWORTHY	RP73D2A19K6BTG
4	1K	RSWT2, RSWT3, R1, R2	RESISTOR, 1K 25PPM 0.1% 0805	WELWYN	PCF0805P-R-1K-BT1
5	3K3	RSWT1, RBLH1, RBLH2, RBLL1, RBLL2	RESISTOR, 3K3 25PPM 0.05% 0805 RESISTOR, 3K3 10PPM 0.1% 0805	WELWYN PANASONIC	PCF0805P-R-3K3-BT1 ERA6ARW332P
1	1K8	RSWT4	RESISTOR, 1K8 25PPM 0.1% 0805 RESISTOR, 1K8 10PPM 0.05% 0805	WELWYN PANASONIC	PCF0805P-R-1K8-BT1 ERA6ARW182P
8	1K1	R25, R26, R27, R28,R29, R30, R31, R32	RESISTOR, 0805, 1K1, 0.1%, 25PPM, 0.125W	PANASONIC	ERA6AEB112V
1	1M	RVIN2	RESISTOR, 0805, 1M, 0.1%, 0.125W	PANASONIC	ERA6AEB105V
2	220R	RVIN4, RSF	RESISTOR, 0805, 220R, 0.1%, 0.125W	PANASONIC	ERA6AEB221V
2	22R	RG5, RG6	RESISTANCE 0805 22R1 10PPM	TE CONNECTIVITY / NEOHM	CPF0805B22RE1
2	267K	RD3, RD4	RESISTOR, 0805, 267K, 25PPM 0.1%, 0.125W	PANASONIC WELWYN	ERA6AEB2673V PCF0805R 267KBI
2	270R	Rldo1,Rldo2	RESISTOR, 2512, 270R 1%, 1.5W	MULTICOMP	MCPWR12FTEA2700
2	294K	RULH1, RULH2	RESISTOR, 0805, 294K, 0.1%, 25PPM 0.125W RESISTOR, 0805, 294K, 0.1%, 15PPM 0.125W	PANASONIC TE CONNECTIVITY	ERA6AEB2943V RP73D2A294KBTG
1	2M2	RPG2	RESISTOR, 0805, 2.2M 1%, 0.125W	MULTICOMP	MCPWR05FTEW2204
4	33K	Rflt1, Rflt2, Rflt3, Rflt4	RESISTOR, 0805, 33K	TE CONNECTIVITY / NEOHM	CPF0805B33KE1
1	300K	RPGTH2	RESISTOR, 0805, 300K, 0.1%, 25PPM, 0.125W	PANASONIC	ERA6AEB304V
1	470R	RG7	RESISTOR, 0805, 1%, 470R	VISHAY DRALORIC	CRCW0805470RFKEAHP
10	470R	RSNUBH1, RSNUBL1, Rgpa1A,Rgpa1B,Rgpa1C,Rgpa1D, Rgpa2A, Rgpa2B, Rgpa2C, Rgpa2D	RESISTOR, 1206, 1%, 470R	VISHAY DRALORIC	CRCW1206470RFKEAHP
1	47K	REN1	RESISTOR, 0805, 47K, 0,5%	YAGEO (PHYCOMP)	RE0805DR-0747KL
1	47R	RTH1	RESISTOR, 0805, 47R	TE CONNECTIVITY / NEOHM	CPF0805B47RE1
5	4K7	R3, R4, R5, R6, R8	RESISTOR, 0805, 4K7	TE CONNECTIVITY / NEOHM	CPF0805B4K7E1
17	4R7	RVIN1, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24	RESISTOR, 0805, 1%, 4R7, 0.250W	PANASONIC	ERJ6BQF4R7V
CAPACITORS					
23	100nF	CAUX1, Cdec23, Cdec24, Cdec25, Cdec26, Cdec27, Cdec28, Cdec29, Cdec30, Cdec31, Cdec32, Cdec33, Cdec34, Cdec35, Cdec36, Cdec37, Cdec38, Cdec39, Cdec40, Cdec50, Cdec51, Cdec52, Cdec53	CAPACITOR, AECQ200, 0805, 50V, 100NF	AVX	08055F104K4T2A
1	100pF	CTH3	CAPACITOR, 0805, 100PF, 600V, C0G 10% CAPACITOR, 0805, 100PF, 100V, C0G 5%	AVX AVX	0805CA101KAT1A 08051A101JAT2A
2	100pF	Cpr1,Cpr2	CAPACITOR, 1206 SIZE, 200V, 100PF	KEMET	C1206C101J2GACTU
2	10nF	CCOMP1, CPGTH1	CAPACITOR, 0805, 10NF, 50V, X8R	AVX	08055F103KAT2A
2	1nF	CPG1, CSF	CAPACITOR, AECQ200, 1000PF, 100V	AVX	08051A102J4T2A
8	1uF	Cdec41, Cdec42, Cdec43, Cdec44, Cdec45, Cdec46, Cdec47, Cdec48	CAPACITOR, 1UF, 50V, 1210	KEMET	C1210C105K5NACTU
12	220nF	Cdec3, Cdec4, Cdec5, Cdec6, Cdec7, Cdec8, Cdec9, Cdec10, Cdec11, Cdec12, Cdec13, Cdec49	CAPACITOR, 220NF, 50V, 0805	KEMET	C0805C224K5NACTU
1	470pF	C1, C2	CAPACITOR, 0805 SIZE, 200V, 470PF	KEMET	C0805C471J2GACTU
1	220pF	CSNUB2	CAPACITOR, 0805 SIZE, 200V, 220PF	KEMET	C0805C221J2GACTU
2	220pF	CSNUBH1, CSNUBL1	CAPACITOR, 1206, 220PF, 500V	AVX	12067A221JAT2A
5	22nF	CFB1, CBA1, CBA2, CBB1, CBB2	CAPACITOR, 0805, C0G, 50V, 22NF	TDK	C2012C0G1H223J
4	22pF	C3, C4, Cmc1, Cmc2	CAPACITOR, 1206, 22PF, 100V	AVX	12061A220JAT2A
9	22uF	Cdec18, Cdec19, Cdec20, Cdec21, Cdec22, Cdec14,Cdec16	MLCC, 1812, X5R, 25V, 22UF	TDK	C4532X5R1E226M
0	22uF	Cdec15, Cdec17	MLCC, 1812, X5R, 25V, 22UF	TDK	C4532X5R1E226M
4	330nF	CST1, CST2, Cdec1, Cdec2	CAPACITOR, 330NF, 25V, 0805	KEMET	C0805C334K3NACTU
1	4.7nF	CSNUB1	CAPACITOR, 1206, 4.7NF, 50V, NP0	KEMET	C1206C472J5GACTU
1	47pF	CTH1	CAPACITOR, 0805 SIZE, 100V, 47PF	KEMET	C0805C470J1GACTU
1	150pF	CTH2	CAPACITOR, 0805 SIZE, 100V, 150PF	KEMET	C0805C151J5GACTU
2	47pF	Cbl1, Cbl2	MLCC, 1206, 47PF, 200V, NP0, 5%	YAGEO (PHYCOMP)	CC1206JRNPOABN470
MAGNETICS					
8	-	TR2, TR3, TR4, TR5, TR6, TR7, TR8, TR9	RHEA pulse transformer	contact CISSOID	TR1-1012-4C65-A0
1	-	TR1	POWER SUPPLY TRANSFORMER	contact CISSOID	TR1-HADES-PWR-20/5-A0
ACTIVES					
1	CHT-74021	U2	CHT-74021, Quad 2-Inputs NOR Gate	CISSOID	CHT-74021-CSOIC16-T
2	CHT-74132	U3, U4	CHT-74132, Quad 2-Input NAND Schmitt Trigger	CISSOID	CHT-74132-CSOIC16-T
2	CHT-ATLAS	U11, U12	CHT-ATLAS, Dual Channel Power Transistor Driver	CISSOID	CHT-TIT3345B-CSOIC28-T
1	CHT-MAGMA	U1	CHT-MAGMA, PWM controller	CISSOID	CHT-MAGMA-CSOIC28-T
3	CHT-MOON	Q5, Q8, Q9	CHT-MOON, Dual NMOS transistor 40V	CISSOID	CHT-PLA2016A-CSOIC16-T
4	CHT-RHEA	U5, U6, U7, U8	CHT-RHEA, Isolated transceiver - dual channel	CISSOID	CHT-TIT4750D-CSOIC28-T
2	CHT-THEMIS	U9, U10	CHT-THEMIS, Dual Channel Power Transistor Driver	CISSOID	CHT-TIT9570A-CSOIC28-T
2	CHT-GANYMEDE	D5,D6	CHT-GANYMEDE, Dual Series Small Signal Diode 80V	CISSOID	CHT-PLA5598C-TO18-T
4	CHT-CALLISTO	D1, D2, D3, D4	CHT-CALLISTO, Dual Common Anode Small Signal Diode 80V	CISSOID	CHT-PLA5520A-TO18-T
3	CHT-SNMOS80	Q1, Q2, Q3	CHT-SNMOS80, Small Signal Transistor - NMOS - 80V	CISSOID	CHT-SNMOS80-TO18-T
0	CHT-SNMOS80	Q4	CHT-SNMOS80, Small Signal Transistor - NMOS - 80V	CISSOID	CHT-SNMOS80-TO18-T
0	CHT-IO	DHV2, DHV4	High Voltage Small Signal Diode	CISSOID	CHT-IO
2	STTH112	DHV1, DHV3	High Voltage Small Signal Diode	STM	STTH112
MECHANICAL					
0	NC	JP9, JP10			
1	HEADER 1X12-PINS	J1	Custom de-populated by Cissoid – Gold vertical Step 5.08mm L=12mm Bottom mounted	FCI	77311-818-36LF
2	HEADER 1X3 PINS	J2, J3	Custom de-populated by Cissoid – Gold vertical Step 7.62mm L=12mm Bottom mounted	FCI	77311-818-36LF
0	JUMPER 2P	JP1, JP2, JP4, JP5			
2	JUMPER 2P	JP3, JP6	0,8mm Wire jumper between pins 1-2		
4	JUMPER 3P	JP7, JP8, JP11, JP12	0,8mm Wire jumper between pins 1-2 (PIN1 is round, PIN2 is center)	ANY	

Ordering Information

Product Name	Ordering Reference	Package	Marking
EVK-HADES (SS NOff JFET)	EVK-TIT0636B	NA	EVK-TIT0636

Contact & Ordering

CISSOID S.A.

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Caution

CAUTION: All handling with high voltages involves risk to life.

It is imperative to comply with the respective safety regulations!