CENTON ELECTRONICS, INC.

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MEMORY
SPECIFICATIONS

16MEGX64 (PC133)

16,777,216 words x 64Bit Synchronous Dynamic RAM Memory Module

(Unbuffered DIMM)

Centon's 128MB Memory Module is 16,777,216 words by 64Bit Synchronous Dynamic RAM Memory Module. The Memory Module is assembled with 4 pieces of a 16MX16Bit PC133 compliant TSOP Synchronous Dynamic RAM on the printed circuit board. The module is optimized for high density and large capacity in a compact size.

16MEGX64 (PC133) - *128MB*

Pinout Information

1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	NC	142	DQ51
3	DQ1	31	NC	59	Vcc	87	DQ33	115	RAS	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	NC	90	Vcc	118	A3	146	NC
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	NC	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vcc	101	DQ45	129	NC	157	Vcc
18	Vcc	46	DQM2	74	DQ28	102	Vcc	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	NC	160	DQ62
21	NC	49	Vcc	77	DQ31	105	NC	133	Vcc	161	DQ63
22	NC	50	NC	78	Vss	106	NC	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	NC
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	NC	109	NC	137	NC	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	WE	55	DQ16	83	SCL	111	CAS	139	DQ48	167	SA2
28	DQM0	56	DQ17	84	Vcc	112	DQM4	140	DQ49	168	Vcc

Pin Name	Function
A_0-A_{12}	Address input (Row=A_0-A_{12},Column=A_0-A_8)
BA_0-BA_1	Select bank
DQ_0-DQ_{63}	Data input/output
CLK_0, CLK_2	Clock input
CKE_0	Clock enable input
/CS_0, /CS_3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM_0-DQM_7	Data input/output mask
V_{DD}	Power supply (3.3V)
V_{SS}	Ground
SDA	Serial data I/O
SCL	Serial clock
SA_0-SA_2	EEPROM Address
NC	No connection

CPCB-00436C

16MEGX64 (PC133) - *128MB*

FEATURES

* 16,777,216 words by 64 bits organization
* Utilizes PC133 compliant SDRAM components
* NON-Buffered, 2 clock implementation
* Single power supply of 3.3V +/- 10%
* Fully Synchronous with all signals registered positive edge of clock
* Internal pipeline operation
* Support progammable Mode Register
* CAS Latency: 2,3
* Burst length; 1, 2, 4, 8 or Full Page
* 8192 refresh cycles / 64ms
* Supports Auto refresh and Self refresh
* All inputs and outputs LVTTL compatible
* 168 pin JEDEC pin compatible
* RoHS compliant.

COMPATIBILITY

Centon's 128MB Memory Module is fully compatible with industry standard PC133 168 pin Memory Modules.

APPLICATION

Main/Expansion Memory Unit for personal computers and Power PCs.

ENVIRONMENT

	OPERATING	STORAGE
TEMPERATURE	0°C to 70°C	-55°C to 125°C
HUMIDITY	20% to 80%	5% to 8%

WARRANTY

Centon will repair or replace any Centon memory product that fails due to defective material or workmanship under normal use for the life of the product.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage	V_{CC}	-0.3 to 4.6	V
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.3 to 4.6	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	Pd	4	W
Operating temperature	T_{OPR}	0 to +70	C
Storage temperature	T_{STG}	-55 to +125	C

Notes:

1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
2. Functional operation should be restricted to recommended operation conditions.
3. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Notes	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	1	V
Input Voltage High	V_{IH}	2.0	3.0	V_{CC}+0.3	1,2	V
Input Low Voltage	V_{IL}	-0.3	0	0.8	1,3	V

Notes:

1. All voltages are referenced to V_{SS}=0V.
2. V_{IH}(max) = V_{CC}+1.2V for pulse width with $\leq$ 3ns of duration
3. V_{IL}(min) = V_{SS} -1.2V for pulse width with $\leq$ 3ns of duration.

DC Characteristics I

(Ta=0 to 70C, Vcc=3.3+/-0.3V)

Parameter (Test Condition)	Symbol	Min	Max	Note	Unit
Input leakage current (V_{IN}=0 to 3.6V, all other pins not under test=0V)	I_{LI}	-20	20		uA
Output leakage current (D_{OUT} is disabled, V_{OUT}=0 to 3.6V)	I_{LO}	-5	5		uA
Output low voltage (I_{OL}=2.0mA)	V_{OL}		0.4		V
Output high voltage (I_{OH}=-2.0mA)	V_{OH}	2.4			V

DC Characteristics II

(Ta=0 to 70C, Vcc=3.3+/-0.3V)

Parameter	Test Condition	Symbol	Min	Max	Note	Unit
Operating Current	Burst Length = 1, $t_{RC} \geq t_{RC}$(min), I_{OL} = 0mA	Icc1		640	1	mA
Precharge standby current in power-down	CKE$\leq V_{IL}$(max), t_{CK}=min	Icc2P		8		mA
	CKE$\leq V_{IL}$(max), t_{CK}=∞	Icc2PS		4		mA
Precharge standby current in non power-down mode	CKE$\geq V_{IH}$(min)=/CS$\geq V_{IH}$(min), t_{CK}=min, Input signals are changed one time during 20ns	Icc2N		120		mA
	CKE$\geq V_{IH}$(min), CLK$\leq V_{IL}$(max), t_{CLK}=∞, Input signals are stable	Icc2NS		20		mA
Active standby current in power-down mode	CKE$\leq V_{IL}$(max), tCLK=min	Icc3P		20		mA
	CKE & CLK$\leq V_{IL}$(max), t_{CLK}=∞	Icc3PS		20		mA
Active standby current in non power-down mode	CKE$\geq V_{IH}$(min), /CS$\geq V_{IH}$(min), t_{CLK}=min, Input signals are changed one time during 20ns	Icc3N		120		mA
	CKE$\geq V_{IH}$(min), CLK$\leq V_{IL}$(max), t_{CLK}=∞, Input signals are stable	Icc3NS		120		mA
Burst mode current	tCLK=min, I_{OL}=0mA, all banks activated	Icc4		600	1	mA
Auto-refresh current	$t_{RC} \geq t_{RC}$(min)	Icc5		800	2	mA
self-refresh current	CKE $\leq$ 0.2V	Icc6		8	3	mA
	CKE $\leq$ 0.2V, LP			4.8		

Notes:

1. Icc1 & Icc4 depend on output loading and cycle rates. Specified values are measured with output open.
2. Min. of t_{RCC} (Refresh /RAS cycle time) is shown at AC CHARACTERISTICS II.
3. LP indicates Low Power self-refresh current

Capacitance

(Vcc=3.3V, Ta = 25deg C, f = 1MHz)

Parameter	Symbol	Max	Unit
Address (A_0 - A_{12}, BA_0-BA_1)	C_{ADD}	25	pF
/RAS, /CAS, /WE	C_{IN}	25	pF
CKE (CKE_0)	C_{CKE}	25	pF
Clock (CLK_0, CLK_2)	C_{CLK}	15	pF
/CS (CS_0, CS_2)	C_{CS}	15	pF
DQM (DQM_0-DQM_7)	C_{DQM}	10	pF
DQ (DQ_0-DQ_{63})	C_{OUT}	10	pF

AC Characteristics I

(Ta=0 to 70C, VCC=3.3V+/-0.3V,Vss=0V)

Parameter		Symbol	Min	Max	Note	Unit
Clock Cycle time	/CAS Latency 3	t_{CK3}	7	1000		ns
	/CAS Latency 2	t_{CK2}	7.5			ns
Clock to valid output delay	/CAS Latency 3	t_{AC3}		5.4	2	ns
	/CAS Latency 2	t_{AC2}		5.4		ns
Output data hold time		t_{OH}	3		2	ns
Clock to Output in High-Z		t_{OHZ}		5.4		ns
Clock to Output in Low-Z		t_{OLZ}	1			ns
Clock high pulse width		t_{CH}	2.5		1	ns
Clock low pulse width		t_{CL}	2.5		1	ns
Address setup time		t_{AS}	1.5		1	ns
Address hold time		t_{AH}	0.8		1	ns
Data input setup time		t_{DS}	1.5		1	ns
Data input hold time		t_{DH}	0.8		1	ns

Note:

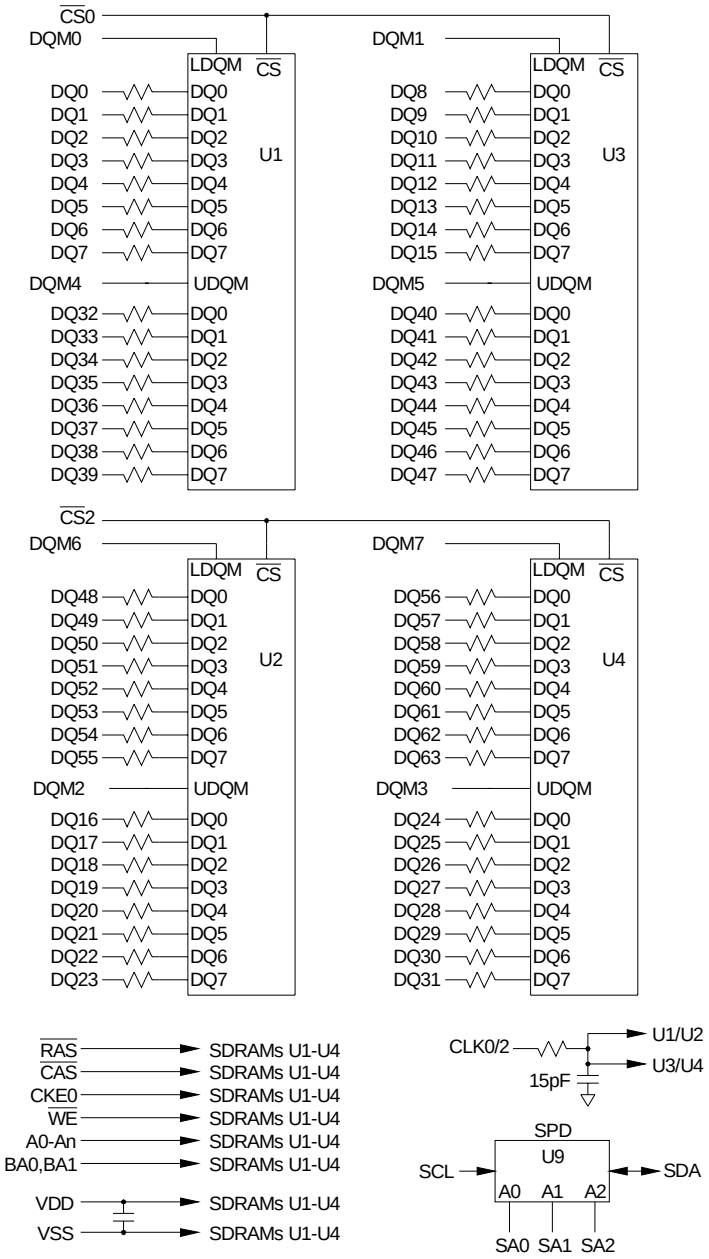
1. Assume t_R/t_F (input rise and fall time) is 1ns.
2. Access times to be measured with input signals of 1V/ns edge rate.

AC Characteristics II

(Ta=0 to 70C, VCC=3.3V+/-0.3V,Vss=0V)

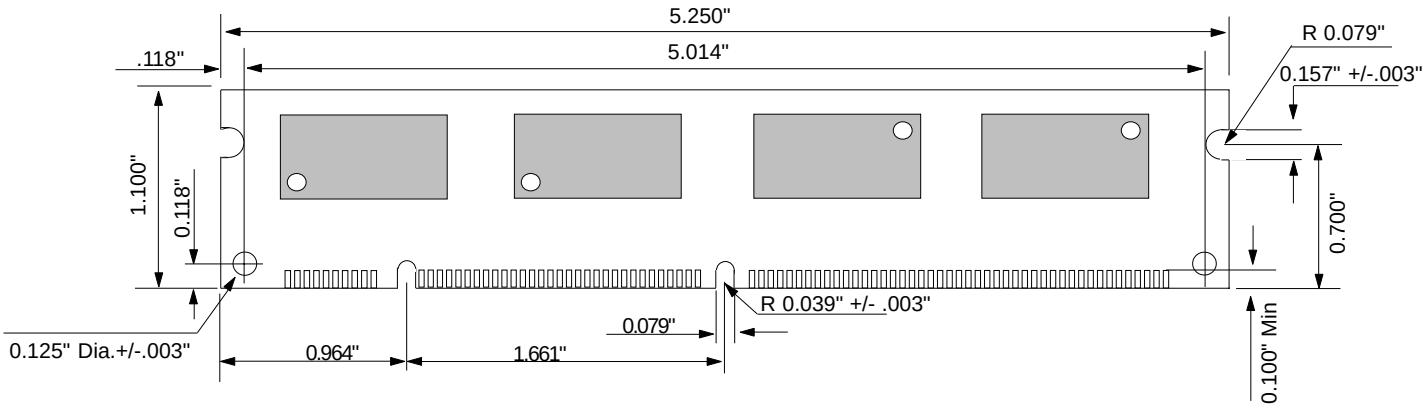
Parameter	Symbol	Min	Max	Note	Unit
/RAS cycle time	t_{RC}(min)	60			ns
/RAS to /CAS Delay	t_{RCD}	15			ns
/RAS to /RAS Bank Active Delay	t_{RRD}	14			ns
/RAS precharge time	t_{RP}	15			ns
/RAS active time	t_{RAS}	37	100K		ns
/CAS to /CAS Delay	t_{CCD}	1			CLK
Data-In to Precharge Command (Write Recovery)	t_{RDL}	2			CLK
Mode Register set to Active Delay	t_{RSC}	2			CLK
Refresh interval time	t_{REF}		64		ms

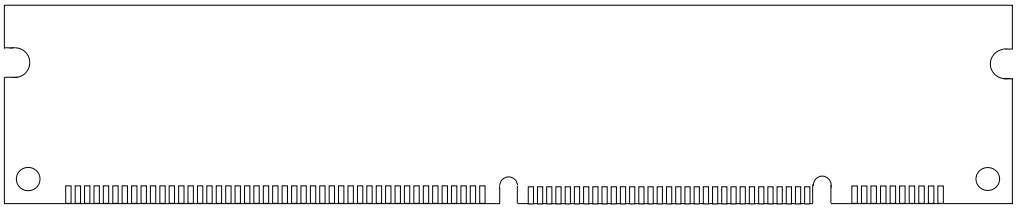
Block Diagram

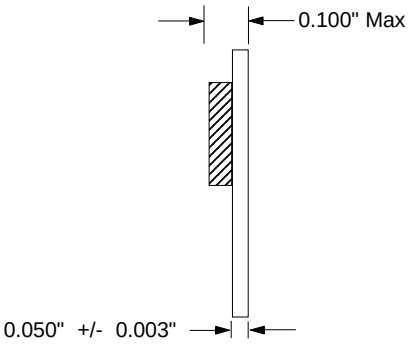


Note: All resistor values are 10 Ohms

Mechanical Drawing







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