N-Channel JFET
Monolithic Dual

calogic
CORPORATION

SST404 / SST405 / SST406

FEATURES

- **Very Low Noise . . . . . $\bar{e}_n$ < 10 nV/$\sqrt{Hz}$ @ 10Hz**
- **Low Input Bias . . . . . I_G < 2pA**
- **High Breakdown Voltage . . . . . B_V > 50V**

APPLICATIONS

- **Precision Instrumentation**
- **Input Amplifiers**
- **Impedance Converters**

DESCRIPTION

The SST404 Series is a very Low Noise Monolithic N-Channel JFET Pair in a surface mount SO-8 plastic package. Designed utilizing Calogic's proprietary JFET processing techniques these devices are ideal for front end amplification of low level signals. The low noise, low leakage and good frequency response are excellent features for sensitive medical, instrumentation and infrared designs.

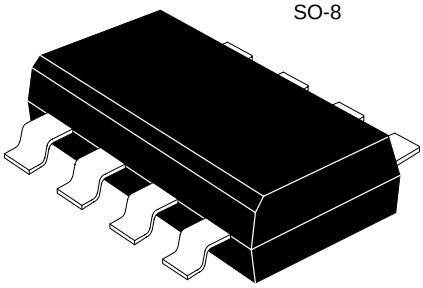
ORDERING INFORMATION

Part	Package	Temperature Range
SST404-6	Plastic SO-8	-55°C to +125°C

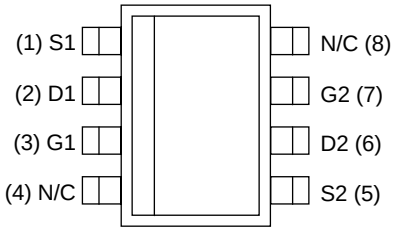
NOTE: For Sorted Chips in Carriers, See U401 Series

PIN CONFIGURATIONS

SO-8



TOP VIEW



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PRODUCT MARKING	
SST404	R04
SST405	R05
SST406	R06

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter/Test Condition	Symbol	Limit	Unit
Gate-Drain Voltage	V_{GD}	-50	V
Gate-Source Voltage	V_{GS}	-50	V
Forward Gate Current	I_G	10	mA
Power Dissipation (per side)	P_D	300	mW
(total)		500	mW
Power Derating (per side)		2.4	mW/ °C
(total)		4	mW/ °C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 200	°C
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

SYMBOL	CHARACTERISTCS	TYP[1]	SST404		SST405		SST406		UNIT	TEST CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
STATIC										
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	-58	-50		-50		-50		V	I_G = -1µA, V_{DS} = 0V
$V_{(BR)G1 - G2}$	Gate-Gate Breakdown Voltage	-58	±50		±50		±50		V	I_G = ±1µA, V_{DS} = 0V, V_{GS} = 0V
$V_{GS(OFF)}$	Gate-Source Cut off Voltage	-1.5	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5	V	V_{DS} = 15V, I_D = 1nA
I_{DSS}	Saturation Drain Current [2]	3.5	0.5	10	0.5	10	0.5	10	mA	V_{DS} = 15V, V_{GS} = 0V
I_{GSS}	Gate Reverse Current	-2		-25		-25		-25	pA	V_{GS} = -30V, V_{DS} = 0V
		-1							nA	T_A = 125°C
I_G	Gate Operating Current	-2		-15		-15		-15	pA	V_{DG} = 15V, I_D = 200µA
		-0.8		-10		-10		-10	nA	T_A = 125°C
$r_{DS(ON)}$	Drain-Source On-Resistance	250							Ω	V_{GS} = 0V, I_D = 0.1mA
V_{GS}	Gate-Source Voltage	-1		-2.3		-2.3		-2.3	V	V_{DG} = 15V, I_D = 200µA
$V_{GS(F)}$	Gate-Source Forward Voltage	0.7							V	IG = 1mA, V_{DS} = 0V
DYNAMIC										
g_{fs}	Common-Source Forward Transconductance	1.5	1	2	1	2	1	2	mS	VDG = 15V, I_D = 200µA f = 1kHz
g_{os}	Common-Source Output Conductance	1.3		2		2		2	µS	
g_{fs}	Common-Source Forward Transconductance	1.5	2	7	2	7	2	7		VDS = 10V, V_{GS} = 0V f = 1kHz
g_{os}	Common-Source Output Conductance	10		20		20		20		
C_{iss}	Common-Source Input Capacitance			8		8		8	pF	V_{DG} = 15V, I_D = 200µA f = 1MHz
C_{rss}	Common-Source Reverse Transfer Capacitance	1.5		3		3		3		
$\bar{e}_n$	Equivalent Input Noise Voltage	10		20		20		20	$nV/\sqrt{Hz}$	V_{DG} = 15V, I_D = 200µA f = 10Hz
MATCHING										
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage			15		20		40	mV	V_{DG} = 10V, I_D = 200µA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Change with Temperature			25		40		80	µV/ °C	T_A = -55 to 25°C, V_{DG} = 10V, I_D = 200µA
				25		40		80		T_A = 25 to 125°C, V_{DG} = 10V, I_D = 200µA
CMRR	Common Mode Rejection Ratio	102	95		90				dB	V_{DG} = 10 to 20V, I_D = 200µA

NOTES: 1. For design aid only, not subject to production testing.
2. Pulse test; PW = 300µs, duty cycle ≤ 3%.