Preliminary Data Sheet

CADEKA
Amplify the Human Experience

Comlinear™ CLC2000

High Output Current Dual Amplifier

FEATURES

- 9.4V_{pp} output drive into R_L=25Ω
- Using both amplifiers, 18.8V_{pp} differential output drive into R_L=50Ω
- ±200mA @ V_O=9.4V_{pp}
- 0.009%/0.06° differential gain/phase error
- 250MHz -3dB bandwidth at G = 2
- 510MHz -3dB bandwidth at G = 1
- 210V/µs slew rate
- 4.5nV/√Hz input voltage noise
- 2.7pA/√Hz input voltage noise
- 7mA supply current
- Fully specified at ±5V supplies
- Lead-free SOIC-8 package

APPLICATIONS

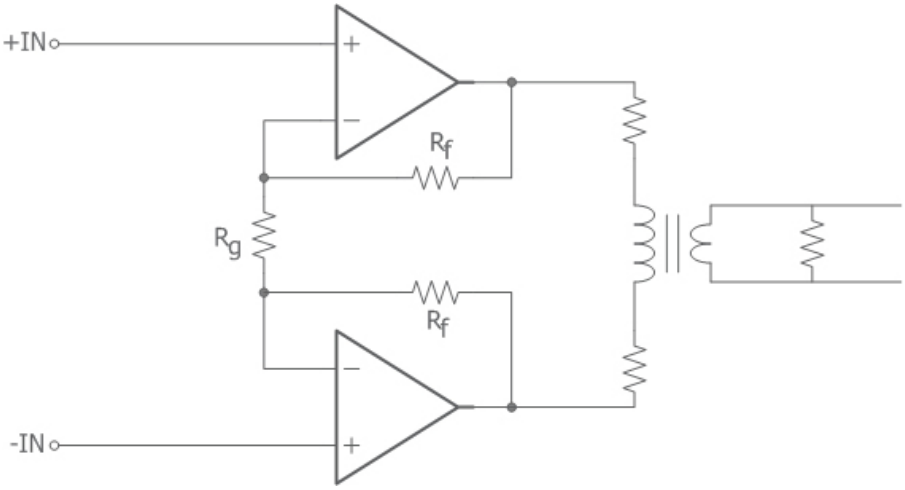
- ADSL PCI modem cards
- xDSL external modems
- Cable drivers
- Video line driver
- Twisted pair driver/receiver

General Description

The *Comlinear* CLC2000 is a dual voltage feedback amplifier that offers ±200mA of output current at 9.4V_{pp}. The CLC2000 is capable of driving signals to within 1V of the power rails. When connected as a differential line driver, the dual amplifier drives signals up to 18.8Vpp into a 25Ω load, which supports the peak upstream power levels for upstream full-rate ADSL applications.

The *Comlinear* CLC2000 can operate from single or dual supplies from 5V to 12V. It consumes only 7mA of supply current per channel. The combination of wide bandwidth, low noise, low distortion, and high output current capability makes the CLC2000 ideally suited for xDSL or video line driving applications.

Typical Application - ADSL Application

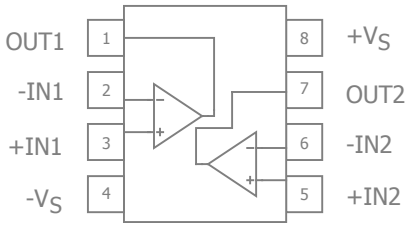


Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packaging Method
CLC2000ISO8X	SOIC-8	Yes	-40°C to +85°C	Reel
CLC2000ISO8	SOIC-8	Yes	-40°C to +85°C	Rail

Moisture sensitivity level for all parts is MSL-1.

CLC2000 Pin Configuration



CLC2000 Pin Assignments

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Parameter	Min	Max	Unit
Supply Voltage	0	14	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Package Thermal Resistance				
8-Lead SOIC		100		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOIC-8
Human Body Model (HBM)	4kV
Charged Device Model (CDM)	TBD

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	±2.5		±6.5	V

Electrical Characteristics

T_A = 25°C, V_S = 5V, R_f = R_g = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}, R_f = 0		422		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		236		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		68		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.2V_{pp}		77		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 2V step; (10% to 90%)		3.7		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		tbd		ns
OS	Overshoot	V_{OUT} = 0.2V step		6		%
SR	Slew Rate	2V step		200		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	2V_{pp}, 100KHz, R_L = 25Ω		-83		dBc
		2V_{pp}, 1MHz, R_L = 100Ω		-85		dBc
HD3	3rd Harmonic Distortion	2V_{pp}, 100KHz, R_L = 25Ω		-86		dBc
		2V_{pp}, 1MHz, R_L = 100Ω		-82		dBc
D_G	Differential Gain	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		tbd		%
D_P	Differential Phase	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		tbd		°
e_n	Input Voltage Noise	> 1MHz		4.2		nV/√Hz
i_n	Input Current Noise	> 1MHz		tbd		pA/√Hz
X_{TALK}	Crosstalk	Channel-to-channel 5MHz		-63		dB
DC Performance						
V_{IO}	Input Offset Voltage			0.3		mV
dV_{IO}	Average Drift			tbd		µV/°C
I_{IO}	Input Offset Current			0.2		µA
I_b	Input Bias Current			10		µA
dI_{bni}	Average Drift			tbd		nA/°C
PSRR	Power Supply Rejection Ratio	DC		81		dB
A_{OL}	Open-Loop Gain	R_L = 25Ω		76		dB
I_S	Supply Current	per channel		6.75		mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		tbd		MΩ
C_{IN}	Input Capacitance			tbd		pF
CMIR	Common Mode Input Range			0.4 to 4.6		V
CMRR	Common Mode Rejection Ratio	DC		80		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		tbd		mΩ
V_{OUT}	Output Voltage Swing	R_L = 25Ω		0.95 to 4.05		V
		R_L = 1kΩ		0.75 to 4.25		V
I_{OUT}	Output Current			tbd		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		tbd		mA

Electrical Characteristics

T_A = 25°C, V_S = 12V, R_f = R_g = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

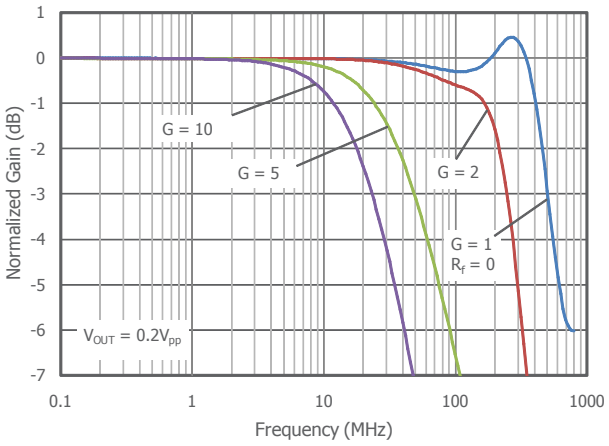
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}, R_f = 0		510		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		250		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 4V_{pp}		35		MHz
$BW_{0.1dB}$	0.1dB Gain Flatness	G = +2, V_{OUT} = 0.2V_{pp}		32		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 4V step; (10% to 90%)		13.3		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		tbd		ns
OS	Overshoot	V_{OUT} = 0.2V step		2		%
SR	Slew Rate	4V step		210		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	2V_{pp}, 100KHz, R_L = 25Ω		-84		dBc
		2V_{pp}, 1MHz, R_L = 100Ω		-86		dBc
		8.4V_{pp}, 100KHz, R_L = 25Ω		-63		dBc
		8.4V_{pp}, 1MHz, R_L = 100Ω		-82		dBc
HD3	3rd Harmonic Distortion	2V_{pp}, 100KHz, R_L = 25Ω		-88		dBc
		2V_{pp}, 1MHz, R_L = 100Ω		-80		dBc
		8.4V_{pp}, 100KHz, R_L = 25Ω		-63		dBc
		8.4V_{pp}, 1MHz, R_L = 100Ω		-83		dBc
D_G	Differential Gain	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.009		%
D_P	Differential Phase	NTSC (3.58MHz), DC-coupled, R_L = 150Ω		0.06		°
e_n	Input Voltage Noise	> 1MHz		4.5		nV/√Hz
i_n	Input Current Noise	> 1MHz		2.7		pA/√Hz
X_{TALK}	Crosstalk	Channel-to-channel 5MHz		-62		dB
DC Performance						
V_{IO}	Input Offset Voltage(1)		-4.2	0.3	4.2	mV
dV_{IO}	Average Drift			tbd		µV/°C
I_{IO}	Input Offset Current(1)		-2	0.2	2	µA
I_b	Input Bias Current(1)			10	20	µA
dI_{bni}	Average Drift			tbd		nA/°C
PSRR	Power Supply Rejection Ratio(1)	DC	73	81		dB
A_{OL}	Open-Loop Gain	R_L = 25		76		dB
I_S	Supply Current(1)	per channel		7	9	mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		tbd		MΩ
C_{IN}	Input Capacitance			tbd		pF
CMIR	Common Mode Input Range			0.6 to 11.4		V
CMRR	Common Mode Rejection Ratio(1)	DC	70	79		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		tbd		mΩ
V_{OUT}	Output Voltage Swing	R_L = 25Ω (1)	1.5	1.2 to 10.8	10.5	V
		R_L = 1kΩ		0.8 to 11.2		V
I_{OUT}	Output Current			tbd		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_S / 2		1000		mA

Notes:
1. 100% tested at 25°C

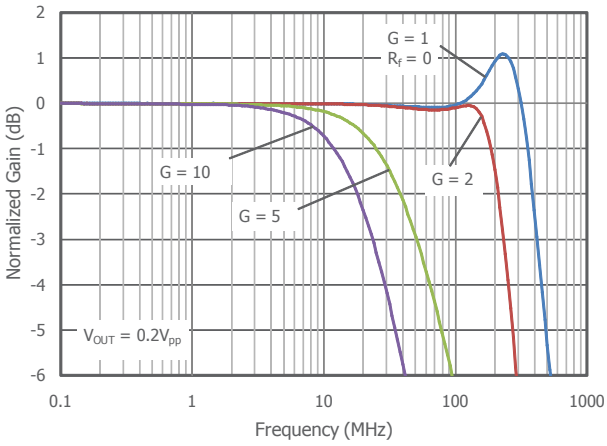
Typical Performance Characteristics

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

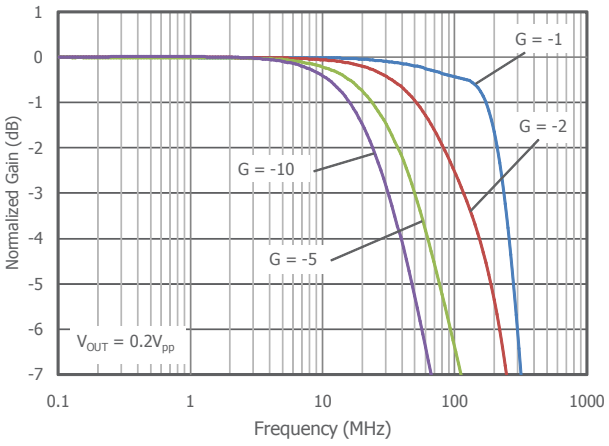
Non-Inverting Frequency Response



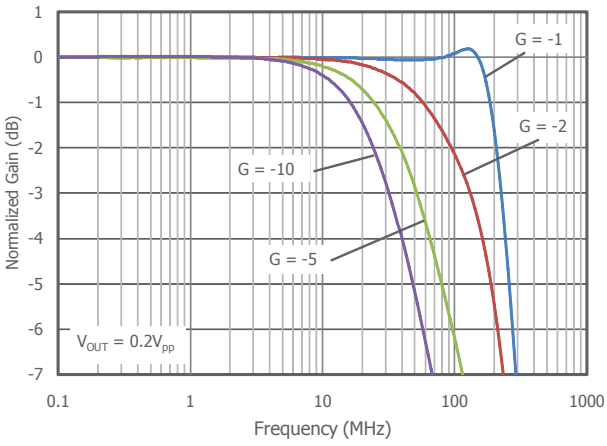
Non-Inverting Frequency Response (V_S=5V)



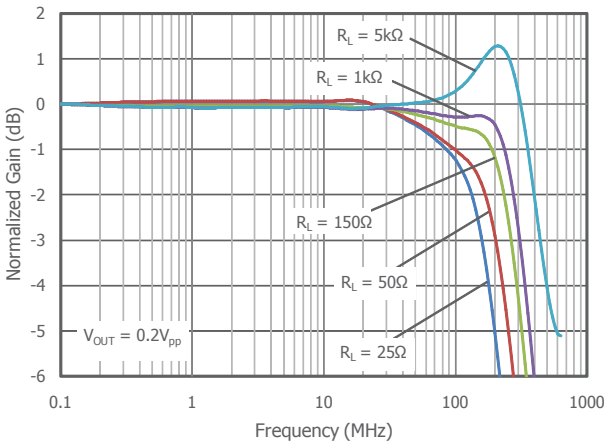
Inverting Frequency Response



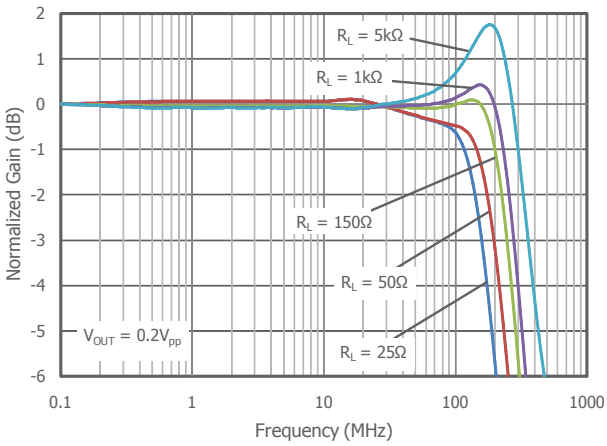
Inverting Frequency Response (V_S=5V)



Frequency Response vs. R_L



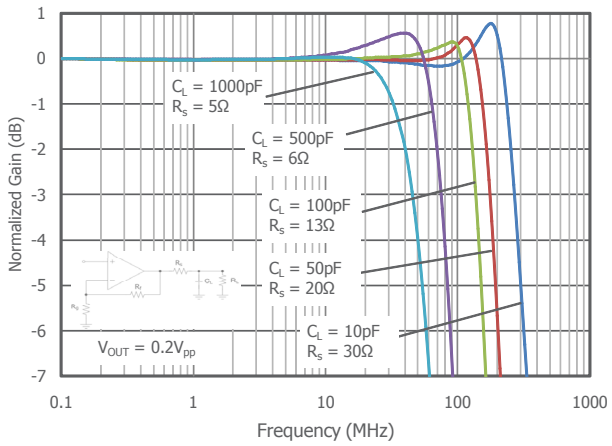
Frequency vs. R_L (V_S = 5V)



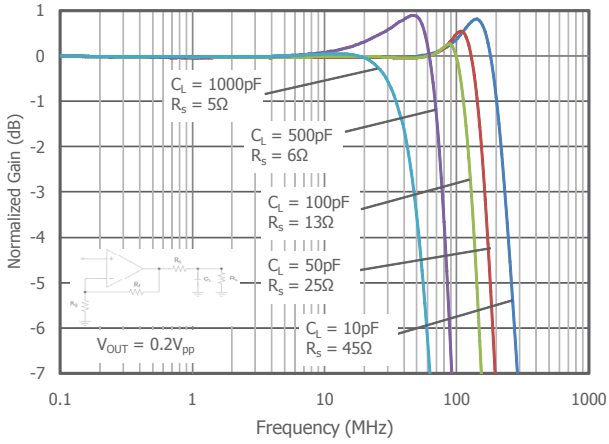
Typical Performance Characteristics

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

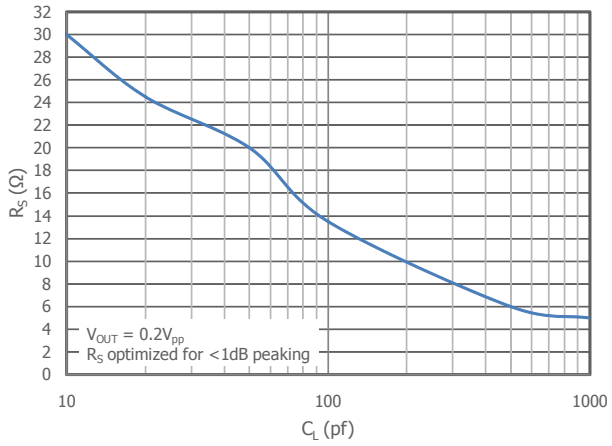
Frequency vs. C_L



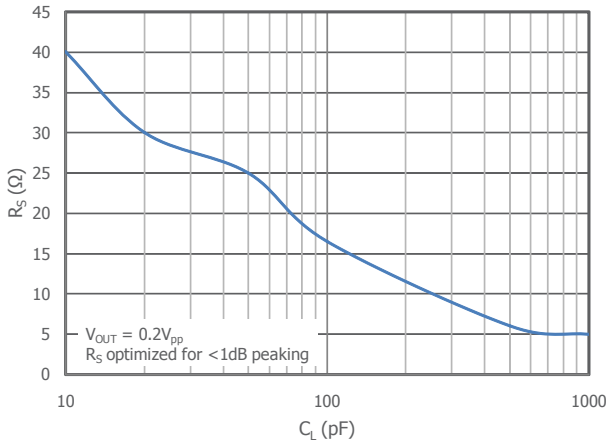
Frequency vs. C_L (V_S = 5V)



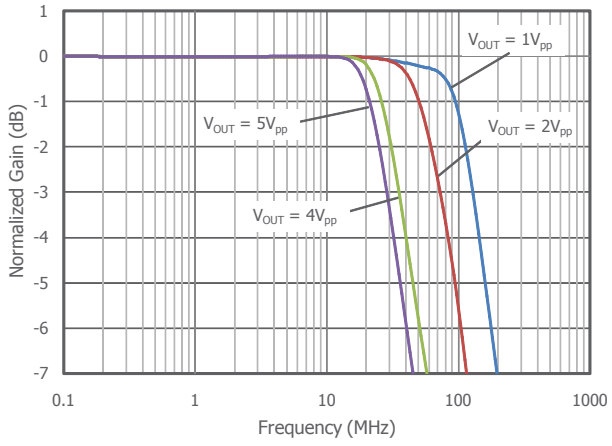
Recommended R_S vs. C_L



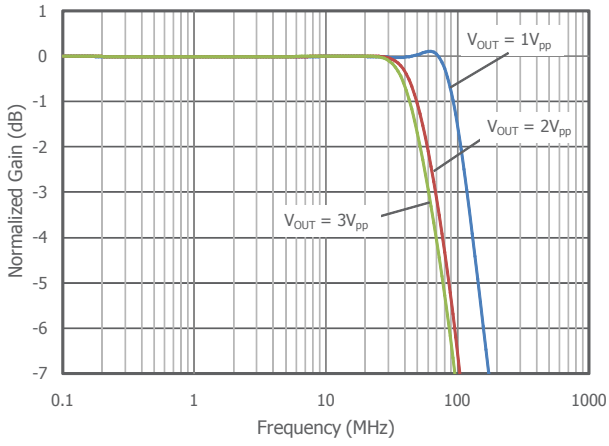
Recommended R_S vs. C_L (V_S = 5V)



Frequency Response vs. V_{OUT}



Frequency Response vs. V_{OUT} (V_S = 5V)



Typical Performance Characteristics - Continued

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

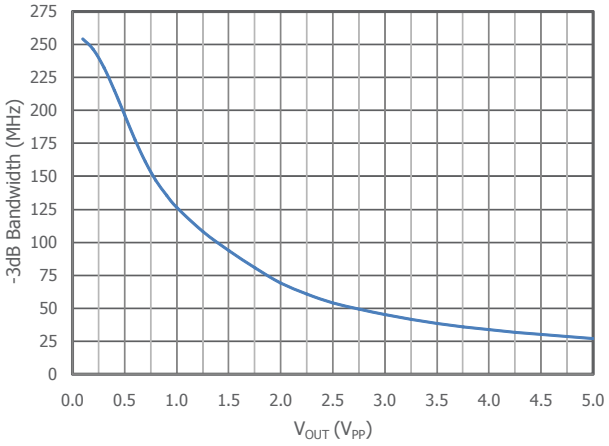
Frequency Response vs. Temperature

TBD

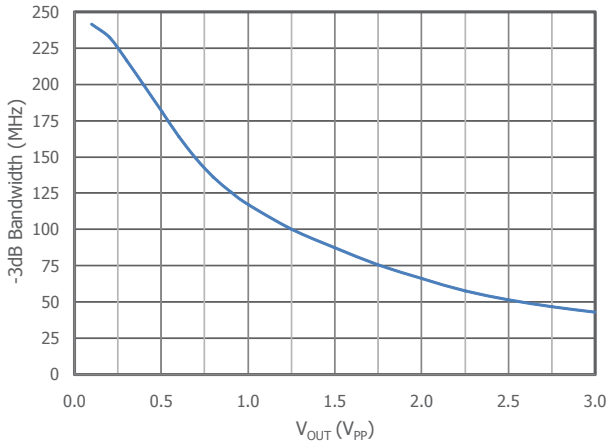
Frequency vs. Temperature (V_S = 5V)

TBD

-3dB Bandwidth vs. Output Voltage



-3dB Bandwidth vs. Output Voltage (V_S=5V)



Open Loop Transimpendance Gain/Phase vs. Frequency

TBD

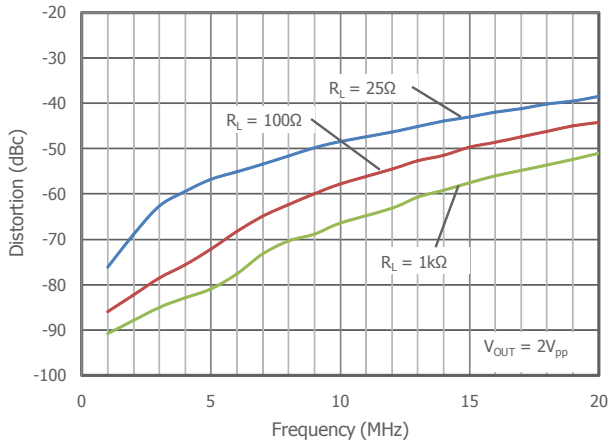
Input Voltage Noise

TBD

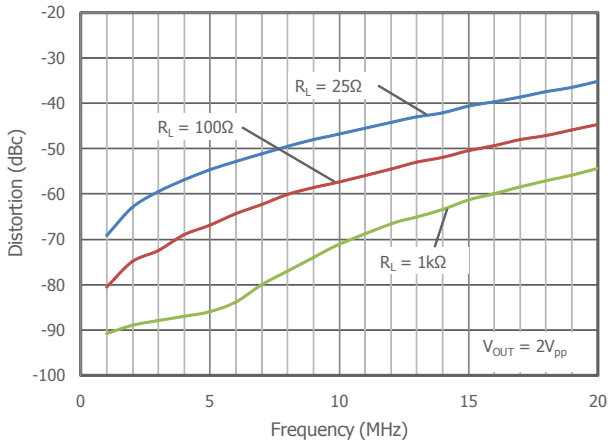
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

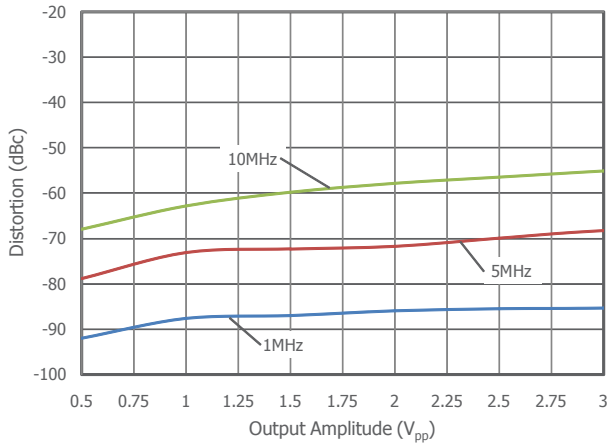
2nd Harmonic Distortion vs. R_L



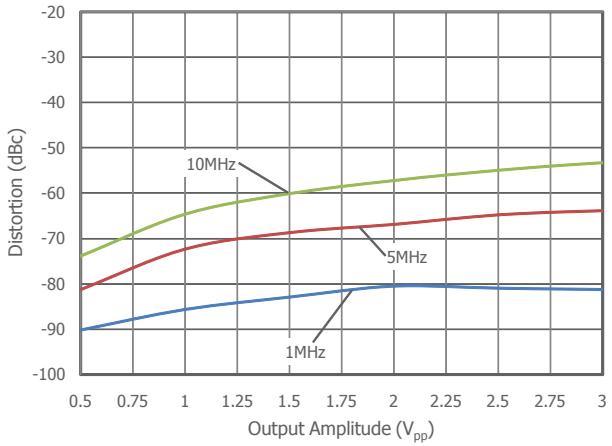
3rd Harmonic Distortion vs. R_L



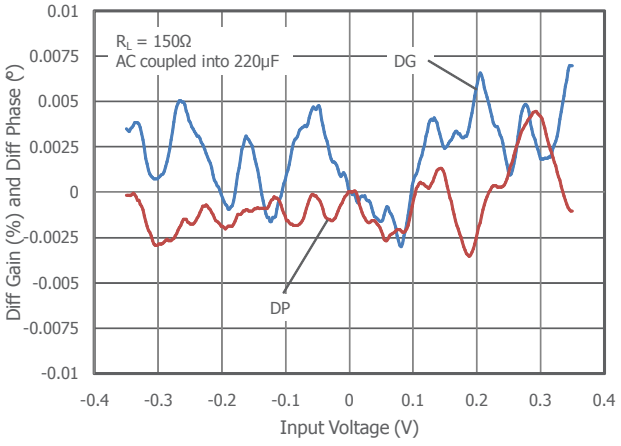
2nd Harmonic Distortion vs. V_{OUT}



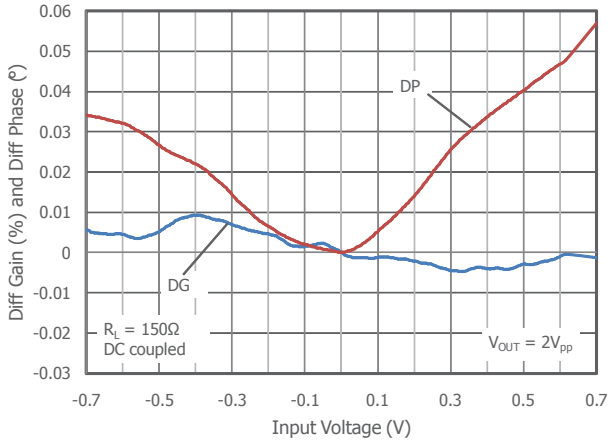
3rd Harmonic Distortion vs. V_{OUT}



Differential Gain & Phase AC Coupled



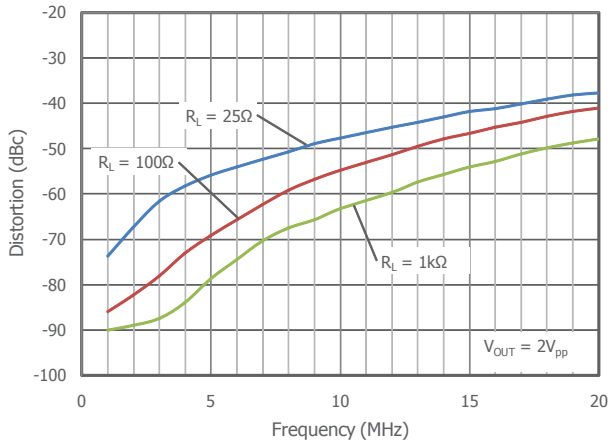
Differential Gain & Phase DC Coupled



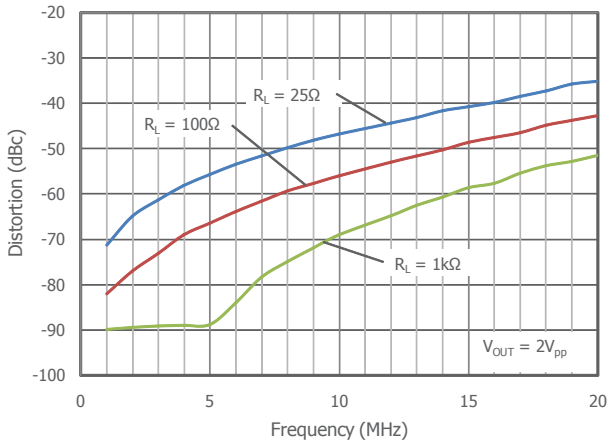
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

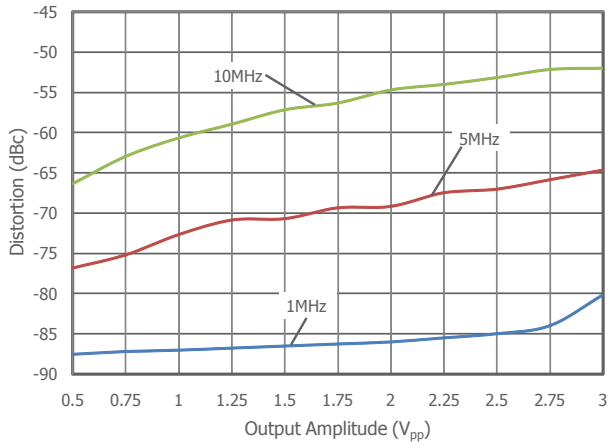
2nd Harmonic Distortion vs. R_L (V_S=5V)



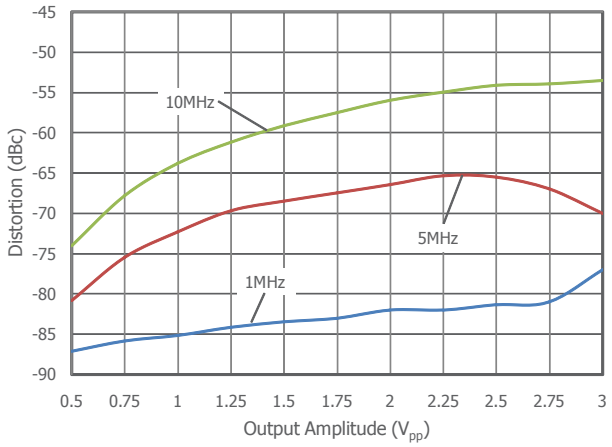
3rd Harmonic Distortion vs. R_L (V_S=5V)



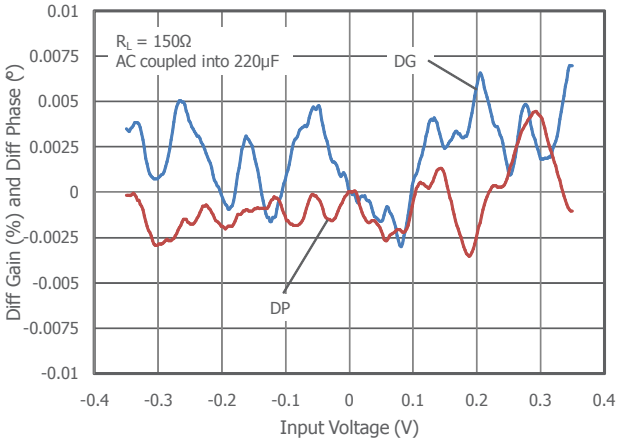
2nd Harmonic Distortion vs. V_{OUT} (V_S=5V)



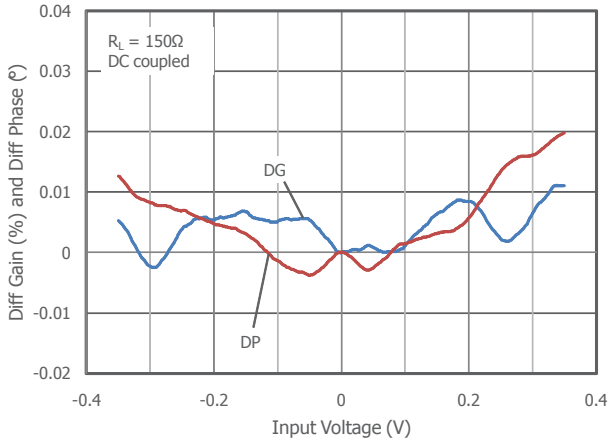
3rd Harmonic Distortion vs. V_{OUT} (V_S=5V)



Differential Gain & Phase AC Coupled (V_S=5V)



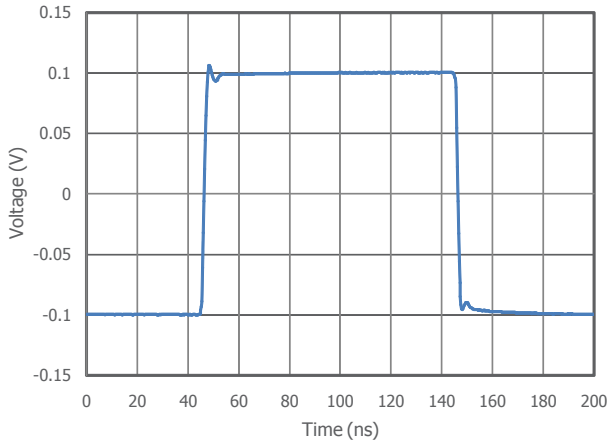
Differential Gain & Phase DC Coupled (V_S=5V)



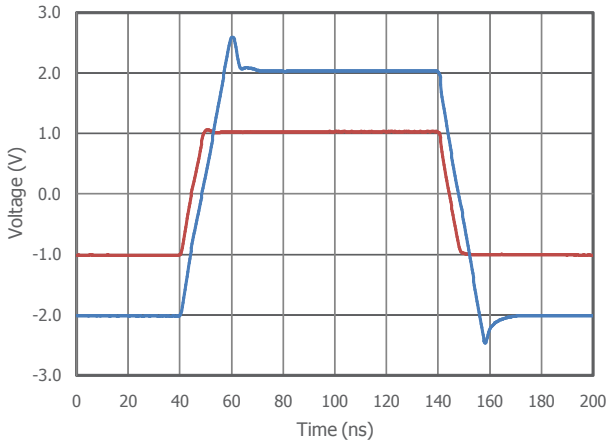
Typical Performance Characteristics - Continued

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

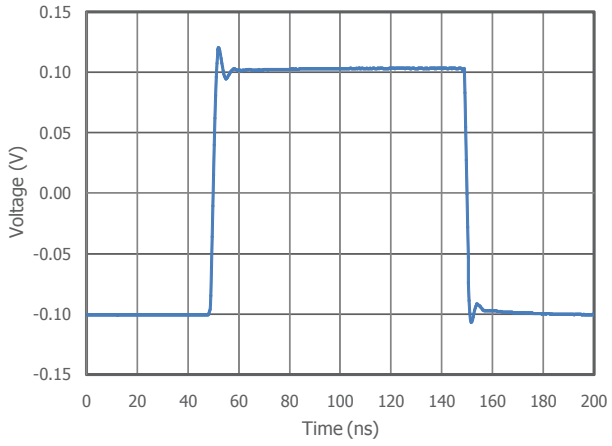
Small Signal Pulse Response



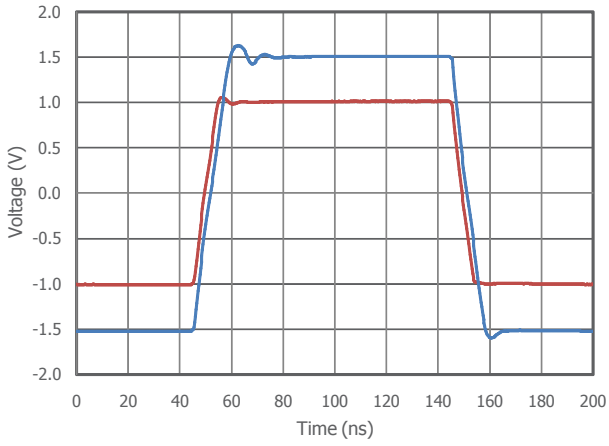
Large Signal Pulse Response



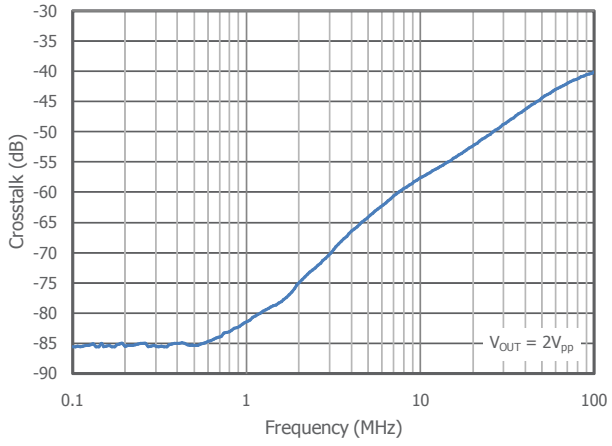
Small Signal Pulse Response (V_S=5V)



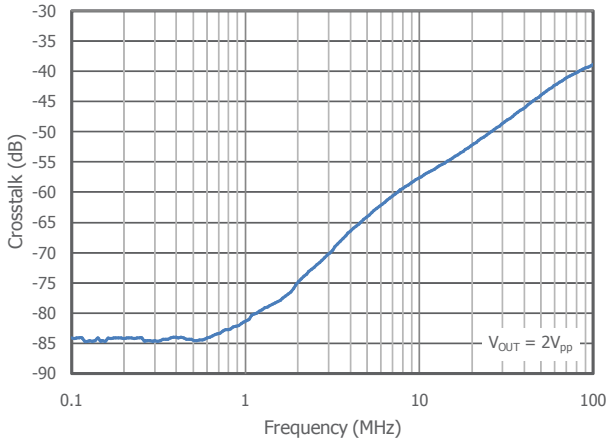
Large Signal Pulse Response (V_S=5V)



Crosstalk vs. Frequency



Crosstalk vs. Frequency (V_S=5V)



Typical Performance Characteristics - Continued

T_A = 25°C, V_S = 12V, R_f = 510Ω, R_L = 100Ω to V_S/2, G = 2; unless otherwise noted.

Closed Loop Output Impedance vs. Frequency

TBD

CMRR vs. Frequency

TBD

PSRR vs. Frequency

TBD

Application Information

Driving Capacitive Loads

The Frequency Response vs. C_L plot on page 5, illustrates the response of the CLC2000 Family. A small series resistance (R_S) at the output of the amplifier, illustrated in Figure 1, will improve stability and settling performance. Rs values in the Frequency Response vs. C_L plot were chosen to achieve maximum bandwidth with less than 1dB of peaking. For maximum flatness, use a larger R_S.

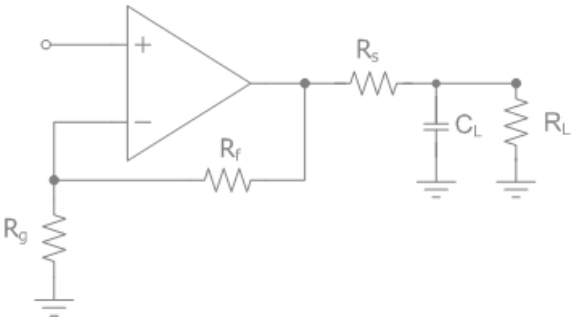


Figure 1. Typical Topology for Driving Capacitive Loads

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C for an extended time, device failure may occur. The CLC2000 are short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. RMS Power Dissipation can be calculated using the following equation:

$$\text{Power Dissipation} = I_S * (V_{S+} - V_{S-}) + (V_{S+} - V_O(\text{RMS})) * I_{OUT}(\text{RMS})$$

Where I_S is the supply current, V_{S+} is the positive supply pin voltage, V_{S-} is the negative supply pin voltage, V_O(RMS) is the RMS output voltage and I_{OUT}(RMS) is the RMS output current delivered to the load. Follow the maximum power derating curves shown in Figure 2 to ensure proper operation.

TBD

Figure 2. Maximum Power Derating

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The CLC2000 Family will typically recover in less than 20ns from an overdrive condition. Figure 3 shows the CLC2000 in an overdriven condition.

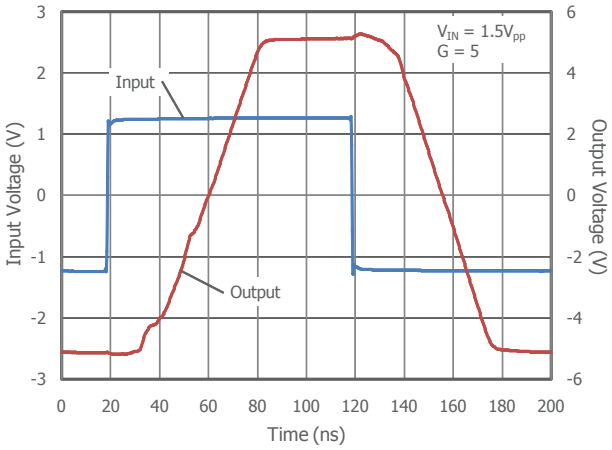


Figure 3. Overdrive Recovery

Video Over Twisted Pair

Several applications require video signals to be transmitted from point A to point B. In these applications, three twisted pairs are used to carry the red, green, and blue (RGB) video signals. Category-3 (CAT-3) unshielded twisted pair (UTP) cable is an economical solution for transmitting video signals, but introduces the most loss compared

to CAT-5 or coaxial cable. Figures 4 and 5 illustrate a low cost video driver/receiver that utilizes the CLC2000 dual amplifier and is capable of driving 3,000ft of CAT-3 UTP. The CLC2000 provides excellent video specifications. It offers extremely low differential gain and phase (TBD%/ TBD°) and 0.1dB gain flatness to TBDMHz for superb standard definition video performance. The output drive capability, TBDmA, effortlessly drives the 100Ω impedance of the twisted pair cable.

TBD

Figure 4. Differential Video Driver

Figure 5. Differential Video Receiver

In this circuit, the first CLC2000 is used to convert a $1V_{pp}$ single-ended signal to a differential signal in order to drive the twisted pair. The two 50Ω resistors are needed to match the characteristic impedance of the UTP. The second CLC2000 is used to convert the differential signal transmitted by the twisted pair into a single ended $1V_{pp}$ signal and compensate for the attenuation caused by the CAT-3 cable. R2 compensates for the signal loss caused by the twisted pair and is adjusted so the overall gain of the system is one. C1 and R1 form a simple equalizer and compensate for the high frequency attenuation introduced by the twisted pair. The 2 examples below show optimum component values for 1,000ft and 3,000ft of CAT-3 cable. For these examples the component values were selected to provide optimal rise/fall times, magnitude, and damping of a $1V_{pp}$ square wave input.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Fairchild has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.01µF ceramic capacitors
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.01µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

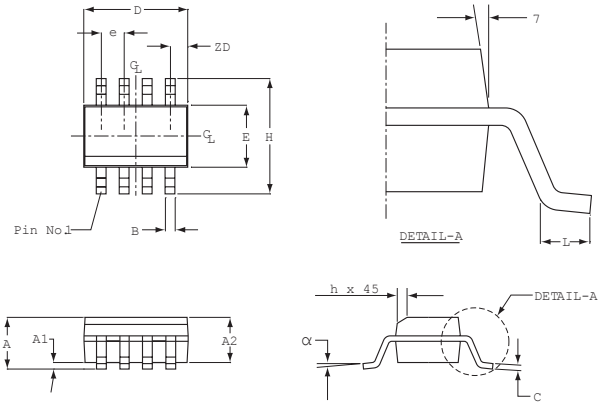
The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB006	CLC2000

Evalutaion Board Schematics

Mechanical Dimensions

SOIC-8 Package



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
	0°	8°
ZD	0.51 ref	
A2	1.37	1.57

NOTE:
1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.10mm (.004") max.
3. Package surface finishing:
   (3.1) Top: matte (charmilles #18~30).
   (3.2) All sides: matte (charmilles #18~30).
   (3.3) Bottom: smooth or matte (charmilles #18~30).
4. All dimensions excluding mold flashes and ext flash from the package body shall not exceed 0.152mm (.006) per side (D).

For additional information regarding our products, please visit CADEKA at: cadeka.com

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