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Data sheet

1. Short description

The power stage control module CY 220B controls time-dependently the power stage transistors of the injectors (solenoid valves MV) of a common rail diesel engine (1 ... 8 cylinders). Based on a 2-bank structure with 2 x 4 outputs, overlapping injection is possible, i.e. one power stage of each bank can be activated simultaneously (by switching 1 x n operation is also possible, n = 1 ... 8).

CY 220Bis controlled for example by a component (CC5xx or GAD4x) which presets the time control of the power stages and the individual phases of the injection with three signals ONx, MODEx, RCHGx as well as determining the selection of the power stage with the YSELxy signals.

The control of a Booster FET (voltage booster) is also realized. If the recovered switch off energy of an injector is insufficient for the boost (iron losses in the injector) further energy must be pumped into the booster capacitor (CBOOS) by a recharging phase. This is achieved by controlling a power stage up to a certain current level so that no pulling up of the injector is possible with subsequent fast decay to the booster capacitor.

The IC monitors the output stages for overcurrent and load drop and checks the function of the fast decay. The error data can be read out serially. Coding is compatible with the other components (e.g. CJ401)

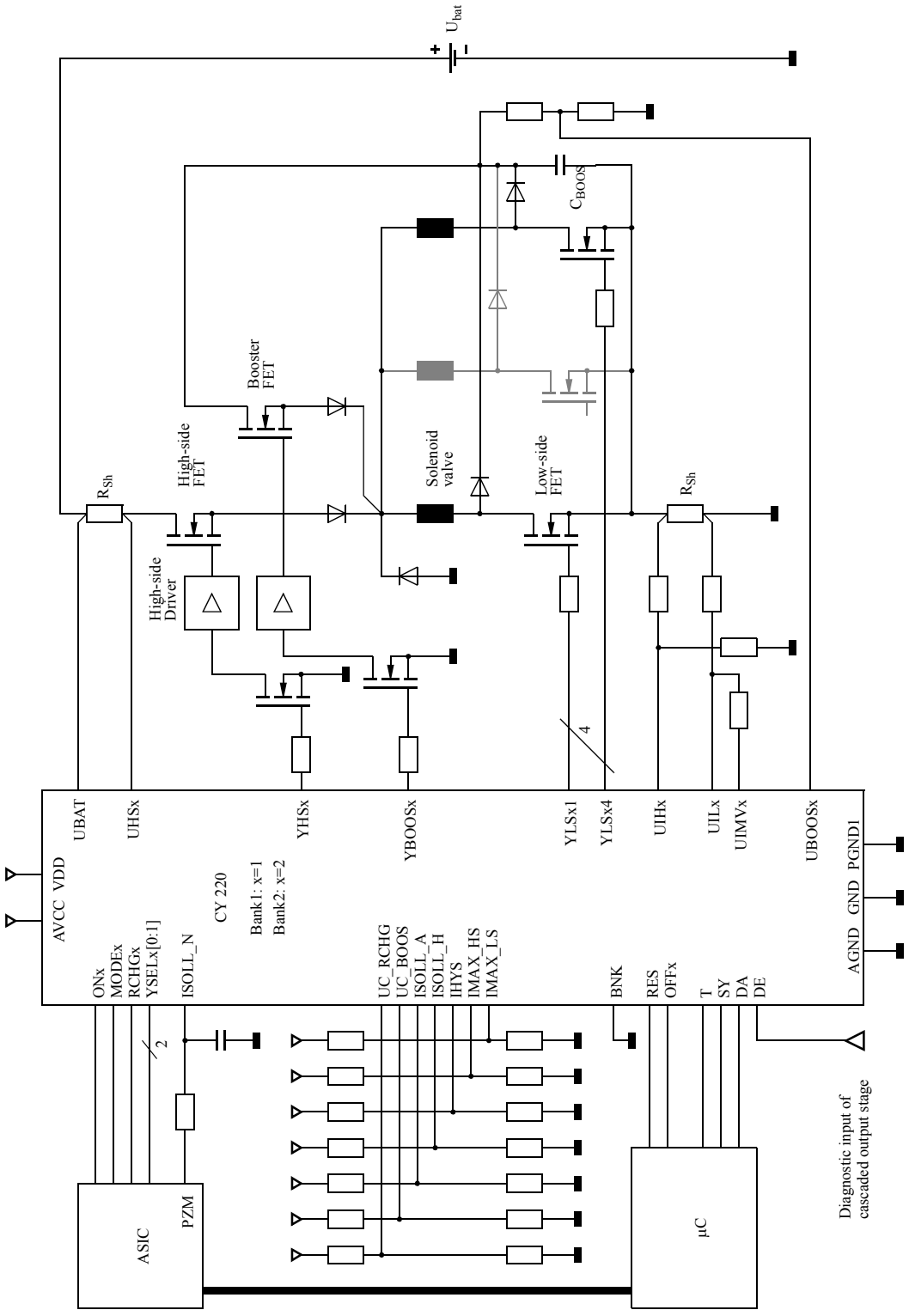
Features and modules:

Power-On switch off for power stage driver
Presets of start, hold and recharging current level, short-circuit current HS/LS
Preset of hysteresis for two-point current regulation
Monitoring of the booster voltage (discharge and recharge voltage)
Preset discharge/recharge voltage
Diagnosis: Error types: Short-circuit to U_{BAT} (low-side protection)
Short-circuit to ground (high-side protection)
load drop
Fast decay error
Error transmission via serial interface coded according to location and type
Cascadable diagnostic interface
Error cut-off of output stages and direct message to the computer
Emergency cut-off of every single bank by controller
8 x low-side power stage drivers (2 x 4 or 1 x 8)
2 x high-side power stage drivers
2 x booster power stage drivers
2 x differential amplifier for MV current measuring at the measuring shunt
2 x current comparators for two-point current regulation
2 x voltage monitoring booster capacitor

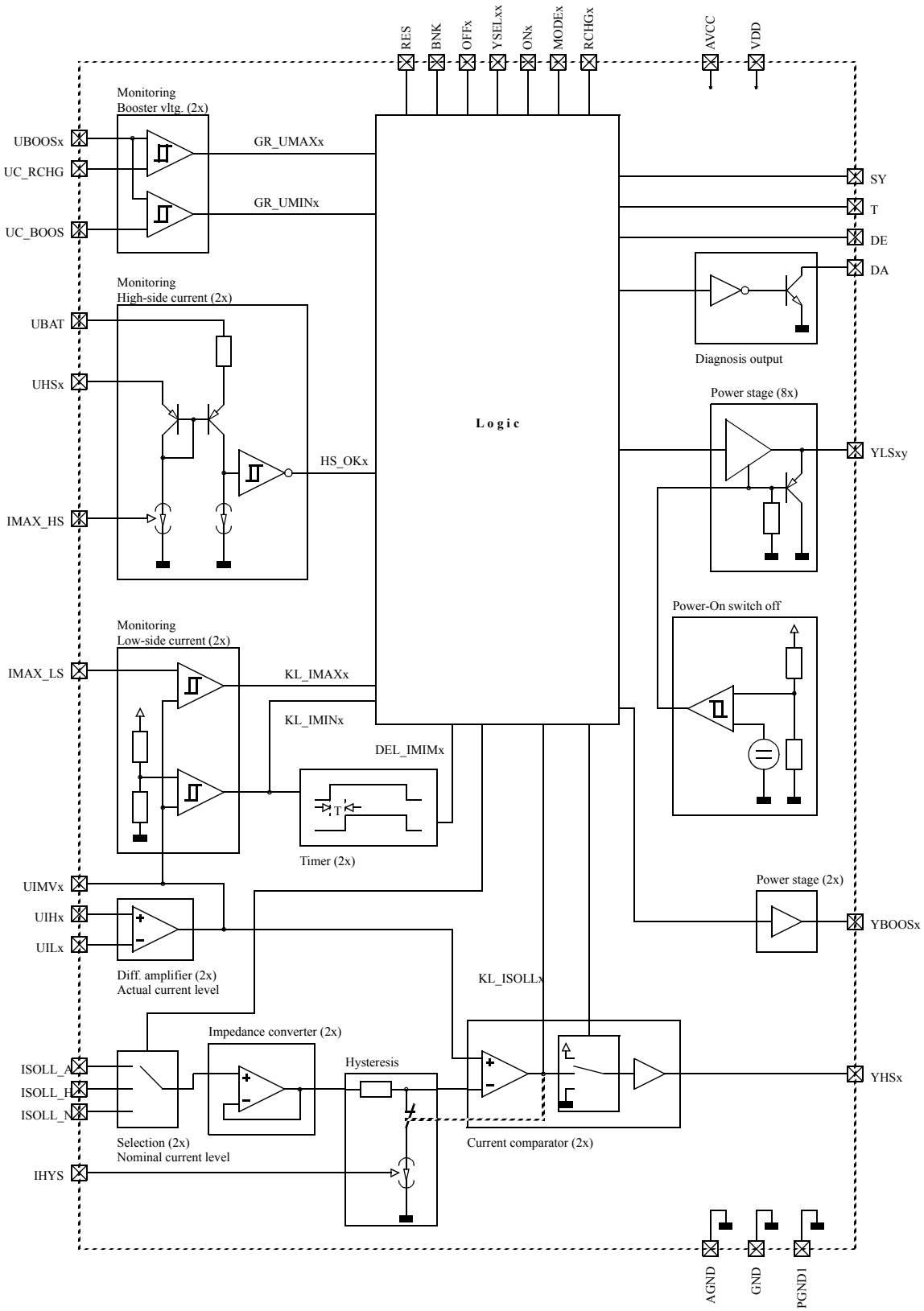
2. Functional description

2.1. Application circuit

Power stage electronics shown for one bank only



2.2. Block diagram



2.3. General information

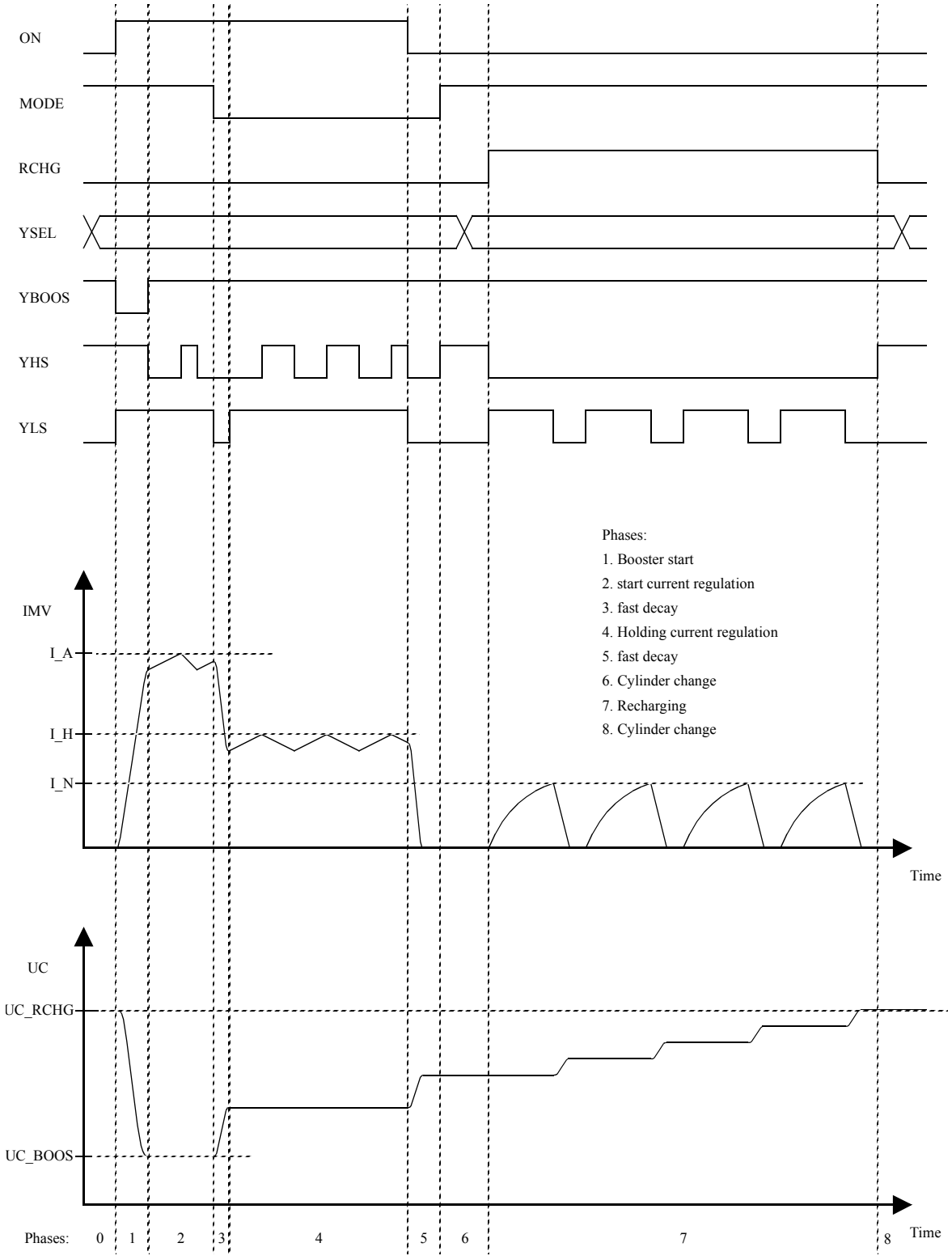
Regulation:
The IC contains a two-point current regulation with adjustable hysteresis IHYS. The set-points for start current ISOLL_A, holding current ISOLL_H and recharging current ISOLL_N can be preset externally. The hysteresis IHYS acts on the start and holding current control. The lower current value IMIN applies for the recharging process.

Low-side FET control:
The Low-side FET to be controlled is selected by binary coded address lines YSELxy. The selected FET is conduction statically during two-point regulation. The fast decay is triggered by switch off the Low-side FET. This happens during the recharging phase and also during the injection phase in the transition start to holding current or holding current to zero.

High-side FET control:
The High-side FET is used as a switch for the two-point current regulation. The High-side FET is conducting during the recharging and fast decay phase.

Control Booster FET:
The Booster FET is used as a switch for the booster operation. It is non- conducting during the other phases.

2.4. Timing diagram



2.5. Timing process

Phase 0: Cylinder change
- The power stage is switched off because both the High-side, Low-side and Booster FET are switched off YHSx=1, YLSxy=0, YBOOSx=1.
- The valid low-side power stage valid for the following injection phase is selected by the select logic YSELxy.

Phase 1: Booster start
- The Low-side FET is activated: YLSxy=1.
- The solenoid valve is switched to the booster capacitor by the Booster FET: YBOOSx=0.
- The High-side FET remains inactive: YHSx=1.
- Phase 1 is finished when the measured booster voltage at pin UBOOSx drops below the threshold UC_BOOS (discharge voltage).

Phase 2: start current regulation
- The MV current is now taken over by the High-side FET and booster operation is deactivated. YHSx=0 / YBOOSx=1.
- On reaching the setpoint ISOLL_A the High-side FET is switched off (free-running) and enabled again on dropping below the hysteresis. (Remark: HYS is calculated from HYS = IHYS / 6).
- Phase 2 is finished when an edge change from 1 ->0 takes place at the MODE pin.

Phase 3: First fast decay
- For the fast decay the Low-side FET is switched off and the High-side FET switched on. YLSxy=0 / YHSx=0.
- Phase 3 is finished when the hold current is droped below ISOLL_H less hysteresis IHYS/6.

Phase 4: Holding current regulation
- High-side FET and Low-side FET are switched on: YHSx=0 / YLSxy=1.
- On reaching the current setpoint ISOLL_H the High-side FET is switched off (free-running) and enabled again on dropping below the hysteresis (ISOLL_H – HYS).
- Phase 4 is finished when the injection process is completed: ONx=0.

Phase 5: Second fast decay
- For the fast decay the Low-side FET is switched off and the High-side FET switched on: YLSxy=0 / YHSx=0.
- The edge change from 0 -> 1 at the MODE signal ends phase 5 as well the injection process.
- The fast decay check is also performed with the edge change (UIMVx < IMIN ?; IMIN is an internal current threshold).
- High Side FET is switched off: YHSx=1.

Phase 6: Cylinder change
- Another power stage in the same bank can be switched to with YSELxy.

Phase 7: Recharging
- Recharging is enabled by RCHGx=1. High-side FET and Low-side FET are switched on: YHSx=0, YLSxy=1.
- On reaching the current setpoint ISOLL_N the Low-side FET is switched off (fast decay): YLSxy=0.
- On dropping below the internal current threshold IMIN a new recharging is enabled after a delay of 10 us: YLSxy=1.
- This procedure is repeated until the voltage setpoint UC_RCHG (recharging voltage) is reached on the booster capacitor or the recharging permission is rescinded: RCHGx=0. If the voltage setpoint is not reached again during the recharging allowed by RCHGx=1, recharging begins again. Resetting of RCHGx always causes a recharging process to be ended immediately: YHSx=1, YLSxy=0.

Phase 8: Cylinder change
- Another power stage in the same bank can be switched to with YSELxy.

2.6. Special features of the timing process

- When the power stage is switched off by OFFx, switching off takes place immediately. It can only be enabled again at the next positive ONx or RCHGx edge.

- An injection process begins with the positive ONx edge and ends with the positive MODEx edge.

- A recharging process begins with the positive RCHGx edge and ends with the negative RCHGx edge.

- The RCHG signal is ignored during an injection process, the ON/MODE signal during a recharging process.

- In pre- and post-injection the holding current regulation can be omitted, i.e. MODEx switches over from 1 to 0 at the same time as ONx.

- An ongoing recharging process can be aborted by a new injection. To do this the control module (CCxx or GADxx) should change the signals in the order RCHG, YSEL, ON but at least simultaneously (stable signals).

- In systems without voltage boosting the booster phase can be suppressed after ONx=1 by connecting UC_BOOS > UBOOSx.

- A rise in the booster voltage after the booster phase does not lead to a new booster operation.

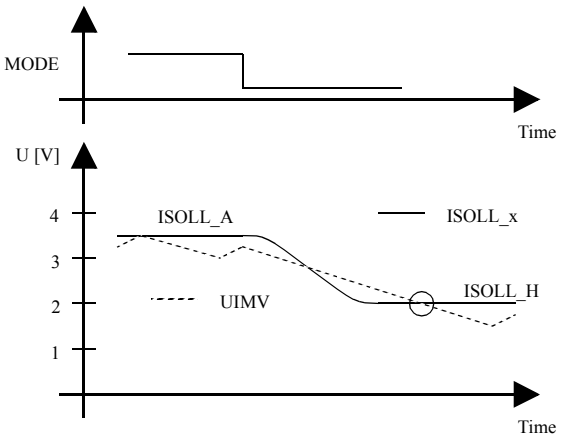
- Slow discharging of the booster capacitance within a recharging process leads to a new recharging process.

- A new active ONx or RCHGx signal will only be recognized as valid when the current from the previous process (recharging or injection) has dropped below the threshold IMIN.

- A cylinder change is only accepted between two processes (recharging or injection), i.e. after the positive MODEx edge or negative RCHGx edge (and zero current) and before the next positive RCHG or ON edge.

- The current regulation of the recharging takes place between ISOLL_N as the upper value and IMIN plus a time delay of approx. 10us.

- The change in current in the MV during fast decay of ISOLL_A to ISOLL_H must be smaller than the switching speed of the nominal current multiplexer (see figure). If the actual value UIMVx drops below the setpoint ISOLL_H, the process control interrupts the fast decay (see figure, circle). If this change is not reached (change in current in the MV faster than switching speed of the current multiplexer), the fast decay is interrupted with certainty on dropping below the current level IMIN.



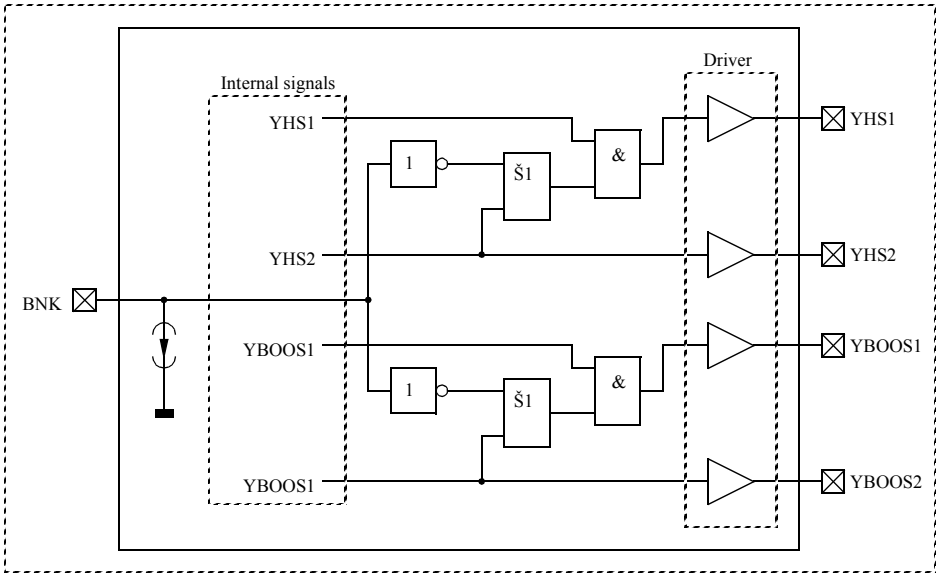
3. Effects RES, OFFx

A Low signal at RES affects Bank1 **and** Bank2.
A Low signal at OFFx **only** affects bank x.

Function	RES=0	OFF1=0	OFF2=0
Low-side Bank1, YLS1x	0	0	-
Low-side Bank2, YLS2x	0	-	0
High-Side Bank1 YHS1	1	1	-
High-Side Bank2 YHS2	1	-	1
Booster Bank1 YHS1	1	1	-
Booster Bank2 YHS2	1	-	1
Error buffer 1	reset	reset	-
Error buffer 2	reset	-	reset
Process control Bank1	reset	-	-
Process control Bank2	reset	-	-
Diagnosis register	reset Status: FF error-free	-	-

4. 1/2-bank operation

With the BNK input the component can be switched from 2-bank operation to 1-bank operation. With a high signal at BNK the outputs YHS2 and YBOOS2 are switched respectively to the outputs of the first bank (YHS1 or YBOOS1) additionally. The logic operation is an OR (see also the structure diagram below). This simplifies the external wiring of the high-side and booster control.



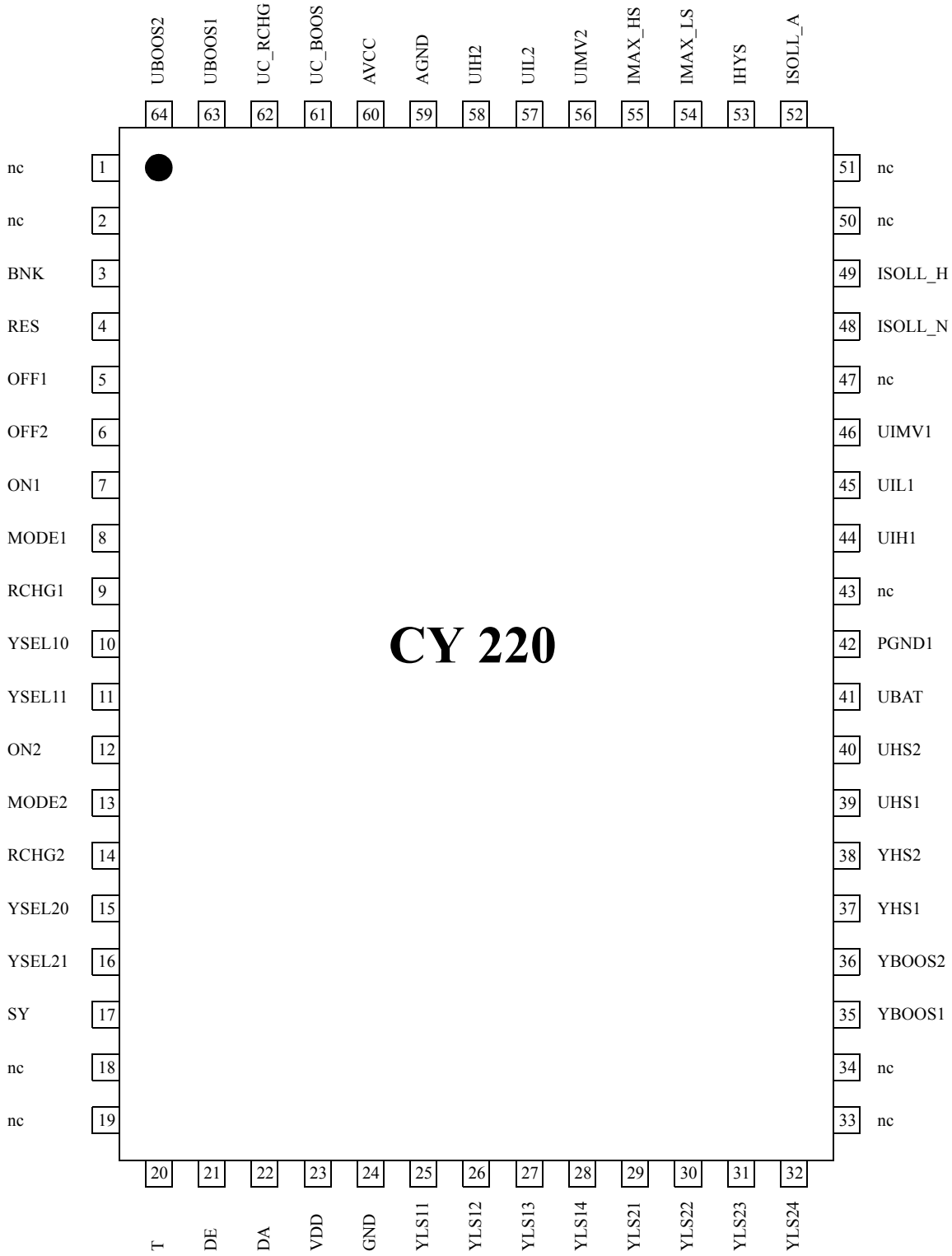
All other inputs and outputs must still be switched in 1-bank operation analogously with 2-bank operation. The differential amplifier for current measuring Bank2 must be switched to the measuring shunt of Bank1. The same applies for the high-side current monitoring and the booster voltage monitoring. The control signals ONx, MODEx, RCHGx, YSELxy must be fed in separately and must be controlled according to the cylinder selection.

If one bank is to be deactivated completely, the Bank2 must be switched as follows for example.

Pin	Connection
UBOOS2, UIH2 OFF2, ON2, RCHG2	GND
MODE2	VDD
UHS2	UBAT
UIL2	over about 25k to VDD
UIMV2 YLS2x, YHS2, YBOOS2	open

5. Configuration of connections

5.1. Packing MQFP 64



5.2. Description of connections

Number	Name	Level	Input/ Output	Int. current source	Function
1	nc				
2	nc				
3	BNK	logic	E	down	Switching 1/2-bank operation HIGH: 1 bank à 8 power stages LOW: 2 bank à 4 power stages
4	RES	logic	E	down	Reset signal HIGH: Normal operation LOW: RESET
5	OFF1	logic	E	down	Asynchronous switch off signal Bank1 HIGH: Power stages in operation LOW: Power stages switched off
6	OFF2	logic	E	down	Asynchronous switch off signal Bank2 HIGH: Power stages in operation LOW: Power stages switched off
7	ON1	logic	E	down	Control signal injection Bank1 HIGH: Injection LOW: No injection
8	MODE1	logic	E	up	Control signal current level Bank1 HIGH: Booster operation/start current regulation. LOW: Holding current regulation./fast decay
9	RCHG1	logic	E	down	Control signal recharging Bank1 HIGH: Recharging allowed LOW: No recharging allowed
10	YSEL10	logic	E	up	Cylinder selection bit 0 Bank1
11	YSEL11	logic	E	up	Cylinder selection bit 1 Bank1
12	ON2	logic	E	down	Control signal injection Bank2 HIGH: Injection LOW: no injection
13	MODE2	logic	E	up	Control signal current level Bank2 HIGH: Booster operation/start current regulation LOW: Hold current regulation./fast decay
14	RCHG2	logic	E	down	Control signal recharging Bank2 HIGH: Recharging allowed LOW: no recharging allowed
15	YSEL20	logic	E	up	Cylinder selection bit 0 Bank2
16	YSEL21	logic	E	up	Cylinder selection bit 1 Bank2
17	SY	logic	E	up	Synchronisation diagnosis interface
18	nc				

Number	Name	Level	Input/ Output	Int. current source	Function
19	nc				
20	T	logic	E	up	Clock diagnosis interface
21	DE	logic	E	up	Data input diagnosis interface
22	DA	open C.	A	-	Data output diagnosis interface
23	VDD				Supply logic/driver
24	GND				Supply logic/driver
25	YLS11	0V / 5V	A	-	Driver for LS-FET cylinder 1 Bank1
26	YLS12	0V / 5V	A	-	Driver for LS-FET cylinder 2 Bank1
27	YLS13	0V / 5V	A	-	Driver for LS-FET cylinder 3 Bank1
28	YLS14	0V / 5V	A	-	Driver for LS-FET cylinder 4 Bank1
29	YLS21	0V / 5V	A	-	Driver for LS-FET cylinder 1 Bank2
30	YLS22	0V / 5V	A	-	Driver for LS-FET cylinder 2 Bank2
31	YLS23	0V / 5V	A	-	Driver for LS-FET cylinder 3 Bank2
32	YLS24	0V / 5V	A	-	Driver for LS-FET cylinder 4 Bank2
33	nc				
34	nc				
35	YBOOS1	0V / 5V	A	-	Output for driver booster FET Bank1
36	YBOOS2	0V / 5V	A	-	Output for driver booster FET Bank2
37	YHS1	0V / 5V	A	-	Output for driver booster HS-FET Bank1
38	YHS2	0V / 5V	A	-	Output for driver booster HS-FET Bank2
39	UHS1	analogous	E	-	Measuring input high-side shunt Bank1
40	UHS2	analogous	E	-	Measuring input high-side shunt Bank2
41	UBAT	analogous	E	-	Measuring input high-side shunt Bank1/2
42	PGND1			-	2. Supply driver
43	nc				
44	UIH1	analogous	E	-	Measuring input low-side shunt Bank1
45	UIL1	analogous	E	-	Measuring input low-side shunt Bank1
46	UIMV1	analogous	A	-	Measuring output low-side Bank1
47	nc				
48	ISOLL_N	analogous	E	-	Nominal recharging current level
49	ISOLL_H	analogous	E	-	Nominal holding current level
50	nc				
51	nc				
52	ISOLL_A	analogous	E	-	Nominal start current level

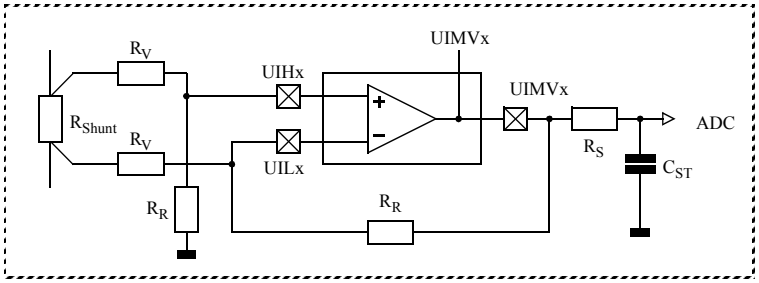
Number	Name	Level	Input/ Output	Int. current source	Function
53	IHYS	analogous	E	-	Hysteresis current level
54	IMAX_LS	analogous	E	-	Short-circuit current low-side
55	IMAX_HS	analogous	E	-	Short-circuit current high-side
56	UIMV2	analogous	E	-	Measuring output low-side Bank2
57	UIL2	analogous	E	-	Measuring input low-side shunt Bank2
58	UIH2	analogous	A	-	Measuring input low-side shunt Bank2
59	AGND				Supply analogous
60	AVCC				Supply analogous
61	UC_BOOS	analogous	E	-	Nominal voltage level discharge booster- C
62	UC_RCHG	analogous	E	-	Nominal voltage level recharge booster- C
63	UBOOS1	analogous	E	-	Actual voltage level booster C1
64	UBOOS2	analogous	E	-	Actual voltage level booster C2

6. Electrical limit values

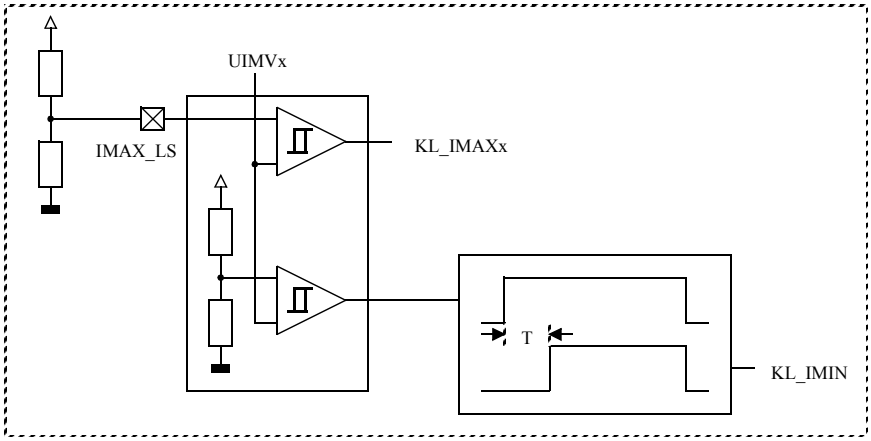
	Parameter or Connection	Conditions	Symbol	Numeric value min	typ	max	Unit
6.1	Supply voltage	no destruction static dynamic (T_i = 1 ms, T = 1 s)	AVCC, VDD	3,6	5	6,0 6,5	V V
6.2	Voltage offset	Supply $\Delta S = \lvert U_{AVCC} - U_{VDD} \rvert$ Ground $\Delta B = \lvert U_{AGND} - U_{GND} \rvert$	ΔS ΔB			0,1 0,1	V V
6.3	Junction temperature		T_J			140	°C
6.4	Ambient temperature	Chip on ceramic Plastic housing	T_U T_U	 -40		125 110	°C °C
6.5	Storage temperature	as chip Plastic housing	T_U T_U	-40 -40		175 125	°C °C
6.6	Input voltage	UBAT/UHSx (T_i = 400 ms, T = 5 s) UIHx/UILx (R_V= 5,62 kΩ) ISOLL_A, ISOLL_H, ISOLL_N, IHYS, UBOOSx, UC_BOOS, UC_RCHG IMAS_HS, IMAX_LS ONx, MODEx, RCHGx, OFFx, YSELxy, RES, BNK, T, DE, SY, DA	U_{UBAT} U_{UHSx} U_{UIHx} U_{UILx} U_{XXX}	-1,5 -0,3 -0,3		60 1,5 U_{AVCC} +0,3	V V V
6.7	Clamp current	UIHx/UILx (R_V= 5,62 kΩ) at overvoltage at undervoltage	 I_{UIHx} I_{UILx}	 -360		5	 mA µA

7. Electrical parameters

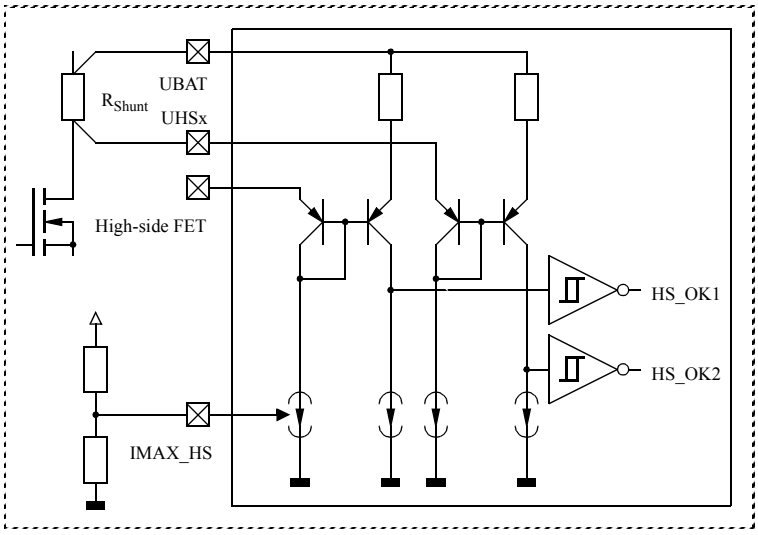
	Parameter or Connection	Conditions	Symbol	Numeric value min	typ	max	Unit
7.1	General information						
7.1.1	Power supply	continuous					
		Range 1: Low-side power stage locked internally	U_{AVCC} U_{VDD}	0		3,3	V
		Range 2: Low-side power stages switched off by external reset (RES), logic fully functional	U_{AVCC} U_{VDD}	3,3		4,5	V
		Range 3: Full function (RES=H)	U_{AVCC} U_{VDD}	4,5		5,5	V
		Range 4: Extended parameters permissible, no information loss	U_{AVCC} U_{VDD}	5,5		6,0	V
7.1.2	Power-On threshold	Transition range 1 -> range 2	U_{AVCC} U_{VDD}	3,3		4,2	V
7.1.3	Current consumption	U_{AVCC} , U_{VDD} = 5V; typically wired					
		static	I_{AVCC} I_{VDD}		12 0	20 15	mA mA
		dynamic	I_{VDD}		100		mA
7.1.4	Digital inputs	(Schmitt trigger input) ONx, MODEx, RCHG, T, DE					
		Buffer input RES, BNK, OFFx, YSELxy, SY					
		Logic level:					
		LOW Schmitt trigger input	U_{xxx}			0,2	U_{VDD}
		LOW buffer input	U_{xxx}			0,3	U_{VDD}
		HIGH Schmitt trigger input	U_{xxx}	0,8			U_{VDD}
		HIGH buffer input	U_{xxx}	0,7			U_{VDD}
		Input capacitance	C_{xxx}		15		pF
		Input current Pull-up current source:					
		MODEx, YSELxy, T, SY	I_{xxx}	-50	-25	-10	µA
		DE	I_{DE}	-250	-125	-50	µA
		Pull-down current source: RES, OFFx, ONx, RCHGx, BNK	I_{xxx}	10	25	50	µA

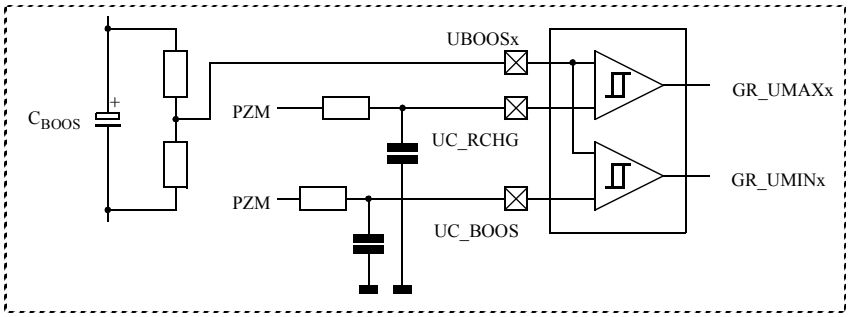
Parameter or Connection		Conditions	Symbol	Numeric value min	typ	max	Unit
7.2	Differential amplifier double	Bank1: UIH1, UIL1, UIMV1 Bank2: UIH2, UIL2, UIMV2 Internal: UIMVx					
7.2.1	Block diagram						
7.2.2	Ext. circuits	Shunt Series resistors Feedback resistors Low pass resistor Low pass capacitance	R_{Shunt} R_V R_R R_S C_{ST}		0,01 5,62 51,1 250 1		Ω kΩ kΩ Ω nF
7.2.3	Differential inputs	UIHx, UILx (Note: Avoid crosstalk by layout capacitances)					
	Clamping	at undervoltage at the shunt - 2 V ≤ U_{Shunt} ≤ -0,1 V Clamp voltage Clamp current	U_{UIxx} I_{UIxx}	-1 -0,36		-0,1 0	V mA
		at overvoltage at the shunt 0,7 V ≤ U_{Shunt} ≤ 28 V Clamp voltage Clamp current	U_{UIxx} I_{UIxx}	0,7 0		3 5	V mA
	Input voltage	Specified range (if UIH leaves the specified range, e.g. clamping in case of short-circuit, the output state at UIMV is retained)	U_{UIxx}	-0,1		0,7	V
	Offset voltage	$U_{OFF} = U_{UIHx} - U_{UILx}$ HT RT TT	U_{OFF} U_{OFF} U_{OFF}	-0,8 -1,2 -1,4		+0,8 +1,2 +1,4	mV mV mV
	Offset drift	$U_{OFFD} = dU_{OFF} / dT$ - 0.1 V ≤ U_{UIxx} ≤ 0.7 V	U_{OFFD}	-10		+10	µV/K
	Input current		I_{UIxx}	-2,5		0	µA
	Offset current	$I_{OFF} = I_{UIHx} - I_{UILx}$	I_{OFF}	-0,2		+0,2	µA

Parameter or Connection		Conditions	Symbol	Numeric value min	Numeric value typ	Numeric value max	Unit
7.2.4	Amplifier output	UIMVx					
	Output voltage	Specified range	U_{UIMV}	0,2		U_{AVCC} - 1 V	V
	Output current	Specified range (for specified offset)	I_{UIMV}	-100		100	µA
	Output impedance		R_{UIMV}		0,5		kΩ
	Rise/fall speed	Load: C = 1 nF (EMC) 10 ... 90 % voltage deviation	dU/dt		2,5		V/µs
	Transient time when connecting the sample capacitance	Typical wiring Sample capacitance 70 pF Transient to final value +/- 4,5 mV	t_{SW}			1,95	µs
	Gain	$V = U_{UIMV} / (U_{UIH} - U_{UIL})$	V		9,09		
	Transit frequency		f_T		2		MHz
	Common mode rejection ratio	DC-value	CMRR	60			dB
	Operating voltage suppression	DC-value f = 50 kHz $D_D = dU_{AVCC}/dU_{UIMVx}$	D_D		40		dB

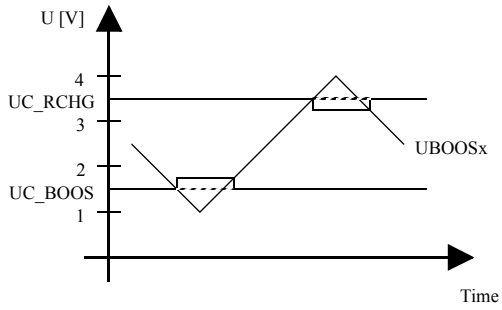
Parameter or Connection	Conditions	Sym-bol	Numeric value min	typ	max	Unit
7.3 Monitoring LS current level Double	Common IMAX_LS Internal: UIMVx Outputs (internal): KL_IMAXx, KL_IMINx					
7.3.1 Block diagram						
7.3.2 Ext. wiring	Preset maximum current by voltage divider at IMAX_LS					
7.3.3 Maximum current preset	IMAX_LS					
Input voltage	Specified range	U_{IMA_LS}	1,8		0,94 x U_{AVCC} -1	V
Input current	1.8 V ≤ U_{IMAX_LS} ≤ 0.94 x U_{AVCC} - 1 V	I_{IMAX_LS}	-5		+5	µA
Hysteresis voltage	Active on UIMV for $U_{UIMV} > U_{IMAX\_LS}$	U_{HYS}		30		mV
Internal limiting	lower (a diode voltage, U_D) upper (0.94 x U_{AVCC} - U_D)	U_{IMA_LS} U_{IMA_LS}		0,7 4,0		V V
Clamp current	- 0.3 V ≤ U_{IMAX_LS} ≤ 1.8 V 0.94 x U_{AVCC} - 1 V ≤ U_{IMAX_LS} ≤ U_{AVCC}	I_{IMAX_LS} I_{IMAX_LS}	-350	0	0	µA µA
7.3.4 Minimum current specification	internal					
Threshold		U_{IMIN}	0,2	0,27	0,32	V
Hysteresis voltage	Active on UIMV for $U_{UIMV} > U_{IMIN}$	U_{HYS}		30		mV
Signal delay	for state $U_{UIMV} < U_{IMIN}$ for state $U_{UIMV} > U_{IMIN}$	T T	7	10	13 200	µs ns

Parameter or Connection	Conditions	Sym-bol	Numeric value min	typ	max	Unit

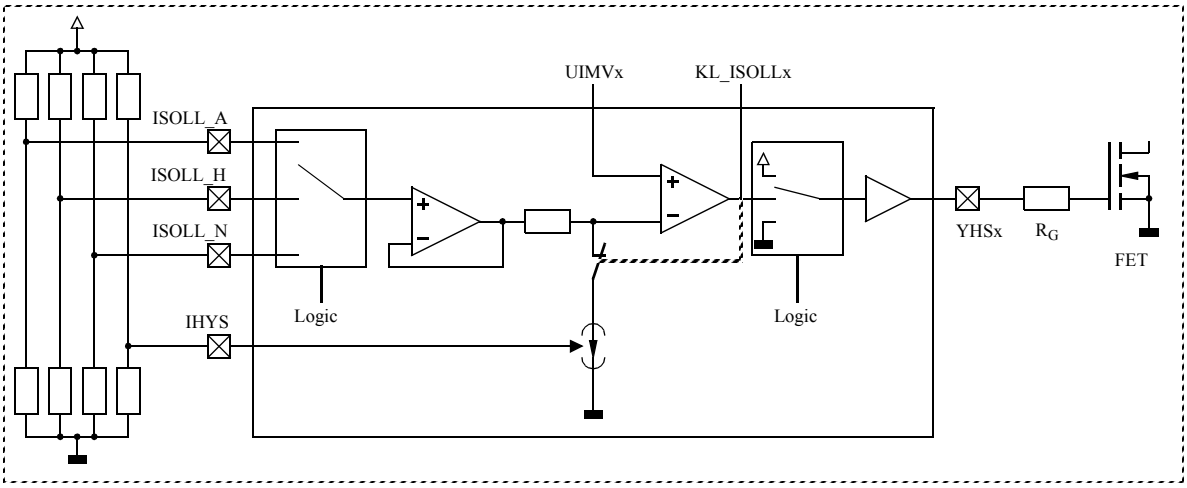
7.4	Monitoring HS current level Double	Common UBAT, IMAX_HS Bank1: UHS1 Bank2: UHS2 Output (internal): HS_OKx					
7.4.1	Block diagram						
7.4.2	Ext. wiring	Shunt Resistance divider (according to spec.)	R_{Shunt}		0,01		Ω
7.4.3	Measuring inputs	UBAT, UHSx					
	Input voltage	Tolerance range 1	U_{UBAT} U_{UHSx}	5,2		36	V
		Tolerance range 2	U_{UBAT} U_{UHSx}	36		60	V
	Difference input voltage	$U_D = U_{UBAT} - U_{UHSx}$ Permissible range	U_D	0,0		2,0	V
	Error	Error related to $U_D = U_{UBAT} - U_{UHSx}$ Tolerance range 1 Tolerance range 2	 F F		5	10 15	% %
	Operating current	$I_{UBAT/UHSx} = U_{IMAX\_HS}$ / 45 kΩ (typ.)					

Parameter or Connection		Conditions	Symbol	Numeric value min	typ	max	Unit
7.4.4	Switch off threshold High side protection	IMAX_HS					
	Input voltage		U_{IMX_HS}	1,5		U_{AVCC} -0,5	V
	Input current		I_{IMAX_LS}	-5		+5	µA
	Standardization of the switch off threshold	$N = U_{IMAX\_HS} / (U_{UBAT} - U_{UHSx})$	N	8.0	9	10	
7.5	Monitoring Voltage Booster capacitance Double	Common UC_RCHG, UC_BOOS Bank1: UBOOS1 Bank2: UBOOS2 Outputs (internal): GR_UMAXx, GR_UMINx					
7.5.1	Block diagram						
7.5.2	Ext. wiring	Voltage divider at the booster capacitance Filter element at the reference inputs for PZM signals Poss. Interference suppression capacitance at UBOOSx because disturbance signals are processed immediately by the fast CMOS comparator					
7.5.3	Actual inputs	UBOOSx					
	Input voltage	Permissible range	U_{UBOOS}	0		U_{AVCC}	V
	Input current		I_{UBOOS}	-0,2	0	+0,2	µA
7.5.4	Nominal inputs	UC_BOOS, UC_RCHG					
	Input voltage	Specified range UC_BOOS (discharge level)	U_{UC_BO}	0.0		U_{AVCC} -2.5	V
		UC_RCHG (charge level)	U_{UC_RC}	2,5		U_{AVCC}	V
	Input current	I_{UC_BOOS} or I_{UC_BOOS}	I_{UC_xxxx}	-0.2	0	+0,2	µA
7.5.5	Offset voltage	$U_{OFF} = U_{UBOOS} - U_{UC\_RCHG}$ $U_{OFF} = U_{UBOOS} - U_{UC\_BOOS}$	U_{OFF}	-20		+20	mV

Parameter or Connection		Conditions	Sym-bol	Numeric value min	typ	max	Unit
7.5.6	Hysteresis voltage	Active on references UC_BOOS, UC_RCHG	U_{HYS}	25	50	75	mV



7.6	Current regulation Double	Common ISOLL_A, ISOLL_H, ISOLL_N, IHYS Internal: UIMV1, UIMV2 Bank1: YHS1 Bank2: YHS2 Output (internal): KL_ISOLLx
7.6.1	Block diagram	



7.6.2	Ext. wiring	Nominal preset by voltage divider at ISOLL_x Voltage divider at IHYS					

Parameter or Connection	Conditions	Symbol	Numeric value min	typ	max	Unit
7.6.3 Nominal inputs						
7.6.3.1 Normal nominal range	ISOLL_A (start current level) ISOLL_H (holding current level) ISOLL_N (recharging current level)					
Input voltage	Specified range	U_{ISOLL}	0,6		U_{AVCC} -1,1	V
Input current	$0,6\ V \le U_{ISOLL\_N} \le U_{AVCC}$ -1,1V	I_{ISOLL_N}	-2		+0,5	µA
	$0,6\ V \le U_{ISOLL\_A} \le 1V$	I_{ISOLL_A}	-5		+0.5	µA
	$0,6\ V \le U_{ISOLL\_H} \le 1V$	I_{ISOLL_H}	-5		+0.5	µA
	$1.0\ V \le U_{ISOLL\_A} \le U_{AVCC}$ -1,1V	I_{ISOLL_A}	-2		+0.5	µA
	$1.0\ V \le U_{ISOLL\_H} \le U_{AVCC}$ -1,1V	I_{ISOLL_H}	-2		+0.5	µA
Level selection	RCHG=0, MODE=0: ISOLL_H RCHG=0, MODE=1: ISOLL_A RCHG=1, MODE=X: ISOLL_N direct access by RCHG and MODE					
Offset voltage	$U_{OFF} = U_{UIMV} - U_{ISOLL}$ (hysteresis not active)	U_{OFF}	-20		+20	mV
Switching speed	Nominal voltage on the current comparator (see also note chapter 3 Functional Description)	dU/dt	0,75			V/µs
7.6.3.2 ISOLL_N range expansion	Range expansion for UISOLL_N, $500mV < U_{ISOLL\_N} < 600mV$:					
Offset voltage	Range 1: $540mV < U_{ISOLL\_N} < 600mV$, $U_{OFFmax}=(1/3) \times (600mV-U_{ISOLL\_N}) + 20mV$ ($U_{OFFmax}= f(U_{ISOLL\_N})$, (applies for U_{ISOLL_N} in range 1)	U_{OFF}	-20		40	mV
	Range 2: $500mV < UI_{ISOLL\_N} < 540mV$, $U_{OFFmax}=(3/8) \times (540mV-U_{ISOLL\_N}) + 40mV$ ($U_{OFFmax}= f(U_{ISOLL\_N})$, (applies for U_{ISOLL_N} in range 2)	U_{OFF}	-20		55	mV
Input current	Total range 1/2, $500mV < U_{ISOLL\_N} < 600mV$: $I_{ISOLL\_Nmin}=$ $- (1\mu A/20mV \times (600mV-U_{ISOLL\_N}) -2\mu A$ ($I_{ISOLL\_N}= f(U_{ISOLL\_N})$, (applies for U_{ISOLL_N} in range 1/2)	I_{ISOLL}	-7		2	µA

Parameter or Connection		Conditions	Sym-bol	Numeric value min	typ	max	Unit
7.6.4	Hysteresis level	IHYS					
	Input voltage	Specified range Note: It must be ensured that it applies U_{ISOLL_X} - HYS_{INT} > 0,5 V	U_{IHYS}	0,2		U_{AVCC} -1,5	V
	Input current	0,2 V ≤ U_{IHYS} ≤ U_{AVCC} -1,5 V	I_{IHYS}	-5		+5	µA
	Standardization of the hysteresis voltage	N = U_{IHYS} / HYS_{INT} (with HYS_{INT} as hysteresis voltage related to U_{ISOLL_X})	N		6,19		
	Tolerance	F = ΔHYS_{INT} / HYS_{INT} for U_{IHYS} > 1 V for U_{IHYS} ≤ 1 V	F ΔHYS_{IN}		5 50	12 100	% mV
7.6.5	Power stage output	YHS1, YHS2 Measuring wiring Load capacitance C = 0,5 nF Series resistor R = 50 Ω Times measured at output YHSx					
	Switching point	YHS = HIGH for U_{UIMV} > U_{ISOLL_X} YHS = LOW for U_{UIMV} > U_{ISOLL_X} - HYS_{INT}					
	Output voltage	State HIGH: 0 < I_{YHS} ≤ - 0,5 mA	U_{YHS}	U_{VDD} -0,2		U_{VDD}	V
		0 < I_{YHS} ≤ - 4,0 mA	U_{YHS}	U_{VDD} -1,1		U_{VDD}	V
		State LOW: 0 < I_{YHS} ≤ 0,5 mA	U_{YHS}	0		0,3	V
		0 < I_{YHS} ≤ 4,0 mA	U_{YHS}	0		0,7	V
	Switching frequency		f_S	50			kHz
	Turn-on time	Rising edge from U_{YHSmin} to U_{YHS} = U_{VDD} - 1,0 V from U_{YHSmin} to U_{YHS} = U_{YHSmax}	t_{rise1} t_{rise2}			300 900	ns ns
	Turn-on delay		t_{ON}			250	ns
	Turn-off time	Falling edge from U_{YHSmax} to U_{YHS} = 1,0 V from U_{YHSmax} to U_{YHS} = U_{YHSmin}	t_{fall1} t_{fall2}			250 900	ns ns
	Turn-off delay		t_{down}			250	ns

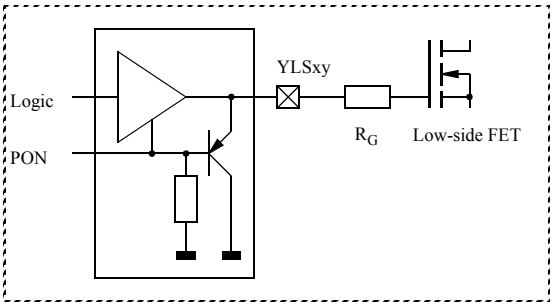
	Parameter or Connection	Conditions	Sym-bol	Numeric value min	typ	max	Unit
7.7	Power stages Booster FET: Double	YBOOSx					
7.7.1	Power stage output	YBOOS1, YBOOS2 Measuring wiring Load capacitance C = 0,5 nF Series resistor R = 50 Ω Times measured at output YBOOSx					
	Output voltage	State HIGH:					
		$0 < I_{YBOOS} \leq$ - 0,5 mA	U_{YBOOS}	U_{VDD} -0,2		U_{VDD}	V
		$0 < I_{YBOOS} \leq$ - 4,0 mA	U_{YBOOS}	U_{VDD} -1,1		U_{VDD}	V
		State LOW:					
		$0 < I_{YBOOS} \leq$ 0,5 mA	U_{YBOOS}	0		0,2	V
		$0 < I_{YBOOS} \leq$ 4,0 mA	U_{YBOOS}	0		0,7	V
	Switching frequency		f_S	50			kHz
	Turn-on time	Rising edge					
		from $U_{YBOOSmin}$ to $U_{YBOOS} = U_{VDD}$ - 1,0 V	t_{rise1}			300	ns
		from $U_{YBOOSmin}$ to $U_{YBOOS} = U_{YBOOSmax}$	t_{rise2}			900	ns
	Turn-on delay		t_{ON}			250	ns
	Turn-off time	Falling edge					
		from $U_{YBOOSmax}$ to U_{YBOOS} = 1,0 V	t_{fall1}			250	ns
		from $U_{YBOOSmax}$ to $U_{YBOOS} = U_{YBOOSmin}$	t_{fall2}			900	ns
	Turn-off delay		t_{down}			250	ns

Parameter or Connection	Conditions	Sym-bol	Numeric value min	typ	max	Unit

7.8 Power stage
Low-side FET
Eightfold

Inputs YSELxy
Outputs: YLSxy

7.8.1 Block diagram



7.8.2 Power stage selection

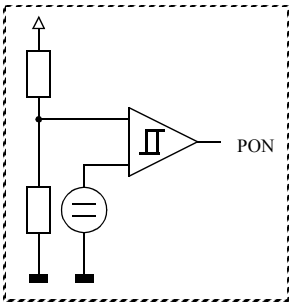
YSELxy
Selection only possible if component is inactive (no injection or recharging)

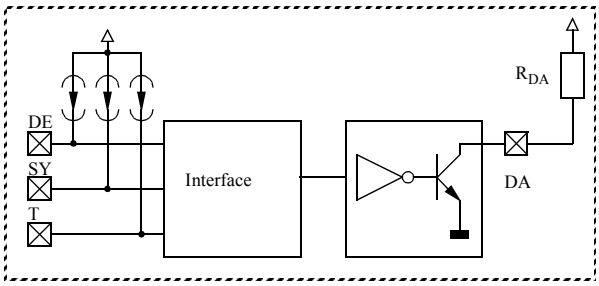
YSELx1	YSELx0	Power stage bank x
0	0	YLSx1
0	1	YLSx2
1	0	YLSx3
1	1	YLSx4

7.8.3 Power stage output

YLSxy
Measuring wiring
Load capacitance C = 15 nF
Series resistor R = 50 Ω
Times measured at output YLSxy

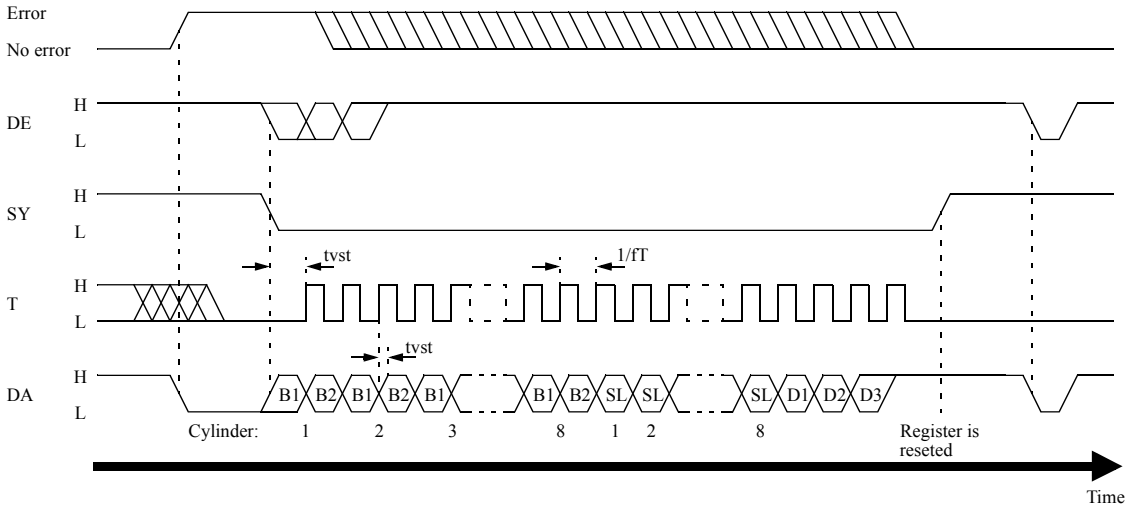
Output voltage static	State HIGH: $0 < I_{YLS} \le -0,5$ mA	U_{YLS}	U_{VDD} -0,4		U_{VDD}	V
	$0 < I_{YLS} \le -4,0$ mA	U_{YLS}	U_{VDD} -1,1		U_{VDD}	V
	State LOW: $0 < I_{YLS} \le 0,5$ mA	U_{YLS}	0		0,2	V
	$0 < I_{YLS} \le 4,0$ mA	U_{YLS}	0		0,7	V
Switching frequency		f_S	50			kHz
Turn-on time	from U_{YLSmin} to $U_{YLS} = U_{VDD} - 1,0$ V	t_{rise1}		1	2	µs
	from U_{YLSmin} to $U_{YLS} = U_{YLSmax}$	t_{rise2}		2	3	µs
Turn-on delay		t_{ON}			500	ns
Turn-off time	from U_{YLSmax} to $U_{YLS} = 1,0$ V	t_{fall1}		200	400	ns
	from U_{YLSmax} to $U_{YLS} = U_{YLSmin}$	t_{fall2}		0,5	1	µs
Turn-off delay		t_{down}			500	ns

Parameter or Connection		Conditions	Sym-bol	Numeric value min	typ	max	Unit
7.8.4	Power-On switch off	Ensures that the outputs are switched off independently of the external system at undervoltage. From U_{AVCC} = 3.8V the external reset signal (RES) must be applied stably so that the then active power stage can ensure switching-off. (see also 7.1.1 and 7.1.2) 					
	Threshold	internal	U_{AVCC}	3,3		4,2	V

Parameter or Connection		Conditions	Symbol	Numeric value min	typ	max	Unit
7.9	Diagnosis	Inputs DE, SY, T Output: DA					
7.9.1	Block diagram						
7.9.2	Ext. wiring	Pull-up resistor DA					
7.9.3	Inputs	DE, T, SY					
	Data input DE	Serial data input of the shift register for cascading					
	Clock T	Shift clock for reading out diagnosis information, active on the rising edge					
	Synchronization SY	Transfer signal for the shift register, active on the falling edge; Rising edge resets the registers, state is then: error-free					
		Clock frequency	f_T			1	MHz
		Data validity after positive clock edge Data validity after SY = Low	tv_{DG}			0,5	µs
		Wait time after SY = Low up to first positive clock edge	tv_{ST}	1			µs
		Low time at SY to reset error memory	tv_{SYL}	1			µs
7.9.4	Output	DA					
	Output voltage	State LOW $0 < I_{DA} \leq 1{,}6$ mA	U_{DA}	0		0,4	V
	Output capacitance		C_{DA}		15		pF
	Input voltage	State HIGH:	U_{DA}			U_{AVCC} +0,3	V
	Input current	State HIGH:	U_{DA}	- 10	0	+ 10	µA

Parameter or Connection	Conditions	Sym-bol	Numeric value min	typ	max	Unit

7.9.5 Transmission protocol



7.9.6 Shift sequence and coding

DE	DE	Cylinder 8	.....	Cylinder 1	Cylinder 8	.....	Cylinder 1
Bit n	Bit 1	Bit SL	Bit SL	Bit SL	Bit 2 | Bit 1	Bit 2 | Bit 1	Bit 2 | Bit 1

Coding fast decay

Error state	Bit SL
No error	H
fast decay error	L

Coding
Short-circuit/drop in load

Error state	Bit 2 | Bit 1
No error	H | H
Drop in load	H | L
Short-circuit to U_{bat}	L | H
Short-circuit to GND	L | L