AS5510

Linear Hall Sensor with I²C Output

Data Sheet

1 General Description

The AS5510 is a linear Hall sensor with 10 bit resolution and I²C interface. It can measure absolute position of lateral movement of a simple 2-pole magnet.
Depending on the magnet size, a lateral stroke of 0.5~2mm can be measured with air gaps around 1.0mm.
To conserve power, the AS5510 may be switched to a power down state when it is not used.

It is available in a WLCSP package and qualified for an ambient temperature range from -30°C to +85°C.

2 Key Features

- 10bit resolution
- I²C Interface
- Power down mode
- Programmable sensitivity

3 Applications

- Position sensing
- Servo drive feedback
- Camera lens control
- Closed loop position control

Figure 1. Linear Position Sensor with AS5510 + Magnet

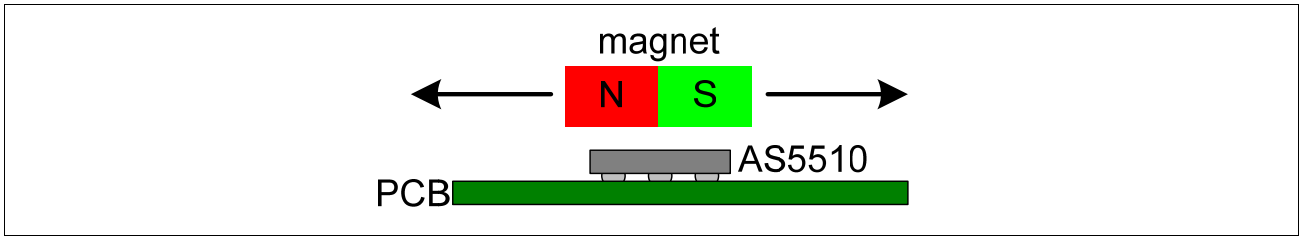
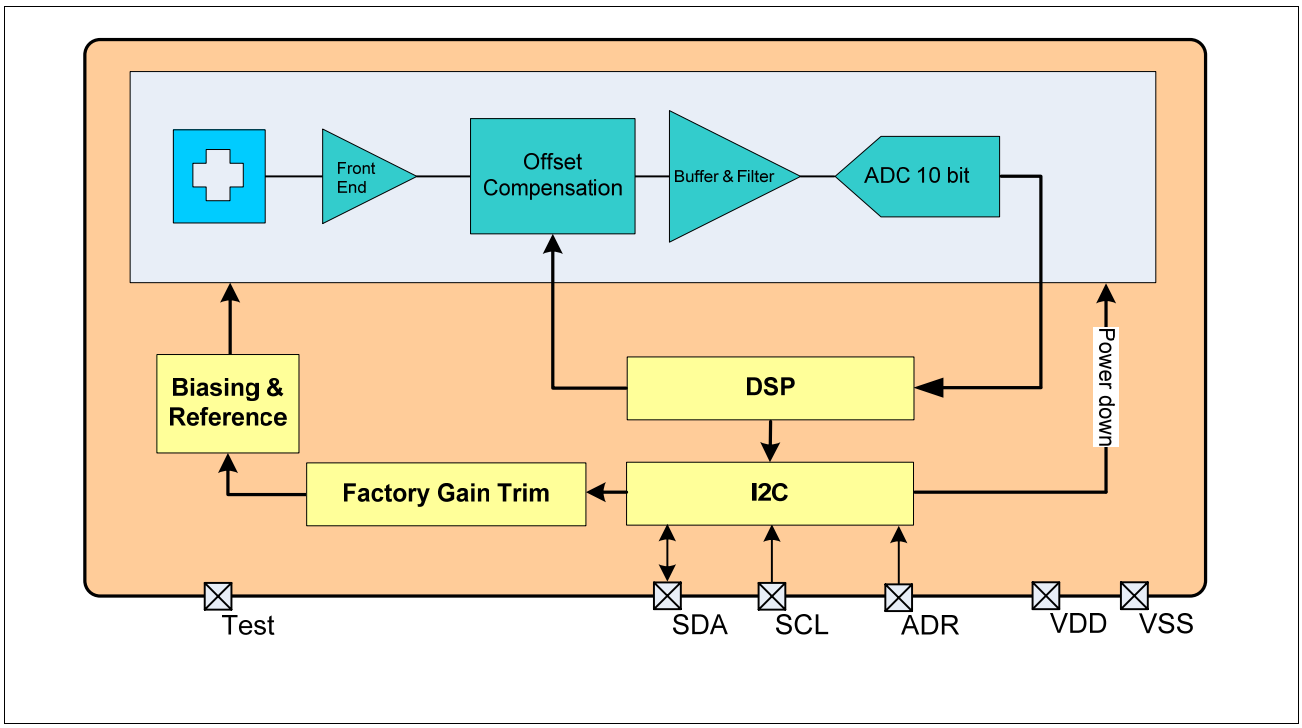
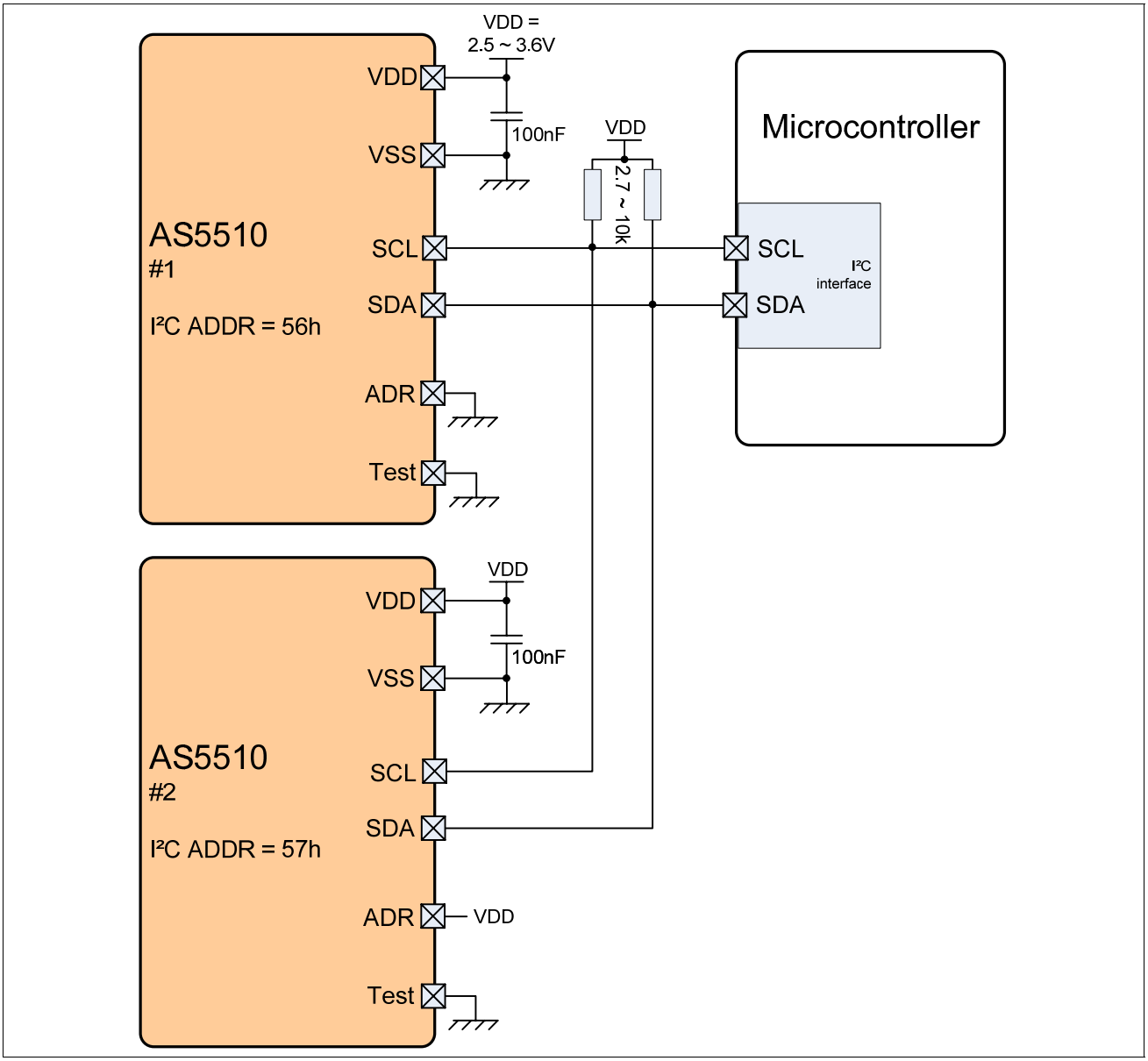


Figure 2. Block Diagram of AS5510



4 Typical Application

Figure 3. Typical Application



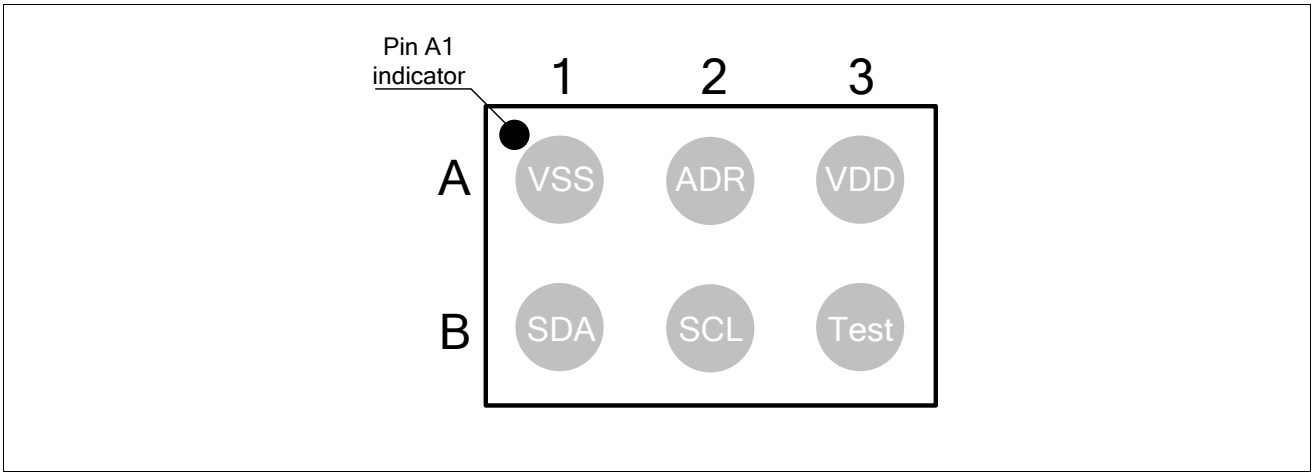
5 Table of Contents

6 Pinout

6.1 Pin Assignments

The AS5510 is available in a 6-pin Chip Scale Package with a ball pitch of 400µm.

Figure 4. Pin Configuration of AS5510 (Top View)



6.2 Pin Description

Table 1. Pin Description AS5510

Pin	Symbol	Type	Description
A1	VSS	S	Negative supply pin, analog and digital ground.
A2	ADR	DI	I²C address selection pin Connect to either VSS (56h) or VDD (57h)
A3	VDD	S	Positive supply pin. A capacitor of 100nF should be connected to this pin and VSS
B1	SDA	DI/DO_OD	I²C data I/O, 20mA driving capability
B2	SCL	DI	I²C clock
B3	Test	DIO	Test pin. Must be connected to VSS during operation

DO_OD digital output open drain
DI digital input
DIO digital input/output
S supply pin

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Comments
DC supply voltage at pin VDD	-0.3	5	V	
Input pin voltage	-0.3	VDD +0.3	V	
Input current (latchup immunity)	-100	100	mA	Norm: JEDEC 78
Electrostatic discharge		± 1	kV	Norm: MIL 883 E method 3015
Storage temperature	-55	125	°C	
Body temperature (Lead-free package)	TBody	260	°C	t=20 to 40s, Norm: IPC/JEDEC J-Std-020C Lead finish 100% Sn “matte tin”
Humidity non-condensing	5	85	%	

7.2 Operating Conditions

Table 3. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage at pin VDD	VDD	2.5	3	3.6	V	
Supply current	Isupp		3.5		mA	@ 25 °C ambient temperature
Power down current	Ipd		25		µA	@ 25 °C ambient temperature
Ambient temperature	Tamb	-30		85	°C	

7.3 DC Characteristics for Digital Inputs and Outputs

7.3.1 CMOS Input: ADR

Table 4. Electrical Characteristics ADR Input

Operating conditions: T_{amb} = -30 to +85°C, VDD = 2.5 to 3.6V (3V operation) unless otherwise noted.

Parameter	Symbol	Min	Max	Unit	Note
High level input voltage	VIH	0.7 * VDD	VDD	V	
Low level input voltage	VIL	0	0.3 * VDD	V	
Input leakage current	ILEAK IiL	-1	1	µA	

7.3.2 CMOS I²C: SDA, SCL

Table 5. Electrical Characteristics I^2C

Operating conditions: T_{amb} = -30 to +85°C, VDD = 2.5 to 3.6V (3V operation) unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	LOW-Level Input Voltage		-0.5		0.3 * VDD	V
V_{IH}	HIGH-Level Input Voltage		0.7 * VDD		VDD +0.5V	V
V_{hys}	Hysteresis of Schmitt Trigger Inputs	V_{DD} > 2.5V	0.05 * VDD			V
V_{OL}	LOW-Level Output Voltage (open-drain or open-collector) at 3mA Sink Current	V_{DD} > 2.5V			0.4V	V
I_{OL}	LOW-Level Output Current	V_{OL} = 0.4V	20			mA
tof	Output Fall Time from VIHmax to VILmax				120 (1)	ns
t_{SP}	Pulse Width of Spikes that must be suppressed by the Input Filter				50 (2)	ns
I_i	Input Current at each I/O Pin		-10		+10 (3)	µA
C_B	Total Capacitive Load for each Bus Line				550	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL) (4)				10	pF

Notes:
(1) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used this has to be considered for bus timing
(2) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
(3) I/O pins of Fast-mode and Fast-mode plus devices must not obstruct the SDA and SCL lines if VDD is switched off.
(4) Special purpose devices such as multiplexers and switches may exceed this capacitance due to the fact that they connect multiple paths together.

7.4 Electrical and Magnetic Specifications

Table 6. Electrical and Magnetic Specifications

Operating conditions: T_{amb} = -30 to +85°C, VDD = 2.5 to 3.6V (3V operation) unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Resolution	RES		10		bit	
Magnetic Input range	Bin		+/- 50		mT	Default setting
			+/- 25		mT	Configurable via I²C or factory trimming option
			+/- 12.5		mT	Configurable via I²C or factory trimming option
			+/- 18.75		mT	Configurable via I²C or factory trimming option
Input related offset (1)	Offsetinp			0.45	mT	
Linearity error (2)				3	%	
Initial Power up time from cold start (3)	tPwrUp			1.5	ms	This time is needed for the first power-up of the device until the offset compensation is finished; Includes readout of the PPROM fuses

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power-on time (4)	tPwrOn		250		µs	Time after switching from power-down mode into active mode until the offset compensation is finished
		Fast mode (default setting)				
ADC sampling frequency	fS			50	kHz	After offset compensation finished
System propagation delay	tdelay			20	µs	After offset compensation finished
Input related noise (5)	Noiseinp			0.8	mTpp	Equivalent to 8 * rms
		Slow mode (I²C command option)				
ADC sampling frequency	fS			12.5	kHz	After offset compensation finished
System propagation delay	tdelay			50	µs	After offset compensation finished
Input related noise (5)	Noiseinp			0.5	mTpp	Equivalent to 8 * rms

Notes:

(1) $Offset_{inp}$ = 0.35mT residual offset + 0.1mT earth magnetic field

(2) Linearity error =

$$lin\_error = 1 - \left(\frac{adc\_out(\max B) - adc\_out(zeroB)}{2 * (adc\_out\left(\frac{\max B}{2}\right) - adc\_out(zeroB)} \right) * 100$$

(3) This time is needed for the first power-up of the device until the offset compensation is finished; Includes readout of the PPROM fuses ; It depends on the sensitivity setting

(4) Time after switching from power-down mode into active mode until the offset compensation is finished

(5) Input related Noise (NoiseInp) is the repeatability of the measurement

8 I²C Interface

The AS5510 includes an I²C slave according to the NXP specification UM10204.

- 7-bit slave address **101011x**, the last address bit x is set by the ADR pin (0 or 1)
- Random/Sequential Read
- Byte/Page Write
- Fast-mode plus with 20mA SDA drive strength
  Internal hold time of 120ns for SDA signal is included (Start/Stop detection)

Not implemented:

- 10-bit Slave Address
- Clock Stretching
- General Call Address
- General Call – Software Reset
- Read of Device ID

The communication from the AS5510 includes:

- reading the magnetic field strength in 10-bit data
- reading the status bits

Note: the I²C address of the chip is selected by hardware (pin ADR). Depending on the state of this pin, the I²C address is either

Pin ADR = LOW → I²C address = 1010110b (56h)

Pin ADR = HIGH → I²C address = 1010111b (57h)

8.1.1 I²C Interface Data

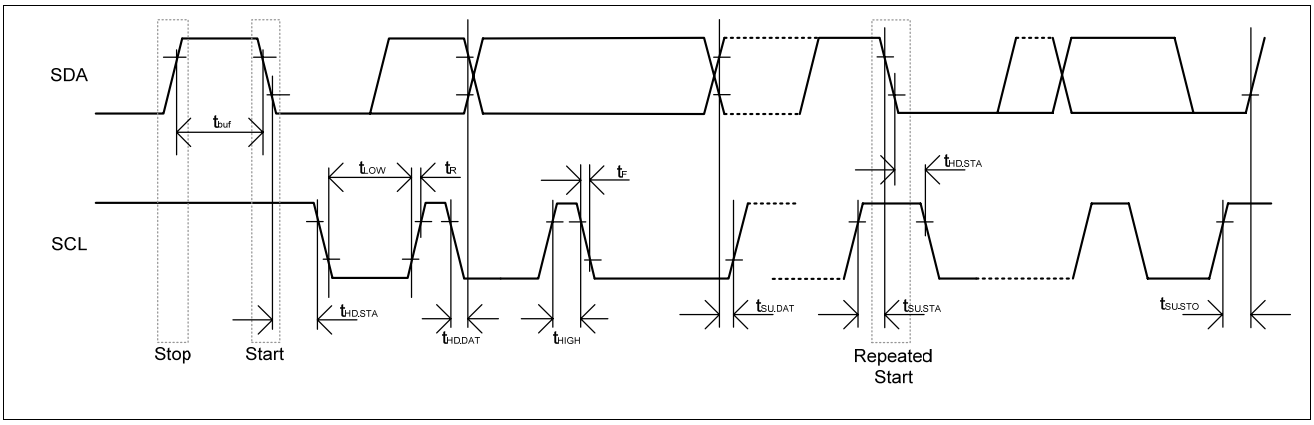
Table 7. I²C Timings

Operating conditions: T_{amb} = -30 to +85°C, VDD = 2.5 to 3.6V (3V operation) unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCLK}	SCL clock Frequency			1	MHz
t_{BUF}	Bus Free Time; time between STOP and START Condition	0.5			µs
$t_{HD.STA}$	Hold Time; (Repeated) START Condition (1)	0.26			µs
t_{LOW}	LOW Period of SCL Clock	0.5			µs
t_{HIGH}	HIGH Period of SCL Clock	0.26			µs
$t_{SU.STA}$	Setup Time for a Repeated START condition	0.26			µs
$t_{HD.DAT}$	Data Hold Time (2)			0.45	µs
$t_{SU.DAT}$	Data Setup Time (3)	50			ns
t_R	Rise Time of SDA and SCL Signals			120	ns
t_F	Fall time of SDA and SCL signals			120 (4)	ns
$t_{SU.STO}$	Setup Time for STOP Condition	0.26			µs

Notes:
(1) After this time the first clock is generated
(2) A device must internally provide a hold time of at least 120ns (Fast-mode Plus) for the SDA signal (referred to the V_{IHmin} of the SCL) to bridge the undefined region of the falling edge of SCL.
(3) A fast-mode device can be used in standard-mode system, but the requirement $t_{SU.DAT}$ = 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does strech the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{Rmax} + T_{SU.DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
(4) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used this has to be considered for bus timing.

Figure 5. I²C Timing Diagram



8.2 I²C Modes

The AS5510 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions must control the bus. The AS5510 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100 kHz maximum clock rate) a fast mode (400 kHz maximum clock rate) and fast mode plus (1MHz maximum clock rate) are defined. The AS5510 works in all three modes. Connections to the bus are made through the open-drain I/O lines SDA and the input SCL. Clock stretching is not included.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as start or stop signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy
Both data and clock lines remain HIGH.

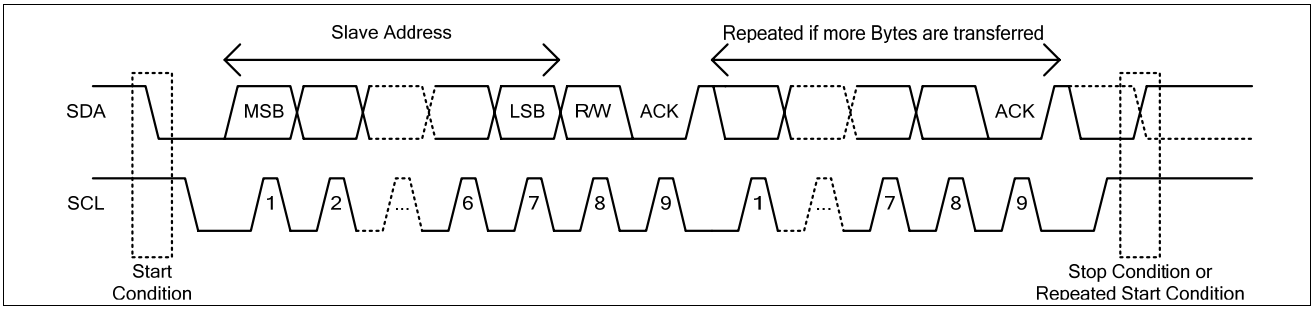
Start Data Transfer
A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer
A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid
The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge
Each receiving device, when addressed, is obliged to generate an acknowledge bit after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.
A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of READ access to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 6. Data Read (Write Pointer, Then Read) - Slave Receive and Transmit



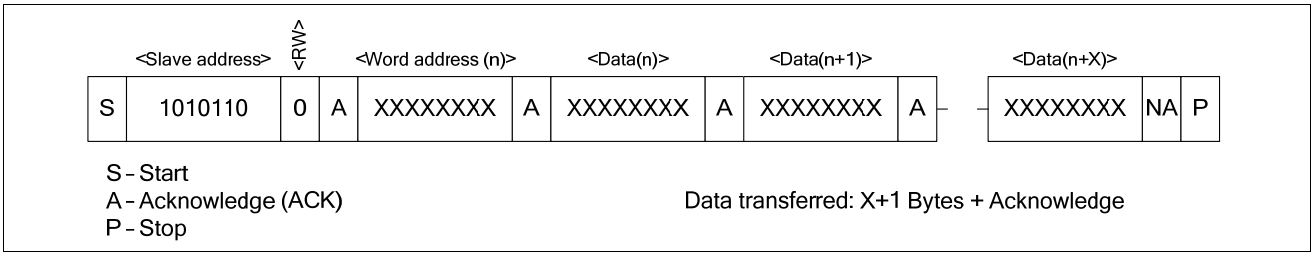
Depending upon the state of the R/W bit, two types of data transfer are possible:

- **Data transfer from a master transmitter to a slave receiver.**
  The first byte transmitted by the master is the slave address, followed by R/W = 0. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. If the slave does not understand the command or data it sends a “not acknowledge”. Data is transferred with the most significant bit (MSB) first.
- **Data transfer from a slave transmitter to a master receiver.**
  The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The AS5510 can operate in the following two modes:

- **Slave Receiver Mode (Write Mode):**
  Serial data and clock are received through SDA and SCL. Each byte is followed by an acknowledge bit (or by a not acknowledge depending on the address-pointer pointing to a valid position). START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see *Figure 7. Data Write - Slave Receiver Mode*). The slave address byte is the first byte received after the START condition. The slave address byte contains the 7-bit AS5510 address. The 7-bit slave address is followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on theSDA. After the AS5510 acknowledges the slave address + write bit, the master transmits a register address to the AS5510. This sets the address pointer on the AS5510. If the address is a valid readable address the AS5510 answers by sending an acknowledge. If the address-pointer points to an invalid position a “not acknowledge” is sent. The master may then transmit zero or more bytes of data. In case of the address pointer pointing to an invalid address the received data are not stored. The address pointer will increment after each byte transferred independent from the address being valid. If the address-pointer reaches a valid position again, the AS5510 answers with an acknowledge and stores the data. The master generates a STOP condition to terminate the data write.

Figure 7. Data Write - Slave Receiver Mode



- **Slave Transmitter Mode (Read Mode):**
  The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the AS5510 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (*Figure 8. Data Read (from Current Pointer Location) - Slave Transmitter Mode* and *Figure 9. Data Read (Write Pointer, Then Read) - Slave Receive and Transmit*). The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS5510 address. The 7-bit slave address is followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The AS5510 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The AS5510 must receive a “not acknowledge” to end a read.

Figure 8. Data Read (from Current Pointer Location) - Slave Transmitter Mode

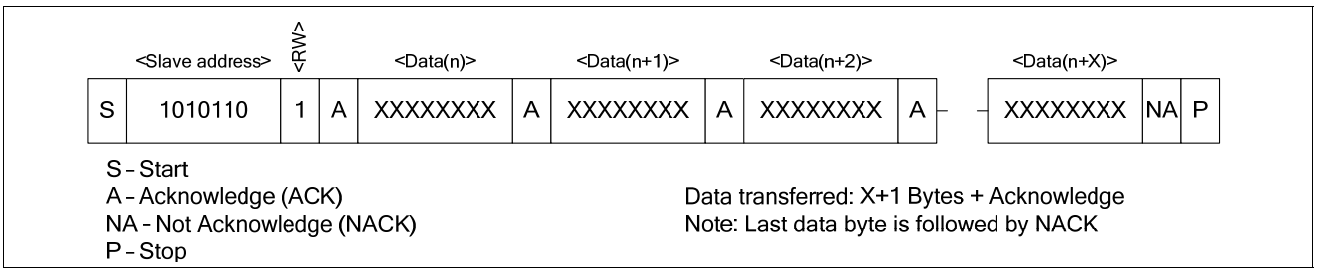
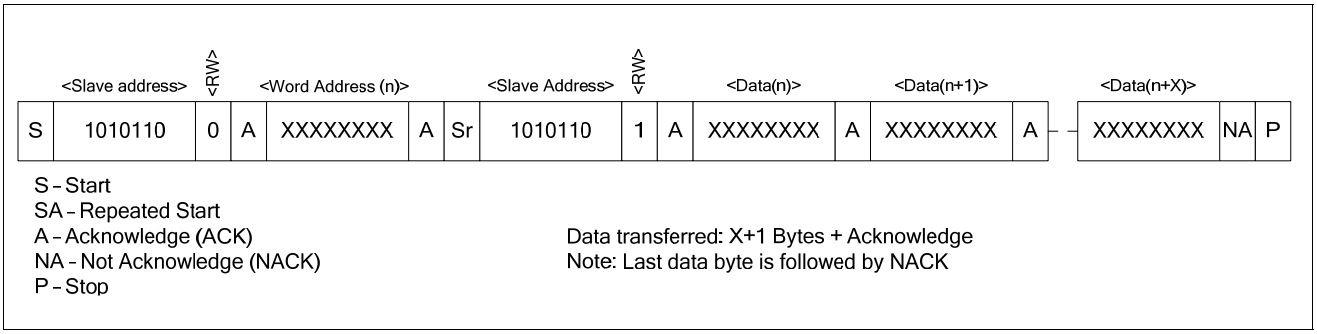


Figure 9. Data Read (Write Pointer, Then Read) - Slave Receive and Transmit



Automatic increment of address pointer:
The AS5510 slave automatically increments the address pointer after each byte transferred. The increase of the address pointer is independent from the address being valid or not.

Invalid Addresses:
If the user sets the address pointer to an invalid address, the address byte is not acknowledged. Nevertheless a read or write cycle is possible. The address pointer is increased after each byte.

Reading:

When reading from a wrong address, the AS5510 slave returns all zero. The address pointer is increased after each byte. Sequential read over the whole address range is possible including address overflow.

Write:
A write to a wrong address is not acknowledged by the AS5510 slave, although the address pointer is increased. When the address pointer points to a valid address again, a successful write accessed is acknowledged. Page write over the whole address range is possible including address overflow.

8.3 SDA, SCL Input Filters

Input filters for SDA and SCL inputs are included to suppress noise spikes of less than 50ns. Furthermore the SDA line is delayed by 120ns to provide an internal hold time for Start/Stop detection to bridge the undefined region of the falling edge of SCL. The delay needs to be smaller than $t_{HD.STA}$ 260ns. For Standard-mode and Fast-mode an internal hold time of 300ns is required, which is not covered by the AS5510 slave.

8.4 Register Map & Description

Table 8. Register Map

Register Address	bit								Access Type
	7	6	5	4	3	2	1	0	
00h	D7	D6	D5	D4	D3	D2	D1	D0	r
01h					OCF	Parity (even)	D9	D8	r
02h						fast (0) slow mode (1)	Polarity (0)	PD (0)	r/w
03h	Offs7	Offs6	Offs5	Offs4	Offs3	Offs2	Offs1	Offs0	r/w
04h							Offs9	Offs8	r/w
05h	reserved for factory testing								r/w
06h									
07h									
0Bh							Sens 1	Sens0	r/w

Table 9. Register Description

Register Address	Name	Description
00h, 01h	D9 to D0	10 Bit ADC output value that corresponds to the magnetic field input
01h	Parity	Even parity bit calculated from D9 to D0
01h	OCF	Offset compensation loop status 0 = Offset compensation loop in use 1 = Offset compensation loop has finished
02h	PD	Power down mode. 0 = Normal operation (Default) 1 = Power Down mode.
02h	Polarity	Output signal polarity 0 = Normal polarity (Default) 1 = Reversed polarity (reversed magnet)
02h	Fast / Slow mode	0 = Fast mode (Default) 1 = Slow mode. Enables averaging of the output values (reduced noise, better repeatability slower sampling frequency. See chapter *7.4*
03h, 04h	Offs9 to Offs0	10 Bit value of the offset compensation. This register is factory trimmed
05h, 06h, 07h	Test	these registers are reserved for factory testing
0Bh	Sensitivity	Sensitivity setting 0h = Input range +/- 50mT → Sensitivity = 97.66µT/LSB (Default) 1h = Input range +/- 25mT → Sensitivity = 48.83µT/LSB 2h = Input range +/- 12.5mT → Sensitivity = 24.41µT/LSB 3h = Input range +/- 18.75mT → Sensitivity = 36.62µT/LSB

9 Package Drawings and Markings

9.1 Chip Scale Package 1.46 x 1.1mm

Figure 10. Package Drawings and Marking

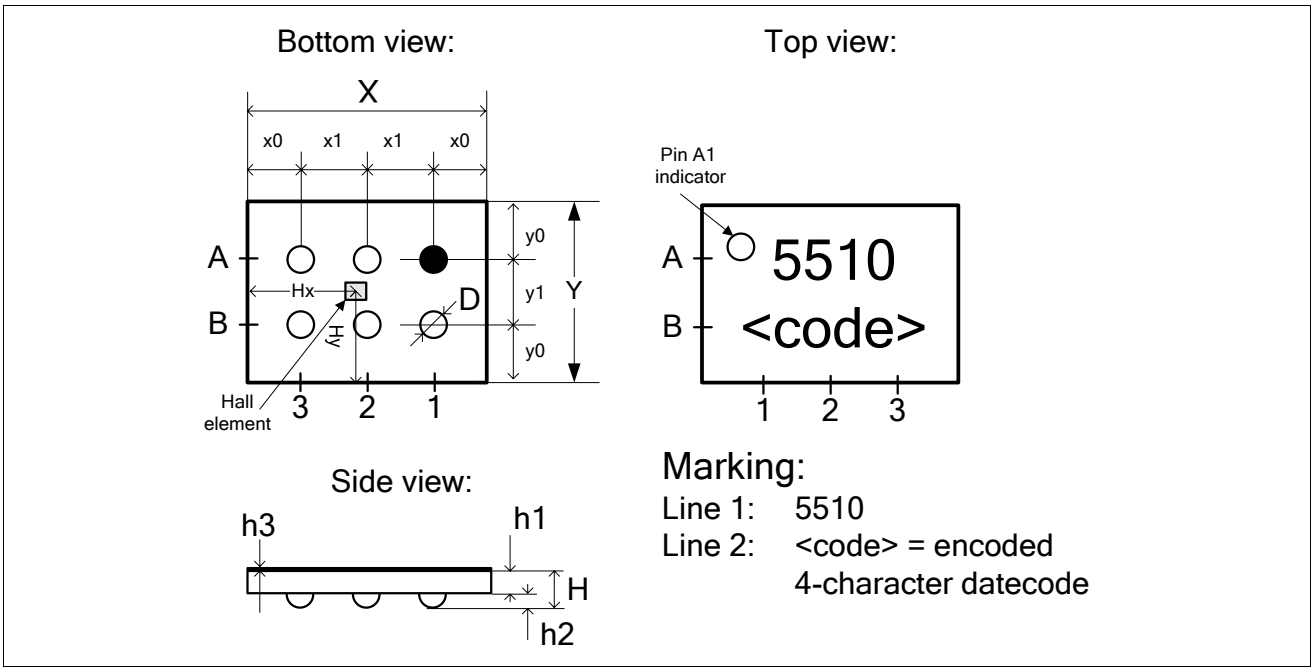


Table 10. Package Dimensions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Die length	X		1460		µm	From center of scribeline
Distance between chip border and bumps in x-direction	x0		330		µm	From center of scribeline
Pitch between bumps in x-direction	x1		400		µm	From center of scribeline
Die width	Y		1100		µm	From center of scribeline
Distance between chip border and bumps in y-direction	y0		350		µm	From center of scribeline
Pitch between bumps in y-direction	y1		400		µm	From center of scribeline
Location of Hall element in x-direction	Hx		650		µm	From center of scribeline
Location of Hall element in y-direction	Hy		550		µm	From center of scribeline
Overall thickness	H	570	600	630	µm	
Wafer thickness	h1	350	360	370	µm	
Backside Laminate	h3	35	40	45	µm	
Solder ball height	h2	180	200	220	µm	
Solder ball diameter	D	260	270	280	µm	

9.2 Ordering Information

Table 11. Ordering Information

Model	Description	Delivery Form	Package
AS5510 DWLT	Linear Hall Sensor	Tape & Reel	CSP 1.46 x 1.1mm

10 Revision History

Table 12. Revision History

Revision No.	Description	Change Date
0.1	Initial revision	17. Sep. 09
1.0 – 1.11	various undocumented changes	
1.12	change ball pitch and pad order, change typ. supply current remove user temperature drift programmability	8. Jan. 10
1.13	change pad layout, add fast/slow mode, add package drawing	8. Mar. 10
1.20	change pinout presentation and description, add sensitivity register, changed VIH VIL chapter 5.3.1	26. Aug. 10
1.21	Figures 7 ,8 and 9: I²C address corrected. I²C timing diagrams redrawn	30. Aug. 10
1.22	I²C Electrical specs: Vhys and Vol	24. Sep. 10
1.24	Teöperature from -30°C	20. Oct. 10

11 Copyrights

12 Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application.
The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.

Contact Information

Headquarters
austriamicrosystems AG
A-8141 Schloss Premstaetten, Austria
Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

http://www.austriamicrosystems.com/contact