AS1320

Data Sheet

200mA Step-Up DC-DC Converter

1 General Description

The AS1320 is a high-efficiency step-up DC-DC converter designed to generate a fixed voltage of +3.3V.

The AS1320 achieves an efficiency of up to 90%. The minimum input voltage is 1.5V, the output voltage is fixed at 3.3V, and output current is up to 200mA (@ 2V).

In order to save power the AS1320 features a shutdown mode, where it draws less than 1µA. In shutdown mode the battery is connected directly to the output enabling the supply of real-time-clocks.

The AS1320 provides a power-on reset output that goes high-impedance when the output reaches 90% of its regulation point.

The SHDNN trip threshold of the AS1320 can be used as an input voltage detector that disables the device when the battery voltage falls to a predetermined level.

An internal synchronous rectifier is included, thus an external transistor or Schottky diode is not required.

The AS1320 is available in a 6-pin SOT23 package.

2 Key Features

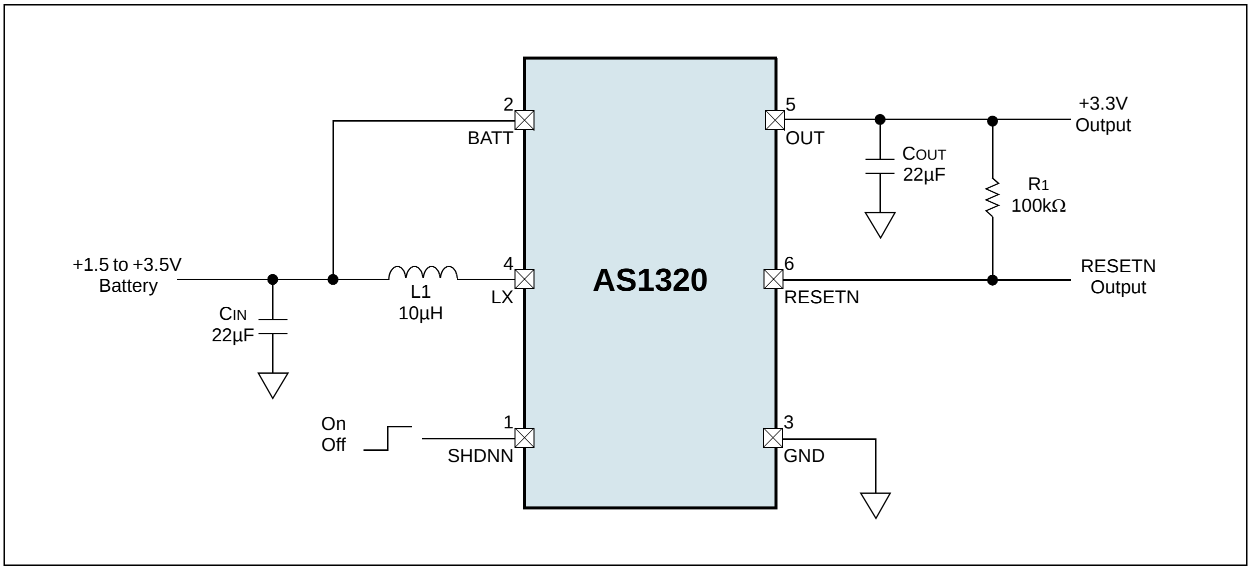
- Fixed Output Voltage: 3.3V
- Output Current: Up to 200mA (@ 2V)
- Internal Synchronous Rectifier
- Requires No External Schottky Diode or FETs
- Shutdown Mode Supply Current: Less Than 1µA
- Efficiency: Up to 90%
- Minimum Input Voltage: +1.5V
- Accurate Shutdown Low-Battery Cutoff Threshold
- Battery Input Connected to Pin OUT in Shutdown Mode for Backup Power
- 6-pin SOT23 Package

3 Applications

The AS1320 is ideal for low-power applications where ultra-small size is critical as in medical diagnostic equipment, hand-held instruments, pagers, digital cameras, remote wireless transmitters, cordless phones, and PC cards.

The device is also perfect as a local 3.3V supply or as a battery backup.

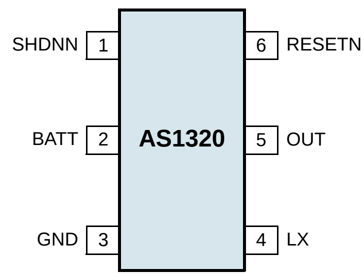
Figure 1. Application Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Name	Pin Number	Description
SHDNN	1	**Active-Low Logic Shutdown Input** 0 = The AS1320 is off and the current into BATT is ≤ 1µA (typ). 1 = The AS1320 is on.
BATT	2	**Battery Voltage Input**
GND	3	**Ground**
LX	4	**External Inductor Connection**
OUT	5	**Output Voltage**
RESETN	6	**Active-Low reset output**

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
All Pins to GND	-0.3	7	V	
LX Current		1	A	
Latch-Up	-100	100	mA	*JEDEC 78*
Package Power Dissipation (T_{AMB} = +70ºC)		500	mW	(Θ_{JA} = 9.1mW/ºC above +70ºC)
Operating Temperature Range	-40	+85	ºC	
Electrostatic Discharge	-500	+500	V	*HBM MIL-Std. 883E 3015.7* methods
Humidity (Non-Condensing)	5	85	%	
Storage Temperature Range	-55	125	ºC	
Junction Temperature		150	ºC	
Package Body Temperature		260	ºC	The reflow peak soldering temperature (body temperature) specified is in compliance with *IPC/JEDEC J-STD-020C "Moisture/ Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*.

6 Electrical Characteristics

T_{AMB} = -40 to +85ºC, V_{BATT} = +2V, V_{OUT} = +3.3, V_{SHDNN} = +1.5V (unless otherwise specified). Typ values @ T_{AMB} = +25ºC.

Table 3. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Battery Input Range	V_{BATT}		1.5		3.5	V
Startup Battery Input Voltage [1]	V_{SU}	R_{LOAD} = 47Ω, T_{AMB} = +25ºC		1.22	1.5	V
		R_{LOAD} = 47Ω, T_{AMB} = -40 to +85ºC		1.24		
Output Voltage [2]	V_{OUT}	T_{AMB} = +25ºC	3.267	3.300	3.333	V
		T_{AMB} = -40 to +85ºC	3.217		3.373	
N-Channel On-Resistance	R_{NCH}	I_{LX} = 100mA, T_{AMB} = +25ºC		0.3	1.2	Ω
		I_{LX} = 100mA, T_{AMB} = -40 to +85ºC			1.5	
P-Channel On-Resistance	R_{PCH}	I_{LX} = 100mA, T_{AMB} = +25ºC		0.4	1.3	Ω
		I_{LX} = 100mA, T_{AMB} = -40 to +85ºC			1.6	
N-Channel Switch Current Limit [1]	I_{MAX}	T_{AMB} = +25ºC	550	700	850	mA
		T_{AMB} = -40 to +85ºC	450		950	
Switch Maximum On-Time	t_{ON}	T_{AMB} = +25ºC	5	7	9	µs
		T_{AMB} = -40 to +85ºC	4		10	
Synchronous Rectifier Zero-Crossing Current		T_{AMB} = +25ºC	8	30	60	mA
		T_{AMB} = -40 to +85ºC	0		65	
Quiescent Current into OUT		V_{OUT} = +3.5V, T_{AMB} = +25ºC		35	55	µA
		V_{OUT} = +3.5V, T_{AMB} = -40 to +85ºC			60	
Shutdown Current into OUT		V_{SHDNN} = 0V, T_{AMB} = +25ºC		0.01	1	µA
		V_{SHDNN} = 0V, T_{AMB} = -40 to +85ºC			2	
Quiescent Current into BATT		V_{OUT} = +3.5V, T_{AMB} = +25ºC		0.01	1	µA
		V_{OUT} = +3.5V, T_{AMB} = -40 to +85ºC			2	
Shutdown Current into BATT		V_{SHDNN} = 0V, T_{AMB} = +25ºC		0.01	1	µA
		V_{SHDNN} = 0V, T_{AMB} = -40 to +85ºC			2	
SHDNN Logic Low [1]		V_{BATT} = +1.5 to +3.5V			0.3	V
SHDNN Threshold		Rising Edge, T_{AMB} = +25ºC	1.185	1.228	1.271	V
		Rising Edge, T_{AMB} = -40 to +85ºC	1.170		1.286	
SHDNN Threshold Hysteresis				0.02		V
RESETN Threshold		Falling Edge, T_{AMB} = +25ºC	2.830	3.000	3.110	V
		Falling Edge, T_{AMB} = -40 to +85ºC	2.800		3.140	
RESETN Voltage Low		I_{RESETN} = 1mA, V_{OUT} = +2.5V, T_{AMB} = +25ºC			0.15	V
		I_{RESETN} = 1mA, V_{OUT} = +2.5V, T_{AMB} = -40 to +85ºC			0.2	
RESETN Leakage Current		V_{RESETN} = +5.5V, T_{AMB} = +25ºC		0.1	100	nA
		V_{RESETN} = +5.5V, T_{AMB} = +85ºC		1		
LX Leakage Current		T_{AMB} = +25ºC		0.1	1000	nA
		T_{AMB} = +85ºC		10		
Maximum Load Current	I_{LOAD}	V_{BATT} = +2V		200		mA
Efficiency	η	V_{BATT} = +3V, I_{LOAD} = 100mA		90		%

1. Guaranteed by design.
2. Voltage which triggers next loading cycle. Ripple and rms value depend on external components.

7 Typical Operating Characteristics

V_{OUT} = 3.3V, V_{BATT} = +2V, T_{AMB} = +25ºC.

Figure 3. V_{OUT} vs. V_{BATT}; On, 16Ω

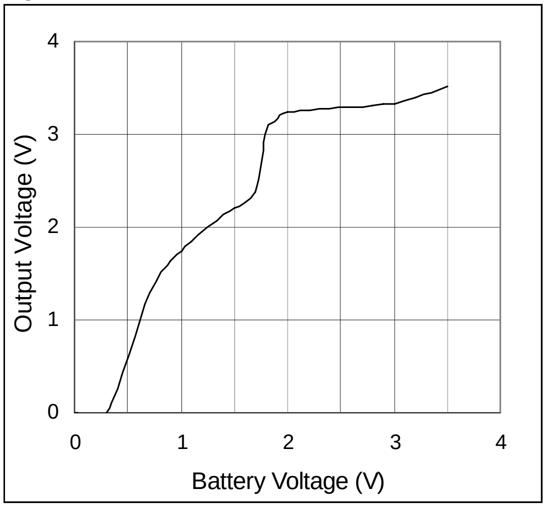


Figure 4. V_{OUT} vs. V_{BATT}; On, 330Ω

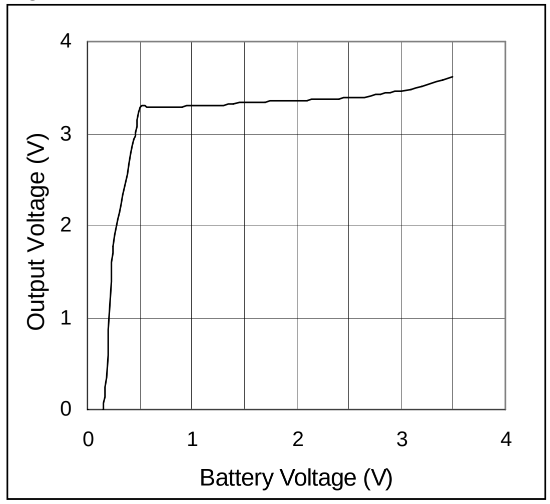


Figure 5. V_{OUT} vs. V_{BATT}; Shutdown, 200mA Load

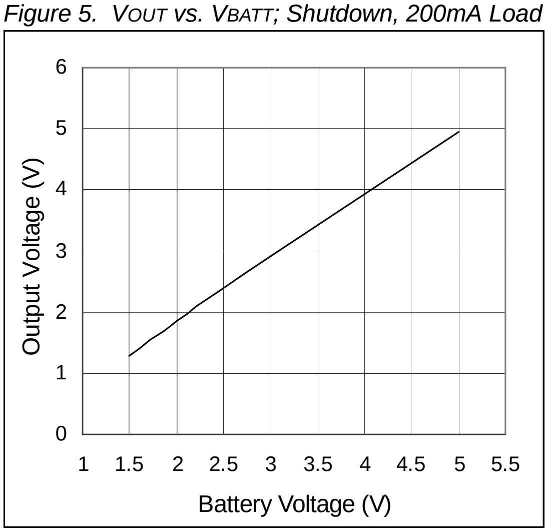


Figure 6. V_{OUT} vs. V_{BATT}; Shutdown, No Load

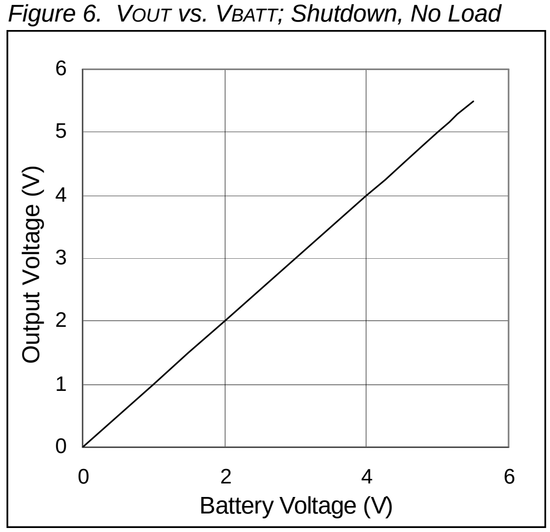


Figure 7. Maximum Output Current vs. V_{BATT}

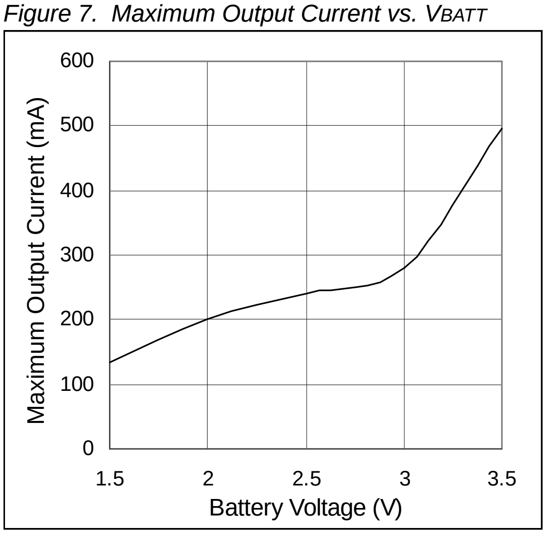


Figure 8. Startup Voltage vs. Load Resistance

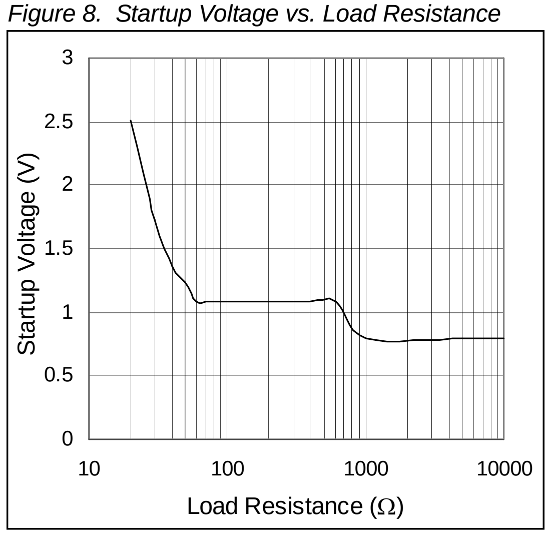


Figure 9. Line Transient

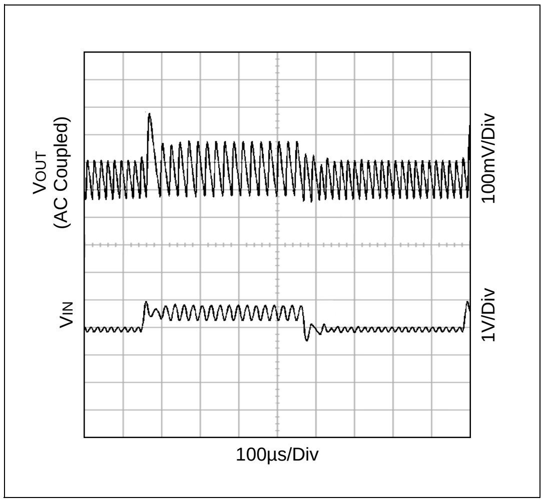


Figure 10. Load Transient

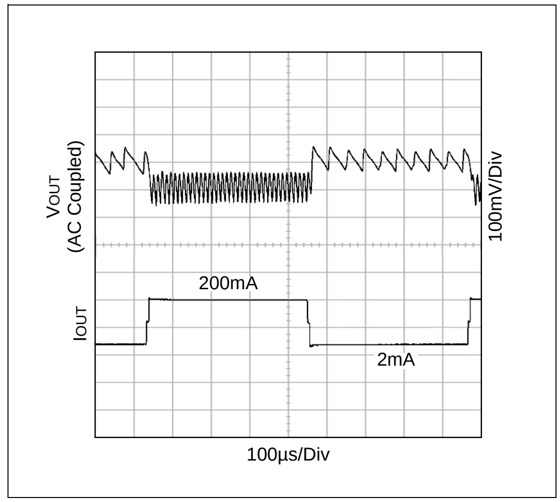


Figure 11. On/Off Response; R_{LOAD} = 33Ω

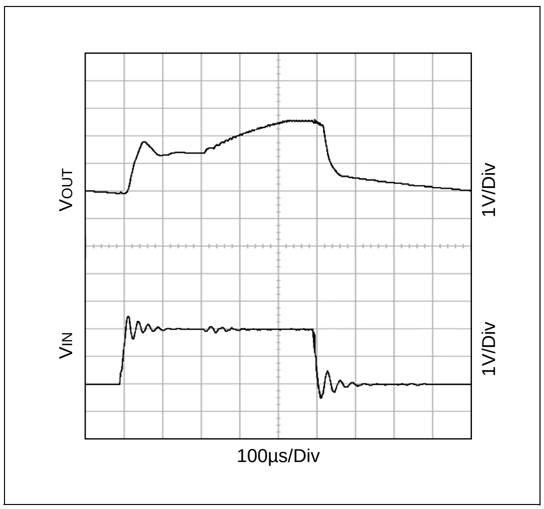


Figure 12. Shutdown Response; R_{LOAD} = 33Ω

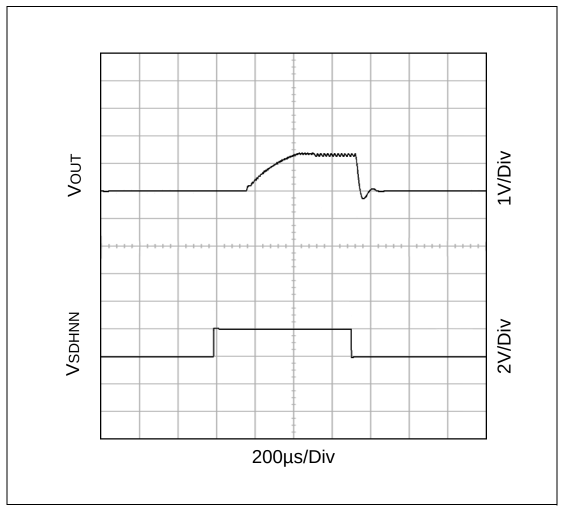


Figure 13. Switching Waveforms; R_{LOAD} = 33Ω

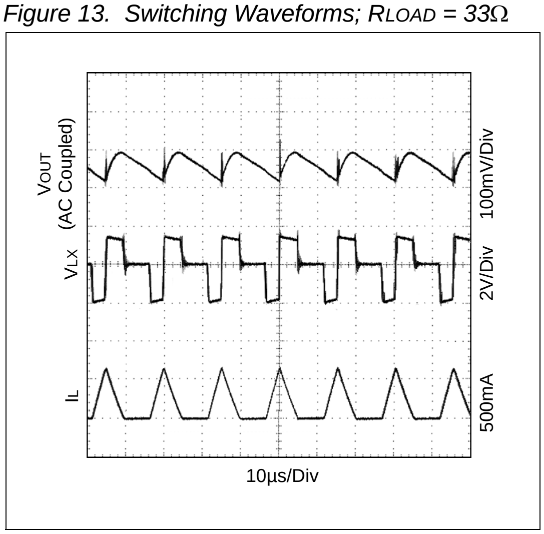
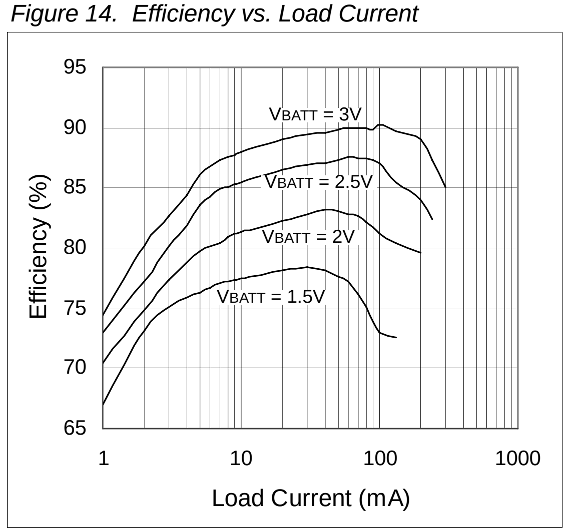


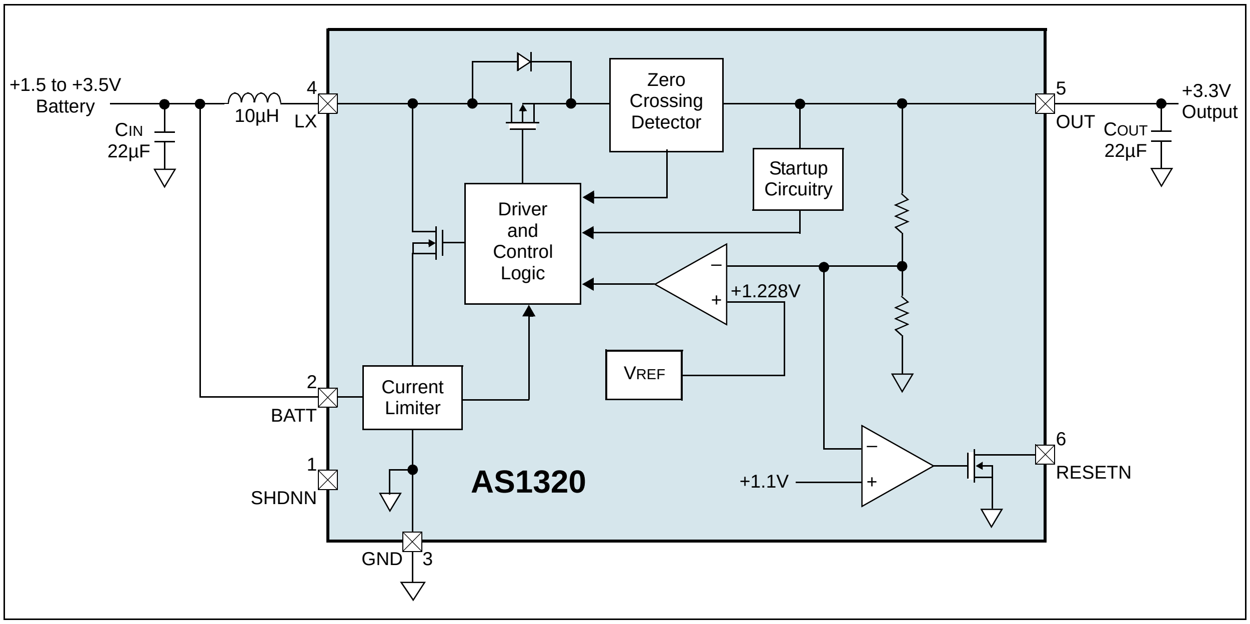
Figure 14. Efficiency vs. Load Current



8 Detailed Description

The AS1320 is a high-efficiency, compact step-up converter with 35µA quiescent supply current which ensures the highest efficiency over a wide load range. With a minimum of +1.5V input voltage, the device is well suited for applications with one- or two-cells, such as lithium ion (Li+), nickel-metal-hydride (NiMH), or alkaline.

Figure 15. Block Diagram



The input battery is connected to the device through an inductor and an internal P-FET when pin SHDNN is low. In this state, the step-up converter is off and the voltage drop across the P-FET body diode is eliminated, and the input battery can be used as a battery-backup or real-time-clock supply.

The built-in synchronous rectifier significantly improves efficiency and reduces PCB circuit size and costs by eliminating the need for an external Schottky diode.

Control Circuitry

The AS1320 integrated current-limited key circuitry provides low quiescent current and extremely-high efficiency over a wide V_{OUT} range without the need for an oscillator. Inductor current is limited by the 7µs switch maximum on-time or by the 0.7A N-channel current limit. At each cycle, the inductor current must ramp down to zero after the on-time before the next cycle may start. When the error comparator senses that the output has fallen below the regulation threshold, another cycle begins.

An internal synchronous rectifier eliminates the need for an external Schottky diode, thereby reducing costs and PCB surface area. As the inductor discharges, the P-channel MOSFET turns on and shunts the MOSFET body diode, resulting in a significant reduction of the rectifier voltage drop, improving efficiency without external components.

Shutdown

When pin SHDNN is low the AS1320 is switched off and no current is drawn from battery; when pin SHDNN is high the device is switched on. If SHDNN is driven from a logic-level output, the logic high-level (on) should be referenced to V_{OUT} to avoid intermittently switching the device on.

Note: If pin SHDNN is not used, it should be connected directly to pin OUT.

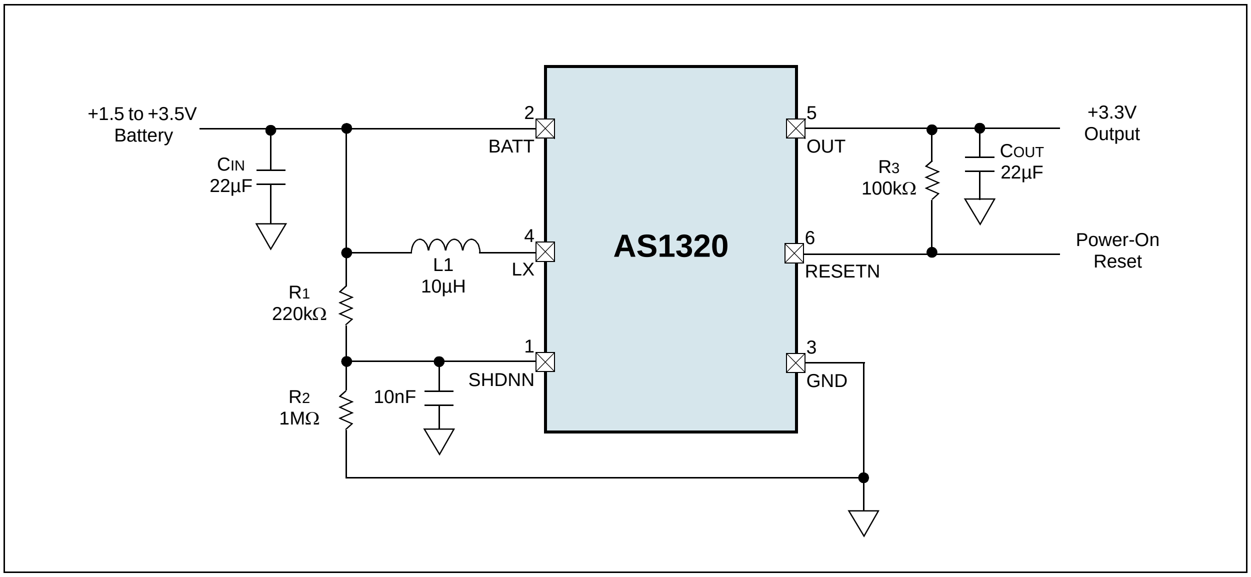
In shutdown the battery input is connected to the output through the inductor and the internal synchronous rectifier P-FET. This allows the input battery to provide backup power for devices such as an idle microcontroller, memory, or real-time-clock, without the usual diode forward drop. In this way a separate backup battery is not needed.

In cases where there is residual voltage during shutdown, some small amount of energy will be transferred from pin OUT to pin BATT immediately after shutdown, resulting in a momentary spike of the voltage at pin BATT. The ratio of C_{IN} and C_{OUT} partly determine the size and duration of this spike, as does the current-sink ability of the input device.

Low-Battery Cutoff

The AS1320 SHDNN trip threshold (1.228V) can be used as an input voltage detector that disables the device when the battery input voltage falls to a pre-set level. An external resistor-divider network can be used to set the battery-detection voltage (see Figure 16).

Figure 16. Low-Battery Cutoff Application Diagram



For the resistor-divider network shown in Figure 16, calculate the value for R_1 by:

$$R_1 = R_2 \times ((V_{OFF}/V_{SHDNN}) - 1) \quad \text{(EQ 1)}$$

Where:

V_{OFF} is the battery voltage at which the AS1320 shuts down.
V_{SHDNN} = 1.228V

The value of R_2 should be between 100kΩ and 1MΩ to minimize battery drain.

Note: Input ripple can cause false shutdowns, therefore to minimize the effect of ripple, a low-value capacitor from SHDNN to GND should be used to filter out input noise. The value of the capacitor should be such that the R/C time constant is > 2ms.

Power-On Reset

The AS1320 provides a power-on reset output (RESETN) that goes high-impedance when the output reaches 90% of its regulation point. RESETN goes low when the output is below 90% of the regulation point. A 100kΩ to 1MΩ pullup resistor between pin RESETN and pin OUT can provide a microprocessor logic control signal.

Note: Connect pin RESETN to GND when the power-on reset feature is not used.

9 Application Information

Inductor Selection

The control circuitry of the AS1320 permits a wide range of inductor values to be selected – from 4.7 to 47µH; 10µH is ideal for most applications.

The intended application should dictate the value of L. The trade-off between required PCB surface area and desired output ripple are the determining factors: smaller values for L require less PCB space, larger values of L reduce output ripple. If the value of L is large enough to prevent I_{MAX} from being reached before t_{ON} expires, the AS1320 output power will be reduced.

For maximum output current calculate the value for L as:

$$(V_{BATT(MAX)}\ (1\mu s))/0.7A < L < (V_{BATT(MIN)}(7\mu s))/0.7A \quad \text{(EQ 2)}$$

$$I_{OUT(MAX)} = [(0.7A/2)(V_{BATT(MIN)} - (0.7A/2)(R_{NCH} + R_{IND}))]/V_{OUT} \quad \text{(EQ 3)}$$

Where:

R_{IND} is the inductor series resistance.
R_{NCH} is the $R_{DS(ON)}$ of the N-channel MOSFET (0.3Ω typ).

Note: Coils should be able to handle 500mA$_{RMS}$ and have a $I_{SAT} \geq 1A$ and should have a $R_{IND} \leq 100m\Omega$.

Capacitor Selection

C_{OUT} Selection

Choose a C_{OUT} value to achieve the desired output ripple percentage. A 22µF ceramic capacitor is a good initial value. The value for C_{OUT} can be determined by:

$$C_{OUT} > (L + 2.5\mu H) \times V_{BATT(MAX)}^2 / r\% \quad \text{(EQ 4)}$$

Where:

r is the desired output ripple in %.

C_{IN} Selection

C_{IN} reduces the peak current drawn from the battery and can be the same value as C_{OUT}. A larger value for C_{IN} can be used to further reduce ripple and improve AS1320 efficiency.

PC Board Layout and Grounding

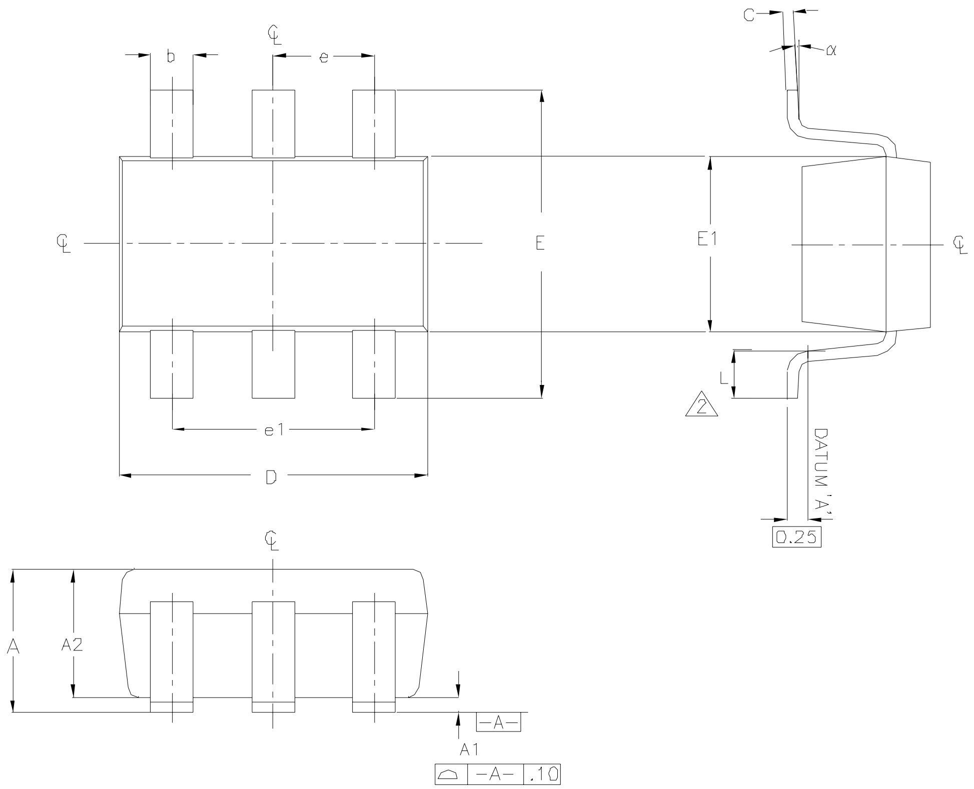
Well-designed printed circuit-board layout is important for minimizing ground bounce and noise.

- Place pin GND lead and the ground leads of C_{IN} and C_{OUT} as close to the device as possible.
- Keep the lead to pin LX as short as possible.
- To maximize output power and efficiency and minimize output ripple voltage, use a ground plane and solder the GND pin directly to the ground plane.

10 Package Drawings and Markings

The AS1320 is available in a 6-pin SOT23 package.

Figure 17. 6-pin SOT23 Package



Notes:

1. All dimensions are in millimeters.
2. Foot length is measured at the intercept point between datum A and lead surface.
3. Package outline exclusive of mold flash and metal burr.
4. Pin 1 is the lower left pin when reading the top mark from left to right.
5. Pin 1 identifier dot is 0.3mm.ϕ min and is located above pin 1.
6. Meets *JEDEC MO178*.

Symbol	Min	Max
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
α	0º	10º

11 Ordering Information

The AS1320 is available as the standard products shown in Table 4.

Table 4. Ordering Information

Part	Marking	Description	Delivery Form	Package
AS1320-T	ASD7	200mA Step-Up DC-DC Converter	Tape and Reel	6-pin SOT23

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