

# AS1301

## 5V/50mA Low Noise Inductorless Boost Converter

### 1 General Description

The AS1301 is a 50mA inductorless boost converter using a double H-bridge charge-pump topology with two external flying capacitors.

The AS1301 runs on a 1MHz fixed frequency and is utilized with a low noise regulation scheme to allow usage together with sensitive RF circuitry from the same battery supply.

Designed to reside in portable and space limited equipment the 1MHz charge pump converts a 2.7 to 5.25V input to regulated 5V output with 5% accuracy.

The shutdown function reduces the supply current to  $<5\mu\text{A}$  and disconnects the load from the output. The integrated soft-start circuitry prevents current spikes being drawn from the battery during start-up.

The AS1301 is available in TDFN (3x3x0.8mm) 10-pin and WL-CSP 8-bumps packages.

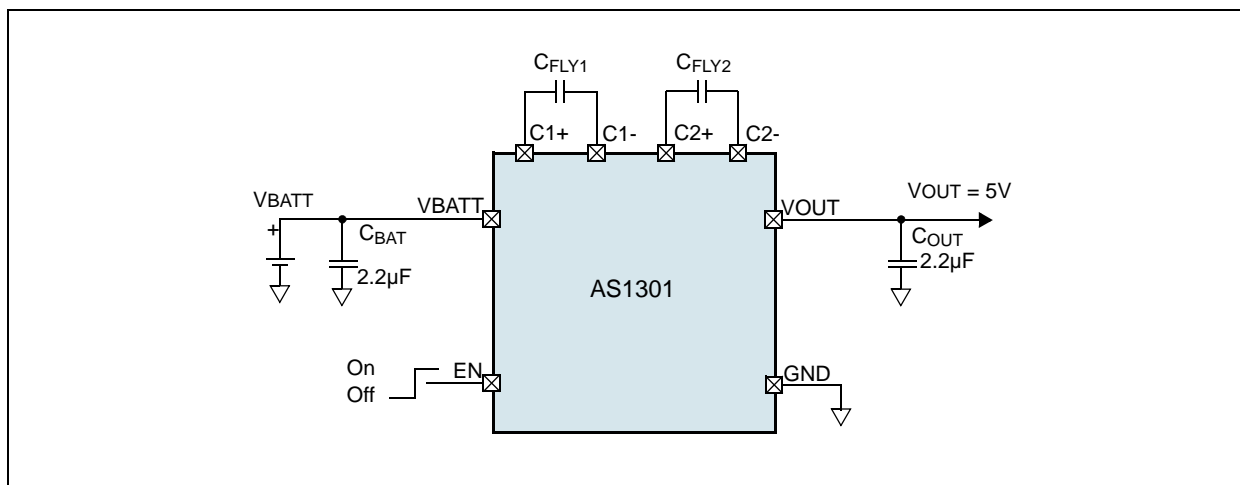
### 2 Key Features

- Up to 92% Efficiency
- 2.7 to 5.25V Input Voltage
- Regulated 5V Output
- Automatic Mode Up-Switching
- $<5\mu\text{A}$  Shutdown Current
- 5V Tolerant Enable Signal
- Up to 50mA Load Current
- Overload Protection
- Output Disconnected During Shutdown
- Soft-Start
- No Inductor Required
- Small External Components Required ( $C_{\text{OUT}} \leq 2.2\mu\text{F}$ ,  $C_{\text{FLY}} \leq 220\text{nF}$ )
- Low Noise Fixed Frequency 1MHz Charge Pump:
  - 1:1 Battery Feed Through Mode
  - 2:3 Single Phase Mode
  - 1:2 Dual Phase Mode
- Package Options:
  - TDFN (3x3x0.8mm) 10-pin
  - WL-CSP 8-bumps with 0.5mm pitch

### 3 Applications

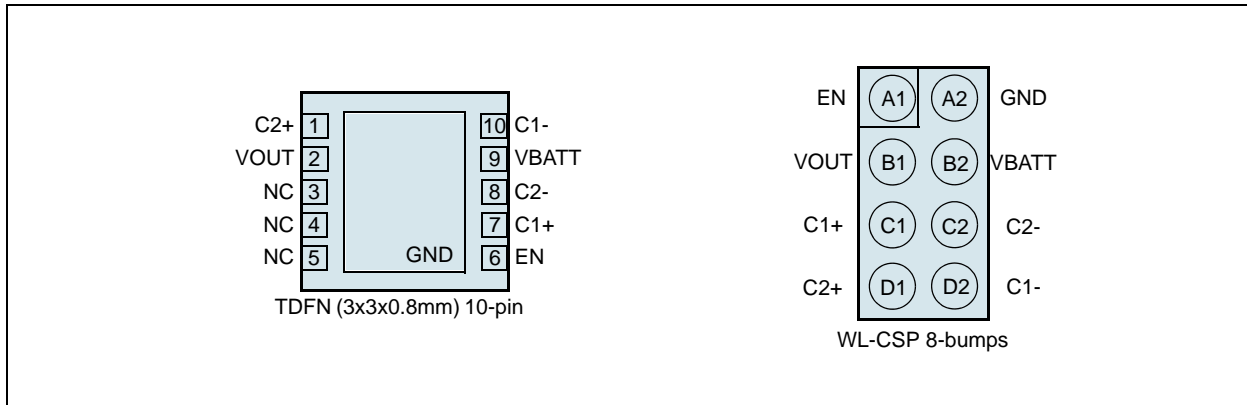
The device is ideal for two or three AA cells or a single Li-Ion battery cell to 5V conversion, mobile phones, portable instruments, microprocessor based systems and remote data-acquisition systems.

Figure 1. Typical Application Diagram



## 4 Pin Assignments

Figure 2. Pin Assignments (Through View)



### Pin Descriptions

Table 1. Pin Descriptions

Pin Name	TDFN Pinout	WLP Pinout	Description
C2+	1	D1	<b>Connector 2+.</b> Positive terminal of flying cap 2.
VOUT	2	B1	<b>+5V Output Voltage.</b> This pin must be bypassed with a $\geq 2.2\mu\text{F}$ low ESR ceramic capacitor.
NC	3	-	Connected to GND or left floating.
NC	4	-	Connected to GND or left floating.
NC	5	-	Connected to GND or left floating.
EN	6	A1	<b>Enable.</b> (operating if EN = 1). Set this digital input to logic high for normal operation. For shutdown, set to logic low.
C1+	7	C1	<b>Connector 1+.</b> Positive terminal of flying cap 1.
C2-	8	C2	<b>Connector 2-.</b> Negative terminal of flying cap 2.
VBATT	9	B2	<b>+2.7V to 5.25V Input Voltage.</b> Bypass this pin to GND with a $\geq 2.2\mu\text{F}$ low ESR ceramic capacitor.
C1-	10	D2	<b>Connector 1-.</b> Negative terminal of flying cap 1.
GND	Exposed Pad	A2	<b>Ground.</b>

## 5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Section 6 Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
All pins to GND	-0.3	+7.0	V	
Operating Temperature Range	-40	+85	°C	
Storage Temperature Range	-65	+125	°C	
ESD	2		kV	<i>HBM MIL-Std. 883E 3015.7 methods</i>
Package Body Temperature	+260		°C	The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"</i> . The lead finish for Pb-free leaded packages is matte tin (100% Sn).

## 6 Electrical Characteristics

$V_{IN} = 2.7$  to  $5.25V$ ,  $V_{OUT} = 5V$ ,  $C_{OUT} = C_{BAT} = 2.2\mu F$ ,  $C_{FLY1} = C_{FLY2} = 220nF$ ,  $T_{AMB} = -40$  to  $+85^{\circ}C$ . Typical values are at  $T_{AMB} = +25^{\circ}C$ , unless otherwise specified.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{ON}$	Startup Voltage, Rising $V_{BATT}$			2.8	2.865	V
$V_{OFF}$	Startup Voltage, Falling $V_{BATT}$		2.505	2.7	2.8	V
$V_{BATT}$	Battery Supply Voltage		$V_{ON}/V_{OFF}$	3.6	5.25	V
$V_{OUT}$	Settled Average Output Voltage		4.75	5.0	5.25	V
$I_{OUT}$	Load Current <sup>1</sup>	after startup of 1ms	0		50	mA
$V_{ripple}$	Output Voltage Ripple	$C_{OUT} = 2.2\mu F$ , 50mA load		15		mV <sub>PP</sub>
$t_{START}$	Startup Time				1	ms
$I_{inr}$	Inrush Current <sup>2</sup>				500	mA
$\Delta V_O/\Delta I_{O11}$	Load Regulation in 1:1 Mode	$V_{BATT} = 5V$ , $I_{OUT} = 10\sim 50mA$		2		mV/mA
$\Delta V_O/\Delta I_{O23}$	Load Regulation in 2:3 Mode	$V_{BATT} = 4.5V$ , $I_{OUT} = 10\sim 50mA$		3		
$\Delta V_O/\Delta I_{O12}$	Load Regulation in 1:2 Mode	$V_{BATT} = 3.1V$ , $I_{OUT} = 10\sim 50mA$		3		
$\eta_{12}$	Efficiency in Switching Mode	$V_{BATT} = 3.1V$ , $I_{OUT} = 30mA$		90		%
$\eta_{23}$	Efficiency in Switching Mode	$V_{BATT} = 3.5V$ , $I_{OUT} = 30mA$		90		%
$f_{OSC}$	Oscillator Frequency	optional selectable		1		MHz
$t_{debut}$	Up Switching Debounce Time			256		$\mu s$
$I_{OP12}$	Operating Quiescent Current	1:2 mode without load		1.5	3.5	mA
$I_{OP23}$	Operating Quiescent Current	2:3 mode without load		1.3	3	
$I_{OP11}$	Operating Current 1:1 Mode	without load		0.1	0.3	
$I_{OFF}$	Shutdown Current	$EN = 0V$		0.7	5	$\mu A$
$T_{OFFL}$	Temperature Shutdown	mode off		145		$^{\circ}C$
$T_{OFFH}$	Temperature Shutdown	mode on		170		$^{\circ}C$
<b>Input Levels</b>						
$V_{IH}$	Input High Level	pin EN	1.5		5.5	V
$V_{IL}$	Input Low Level		0.0		0.5	V

1. The device is tested in a proprietary test mode.
2. The inrush current is limited by the internal soft-start circuitry.

## 7 Typical Operating Characteristics

$V_{IN} = 2.7$  to  $5.25$ V,  $V_{OUT} = 5$ V,  $C_{OUT} = C_{BAT} = 2.2\mu$ F,  $C_{FLY1} = C_{FLY2} = 220$ nF,  $T_{AMB} = +25^{\circ}$ C, unless otherwise specified.

Figure 3. Efficiency vs. Input Voltage;  $I_{LOAD} = 10$ mA

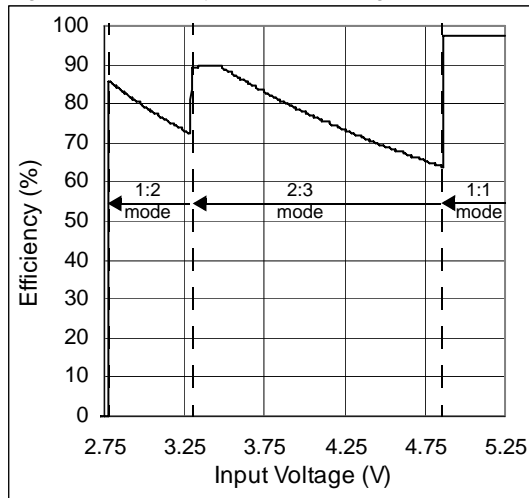


Figure 4. Efficiency vs. Input Voltage;  $I_{LOAD} = 20$ mA

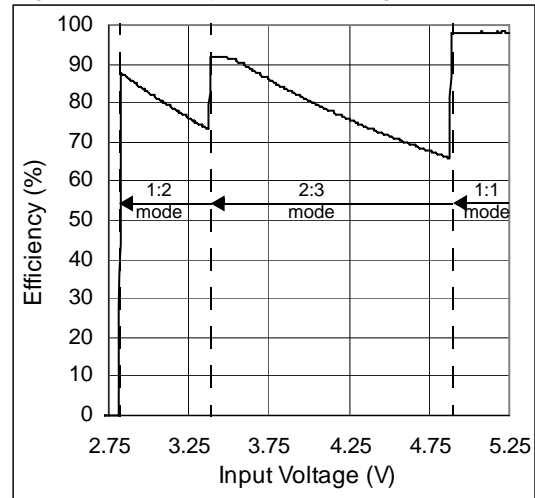


Figure 5. Efficiency vs. Input Voltage;  $I_{LOAD} = 30$ mA

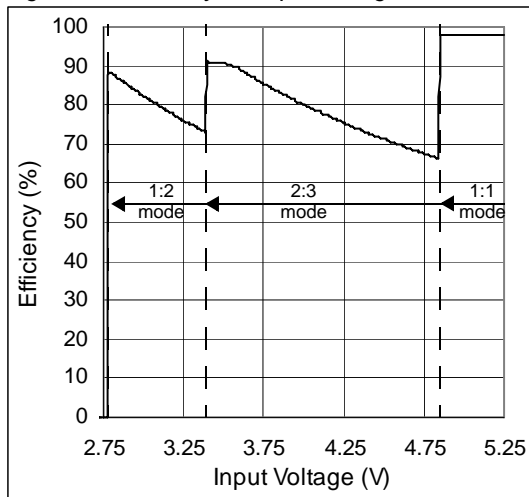


Figure 6. Efficiency vs. Input Voltage;  $I_{LOAD} = 40$ mA

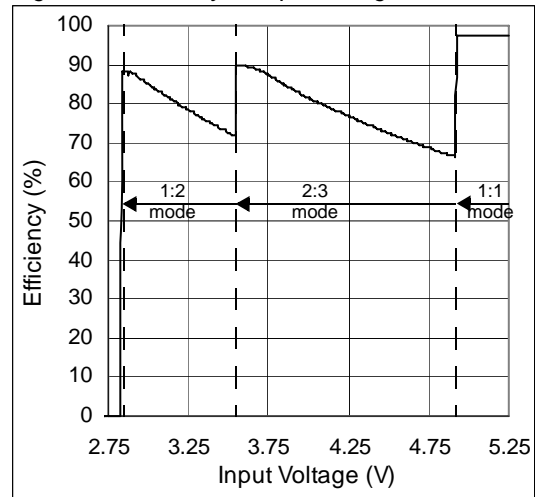


Figure 7. Efficiency vs. Input Voltage;  $I_{LOAD} = 50$ mA

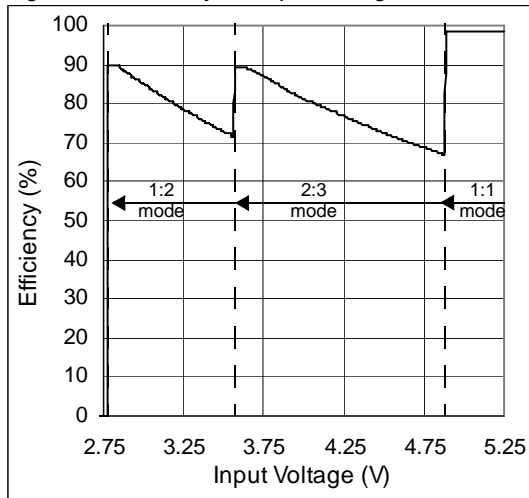


Figure 8. Quiescent Current vs. Input Voltage

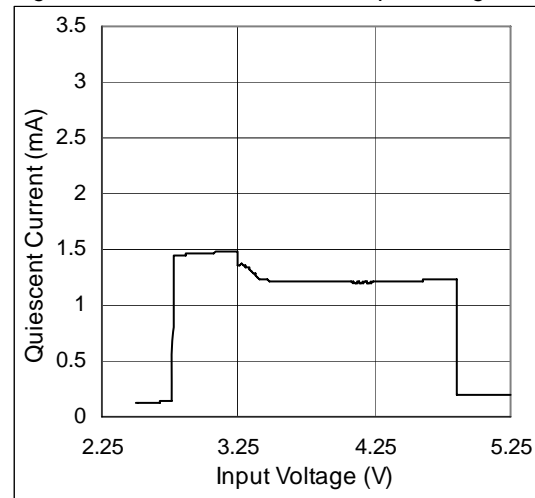


Figure 9. Output Voltage vs. Output Current

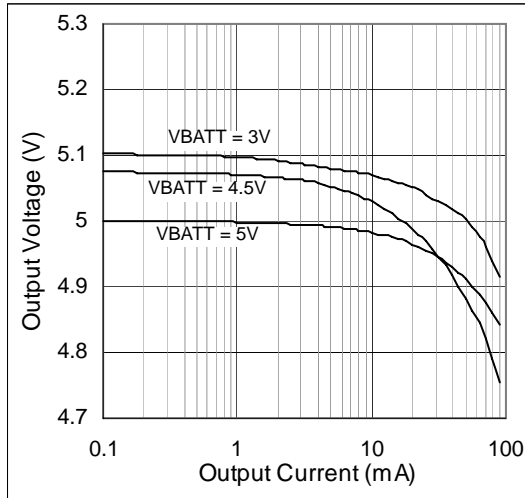


Figure 10. Output Voltage vs. Output Current

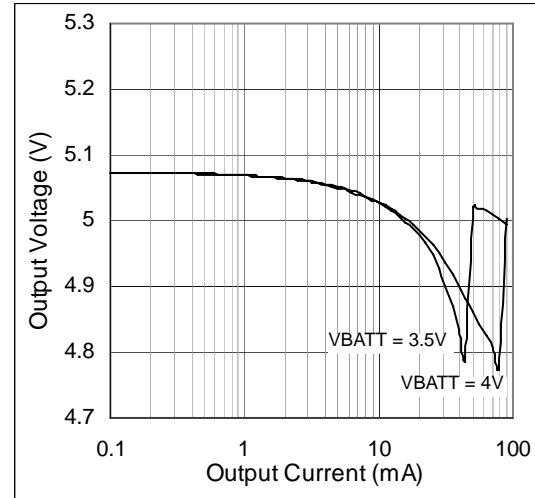


Figure 11. Output Voltage vs. Input Voltage

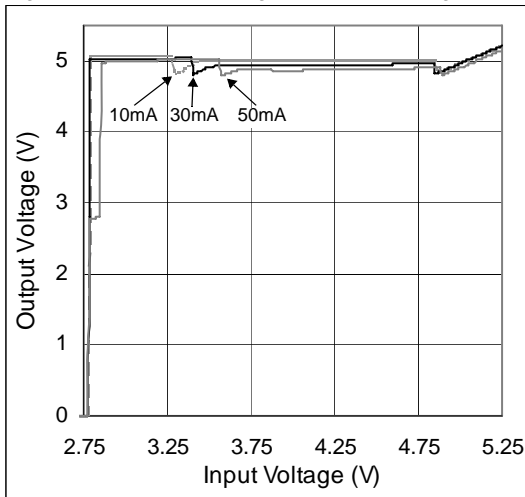


Figure 12. Output Voltage vs. Temp.; IOUT = 0.1mA

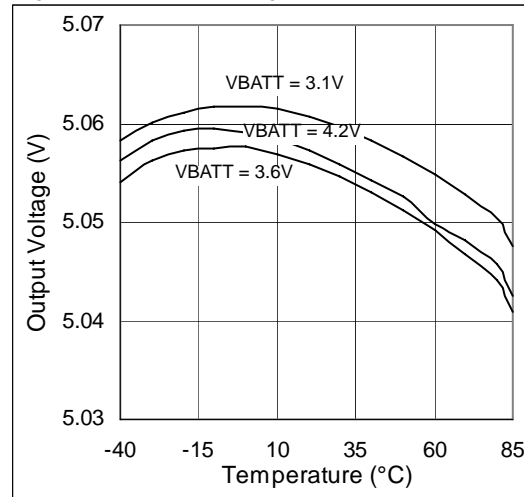


Figure 13. Output Voltage vs. Temp.; IOUT = 10mA

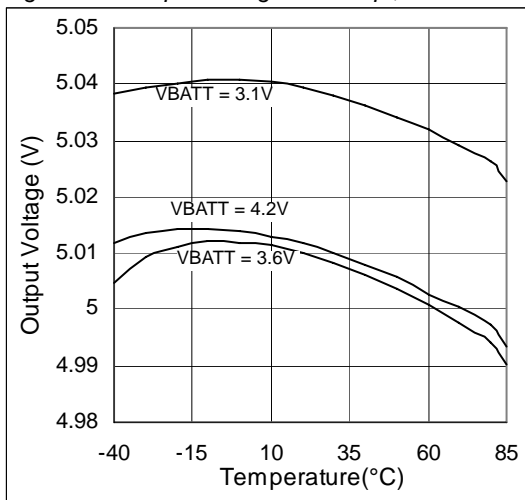


Figure 14. Output Voltage vs. Temp.; IOUT = 30mA

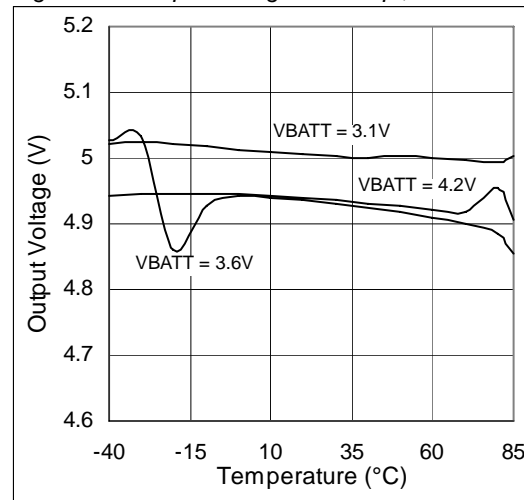


Figure 15. Efficiency vs. Output Current;  $V_{IN} = 3V$

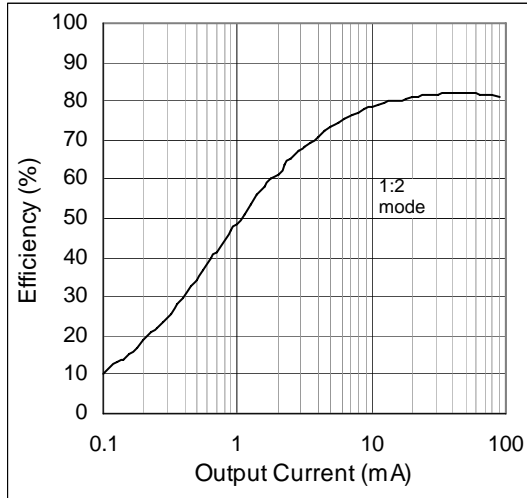


Figure 16. Efficiency vs. Output Current;  $V_{IN} = 3.3V$

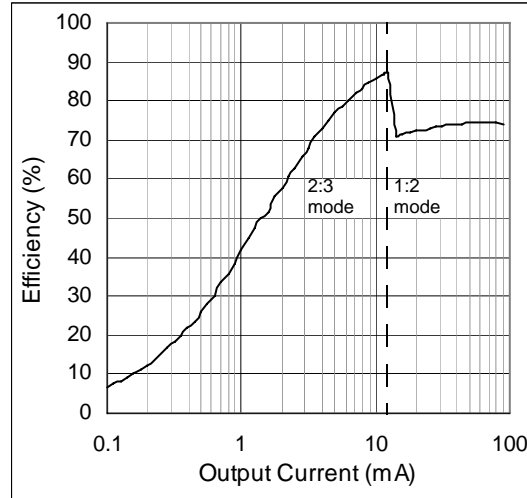


Figure 17. Efficiency vs. Output Current;  $V_{IN} = 3.5V$

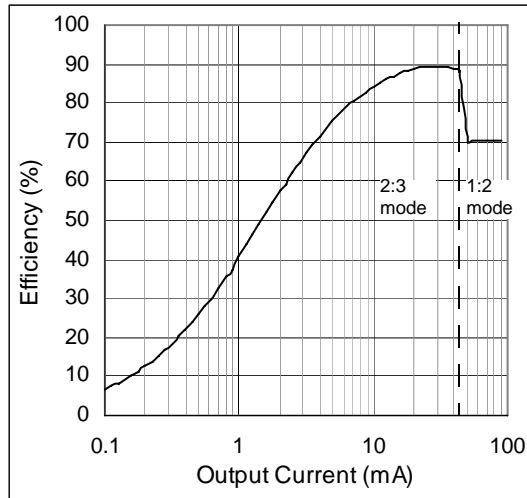


Figure 18. Efficiency vs. Output Current;  $V_{IN} = 4V$

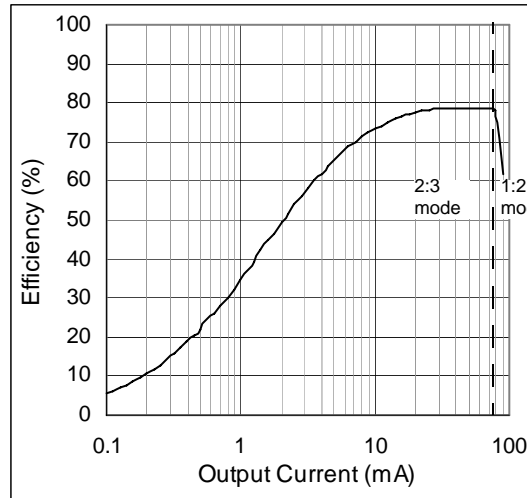


Figure 19. Efficiency vs. Output Current;  $V_{IN} = 4.3V$

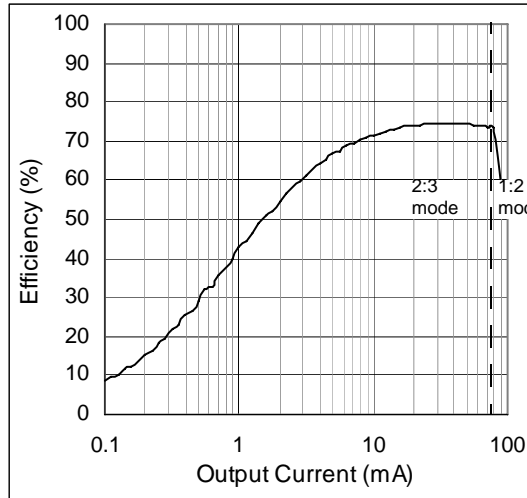


Figure 20. Efficiency vs. Output Current;  $V_{IN} = 4.7V$

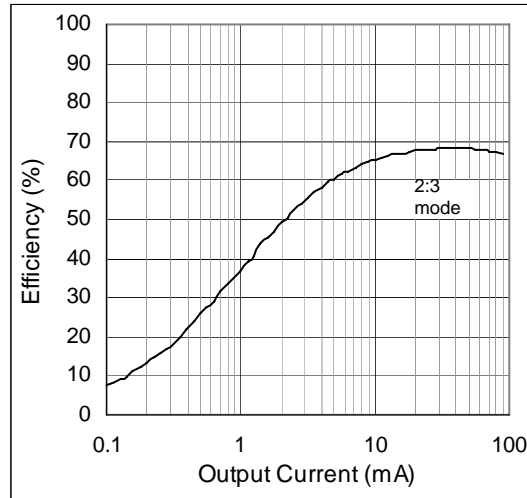


Figure 21. Load Transient;  $V_{BATT} = 5.2V$

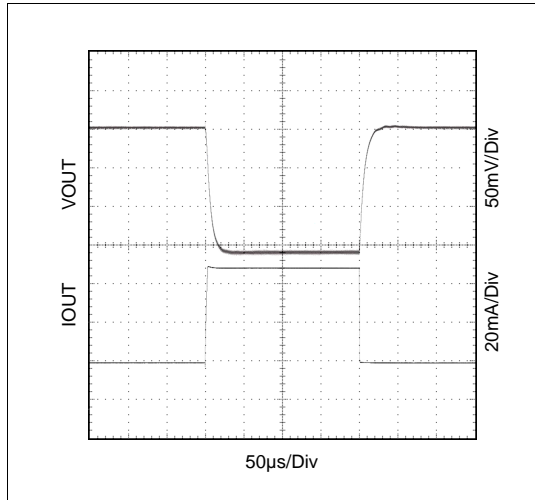


Figure 22. Load Transient;  $V_{BATT} = 3.6V$

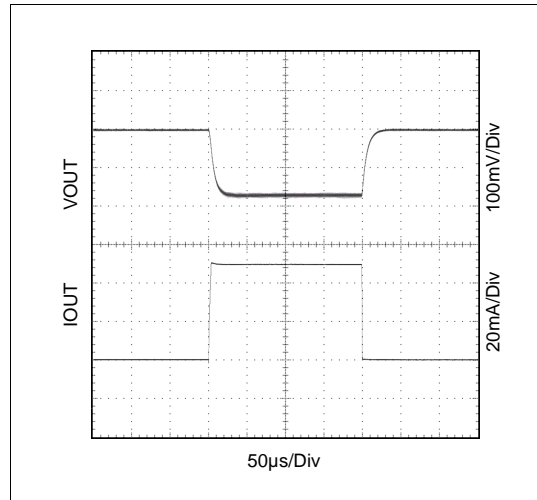


Figure 23. Start-Up Time;  $V_{BATT} = 3V$

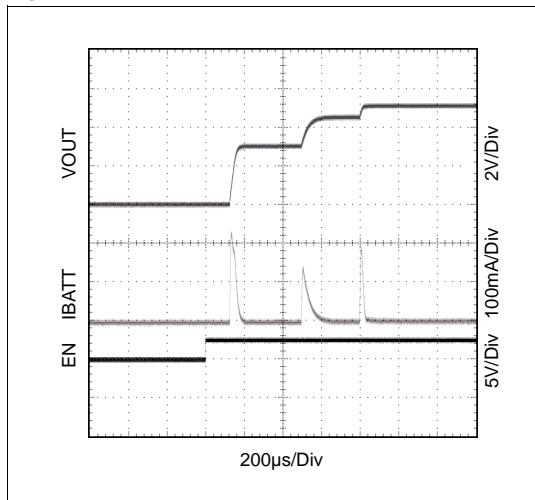


Figure 24. Start-Up Time;  $V_{BATT} = 5.25V$

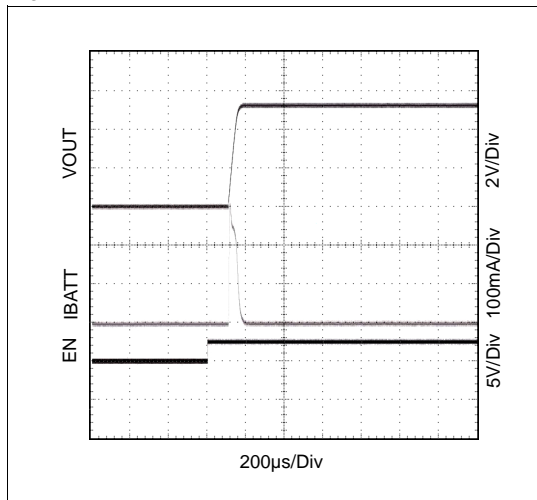
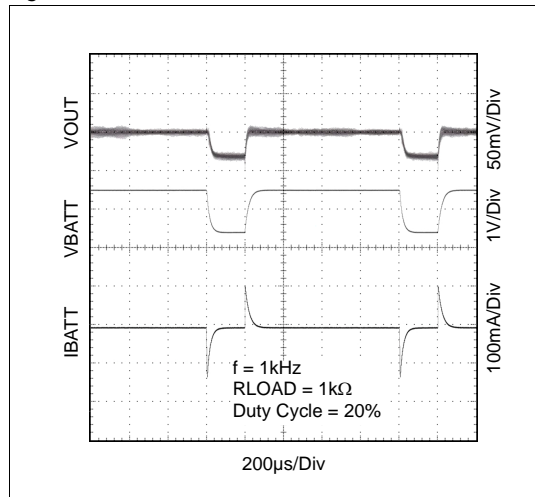


Figure 25. Line Transient;  $V_{BATT} = 4.5V$  to  $3.5V$





## 8 Detailed Description

### Operating Principle

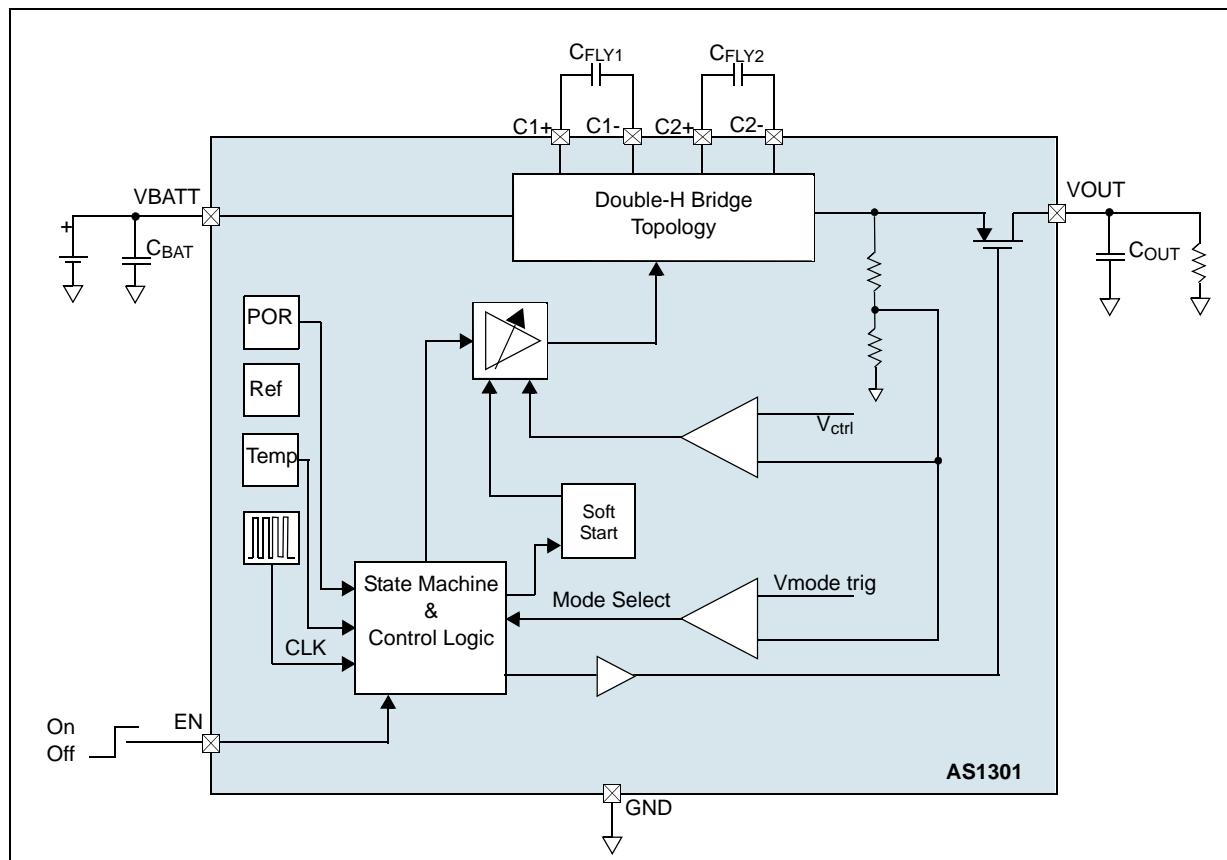
#### Functional Description

The AS1301 is a high efficiency and low noise switched capacitor DC-DC converter that is capable of boost operation. It is equipped with two built-in coupled H-bridge type switch configurations. Based on the value of the output voltage the system automatically initiates mode-switching to achieve the highest possible efficiency. The regulation of the output voltage is achieved by a regulation loop, which modulates the current drive capability of the power transistors so that the amount of charge transferred from the input to the output at each clock cycle is controlled and is equal to the charge needed by the load.

#### Regulation Loop

The AS1301 operates at constant frequency at any load. For the regulation loop power transistors, a resistor divider, and an error amplifier is used to keep the output voltage within the allowed limits. The error amplifier takes the feedback and reference signals as inputs and generates the error voltage signal. The error voltage controls a driver that triggers the gate of the power transistor which modulates the current drive capability of the power transistors. The modulated power transistors control the charge transferred from the input to the output and therefore the regulation of the output voltage is realized. Based on adjusting the amount of charge transferred, this regulation concept delivers the smallest voltage ripple possible.

Figure 26. Functional Block Diagram

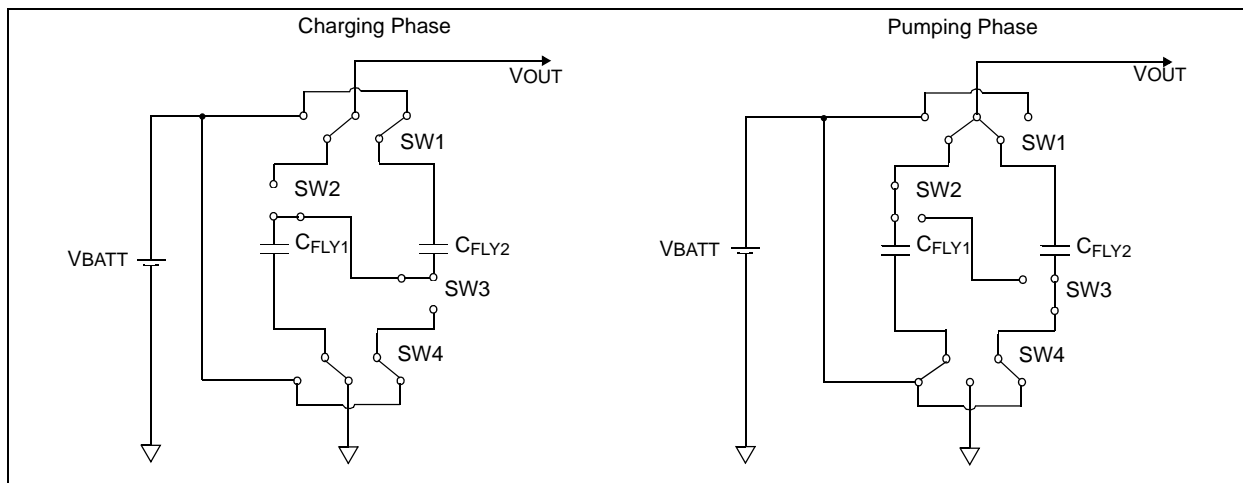


### Switch Configuration

The AS1301 has nine built-in power switches in the shape of two coupled H-bridge topologies. The system features 1:2 and 2:3 operation modes as well as a 1:1 operation where the input is directly connected to the output. This feedthrough mode is suitable for input voltages higher than the output voltage.

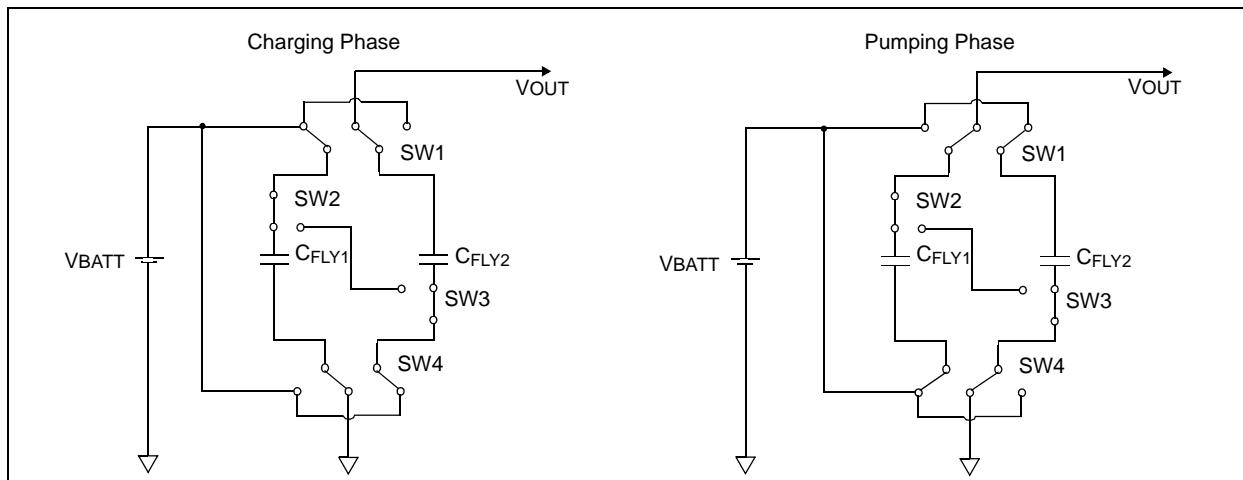
In 2:3 operation mode two flying capacitors are placed in series and each capacitor is charged to a half of the input voltage. In pumping phase the flying capacitors are placed in parallel. The bottom-plates of the parallel flying capacitors  $C_{FLY1}$  and  $C_{FLY2}$  are then connected to the input voltage so that the voltage at the top-plates of the flying capacitors is boosted to a voltage equal to  $V_{BATT} + V_{BATT}/2$ . By connecting the top-plates of the capacitors to the output, the output voltage in 2:3 mode can be up to one and a half of  $V_{BATT}$ . If the top-plate voltage is higher than 5V, the regulation loop adapts the power transistor's current drive capability to drop some voltage. The 2:3 operation mode runs in single-phase operation only.

Figure 27. 2:3 Operating Mode



In 1:2 operation mode just one of both flying capacitors is placed in series to the input voltage, and therefore charged to the input voltage. During pumping phase the input voltage is connected to the bottom-plate of the discharged flying capacitor  $C_{FLY}$ . The voltage at the top-plate of the capacitor is now boosted to  $2V_{BATT}$ . By connecting the top-plate of the capacitor to the output, the output can be charged to twice the voltage of  $V_{BATT}$ . If the top-plate voltage is higher than 5V the regulation loop limits the charge transfer to the output. In collaboration with the second flying capacitor this mode features dual-phase operation.

Figure 28. 1:2 Operating Mode



### Overload Protection

When the output voltage drops significantly below battery voltage due to a very high load the AS1301 enters into an overload protection condition. In this condition the output is connected to the input via a current limiting connection. Once the overload is removed, the device enters soft-start period and ramps up to the nominal output voltage.

### Undervoltage Lockout, UVLO

The AS1301 is equipped with undervoltage lockout functionality. If the battery voltage drops below 2.7V (typ) the device enters the undervoltage lockout condition. The device remains in this condition until the battery voltage is high enough to enter the soft-start period. An internal hysteresis of 100mV will prevent ringing during startup. If the input voltage climbs back to 2.8V (typ) after such a condition, the device turns-on automatically.

### Shutdown Mode

The AS1301 enters low-power shutdown mode when EN is set to logic low. In shutdown the charge-pump action is halted, the output is completely disconnected from the input and  $V_{OUT}$  will drop to 0V. During shutdown the output is set to a high-Z condition. So it can be forced higher voltage than the input, because the permanent monitoring of the input- and output voltage will prevent an erroneous current from the output back to the input during shutdown.

### Thermal Shutdown

The AS1301 offers thermal shutdown, which prevents eventual damage due to an over-temperature condition. Thermal shutdown will be initiated if the junction temperature exceeds 145°C. If the temperature drops below this value, the thermal shutdown will be released automatically and the device will resume operation.

## 9 Application Information

### External Component Selection

The high internal oscillator frequency of 1MHz permits the use of small capacitors for both, the flying capacitors and the output capacitors. For any given load value of the flying- and output capacitors as well as their ESR are affecting the output voltage performance.

In general, the capacitor's ESR is inversely proportional to its physical size. Larger capacitances and higher voltage ratings tend to reduce ESR. The ESR is a function of the frequency too, so it must be rated at the devices operating frequency. Another factor affecting capacitor ESR is temperature.

**Note:** Many capacitors have a huge capacity variation over temperature. This can be compensated by choosing a capacitor with a better thermal coefficient or by choosing a larger nominal value to ensure proper operation over temperature.

### Input and Output Capacitor Selection

It is not critical which type of input bypass capacitor  $C_{BAT}$  and output filter capacitor  $C_{OUT}$  is used, but it will affect the performance of the charge pump. Low ESR capacitors should be used to minimize  $V_{OUT}$  ripple. Multi-layer ceramic capacitors are recommended since they have extremely low ESR and are available in small footprints.

#### Input Capacitor

An  $2.2\mu\text{F}$  input bypass low ESR capacitor such as tantalum or ceramic is recommended to reduce noise and supply transients. During startup and mode change it supplies part of the peak input current drawn by the device.

#### Output Capacitor

The output capacitor is charged to the  $V_{OUT}$  voltage during pumping phase. The ESR of the output capacitor introduces steps in the output voltage waveform whenever the charge pump charges  $C_{OUT}$ . These steps contribute to the ripple voltage of  $V_{OUT}$ . Therefore, ceramic or tantalum low ESR capacitors are recommended for  $C_{OUT}$  to minimize the output voltage ripple.

Table 4. Recommended Input and Output Capacitor

Part Number	C	TC Code	Rated Voltage	Dimensions (L/W/T)	Manufacturer
GRM21BR71A225KA01	$2.2\mu\text{F}$	X7R	10V	2x1.2x1.35mm	Murata <a href="http://www.murata.com">www.murata.com</a>

### Flying Capacitor Selection

To ensure the required output current and avoid high peak currents the values of the flying capacitors  $C_{FLY1}$  and  $C_{FLY2}$  are very critical. A  $220\text{nF}$  capacitor is sufficient for most applications. Dependent on the operation mode the AS1301 alternately charges and discharges  $C_{FLY1/2}$ . Since the flying capacitors lead a higher current than the output capacitor the ESR of  $C_{FLY1/2}$  has a greater impact on the performance of the whole system. The voltage drop caused by the ESR of the flying capacitors directly adds to the output source resistance of the charge pump.

Therefore low ESR capacitors, e.g. tantalum or ceramic, are recommended for the flying capacitors as well.

Table 5. Recommended Flying Capacitor

Part Number	C	TC Code	Rated Voltage	Dimensions (L/W/T)	Manufacturer
GRM188R71E224KA88	$220\text{nF}$	X7R	25V	1.6x0.8x0.87mm	Murata <a href="http://www.murata.com">www.murata.com</a>

## 10 Package Drawings and Markings

The device is available in a TDFN (3x3x0.8mm) 10-pin and WL-CSP 8-bumps package.

Figure 29. TDFN (3x3x0.8mm) 10-pin package Diagram

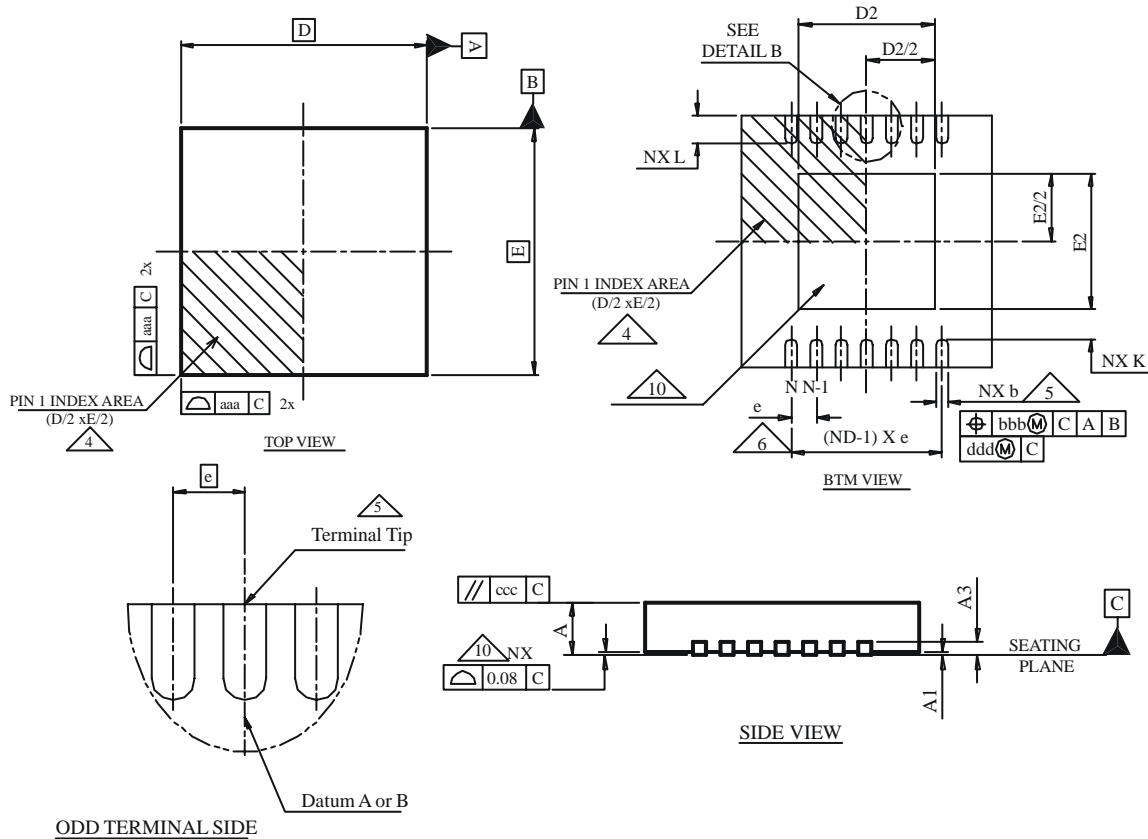


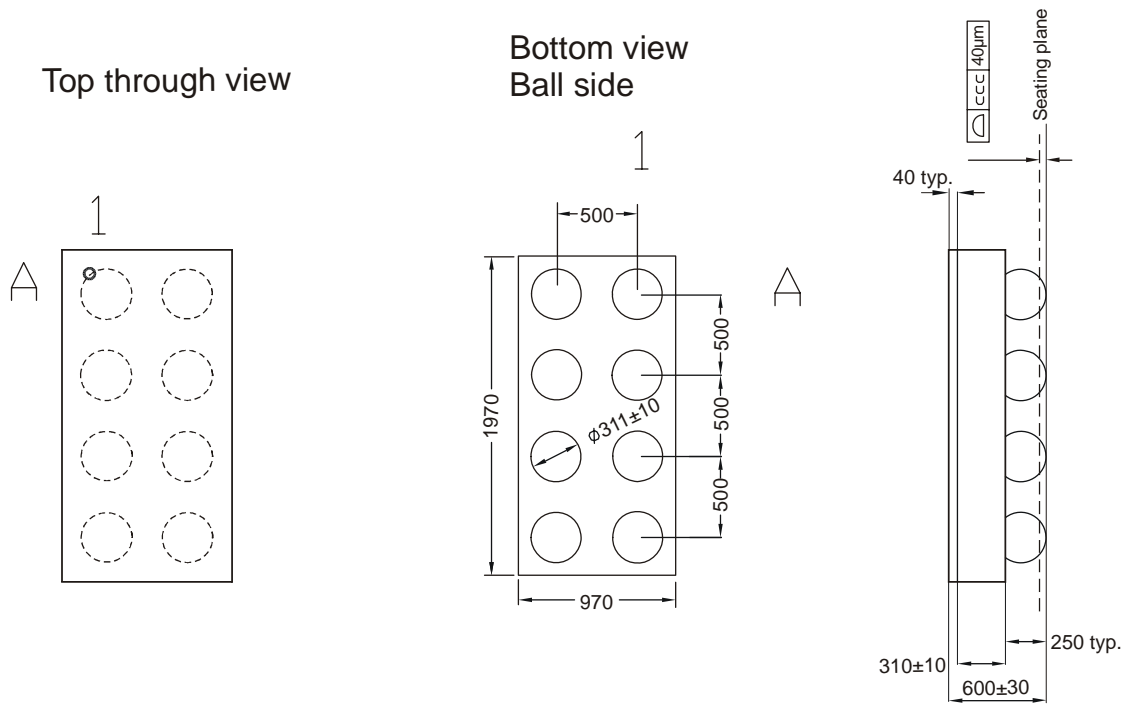
Table 6. TDFN (3x3x0.8mm) 10-pin package Dimensions

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.70	0.75	0.80	D BSC		3.00	
A1	0.00	0.02	0.05	E BSC		3.00	
A3		0.20 REF		D2	2.20		2.70
L1	0.03		0.15	E2	1.40		1.75
L2			0.13	L	0.30	0.40	0.50
aaa		0.15		$\theta$	0°		
bbb		0.10		k	0.20		
ccc		0.10		b	0.18	0.25	0.30
ddd		0.05		e		0.50	
eee		0.08		N		10	
ggg		0.10		ND		5	

**Note:**

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters, angle is in degrees.
3. N is the total number of terminals.

Figure 30. WL-CSP 8-bumps Package Diagram



**Notes:**  
ccc Coplanarity  
All dimensions in μm

## 11 Ordering Information

Table 7. Ordering Information

Part	Marking	Description	Delivery Form	Package
AS1301A-BWLT	ASO4	5V/50mA Low Noise Inductorless Boost Converter	T&R	WL-CSP 8-bumps
AS1301A-BTDT	ASO4	5V/50mA Low Noise Inductorless Boost Converter	T&R	TDFN (3x3x0.8mm) 10-pin

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