

## General Description

The AAT4650 SmartSwitch is a single channel PC card (PCMCIA) power switch. It is used to select between two different voltage inputs, each between 2.7V and 5.5V. An internal switch powers the circuitry from whichever input voltage is higher. The device's output,  $V_{CC}$ , is slew rate controlled and current limited, in compliance with PC card specifications. The current limit response time to a short circuit is typically  $1\mu\text{s}$ . The internal P-channel MOSFET switches are configured to break before make; that is, both switches cannot be closed at the same time. Controlled by a 2-bit parallel interface, the four states for  $V_{CC}$  are  $V_{CC5}$ ,  $V_{CC3}$ , high impedance, or ground. When in the ground state,  $V_{CC}$  is pulled to ground by a  $5\text{k}\Omega$  resistor. An open drain  $\overline{\text{FAULT}}$  output is asserted during over-current conditions. During power-up slewing,  $\overline{\text{FAULT}}$  also signals that  $V_{CC}$  is out of tolerance. An internal over-temperature sensor forces  $V_{CC}$  to a high impedance state when an over-temperature condition exists. Quiescent current is typically a low  $15\mu\text{A}$ , as long as  $I_{CC}$  is less than approximately  $500\text{mA}$ . Above this load current, the quiescent current increases to  $200\mu\text{A}$ .

The AAT4650 is available in a Pb-free, 8-pin SOP or TSSOP package and is specified over the  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  temperature range.

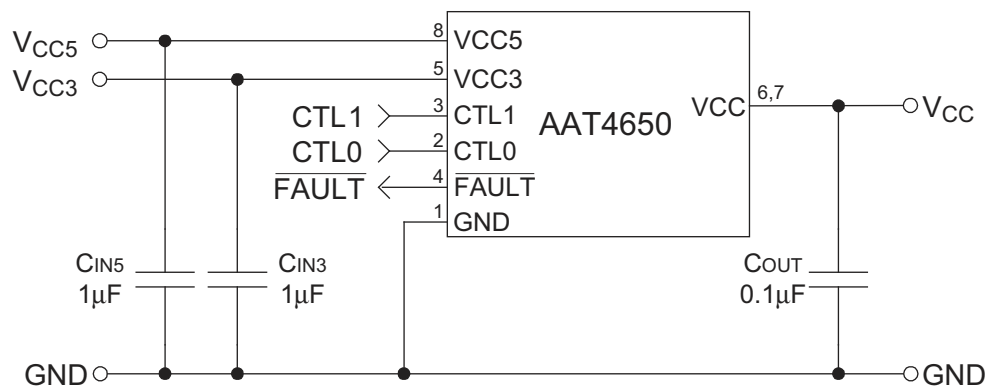
## Features

- 2.7V to 5.5V Input Voltage Range
- $80\text{m}\Omega$  (5V) Typical  $R_{DS(ON)}$
- Low Quiescent Current  $15\mu\text{A}$  (typ)
- Reverse-Blocking Switches
- Short-Circuit Protection
- Over-Temperature Protection
- $\overline{\text{FAULT}}$  Flag Output
- Temperature Range:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
- 8-Pin SOP or TSSOP Package

## Applications

- Notebook Computer
- PDA, Subnotebook
- Power Supply Multiplexer Circuit

## Typical Application

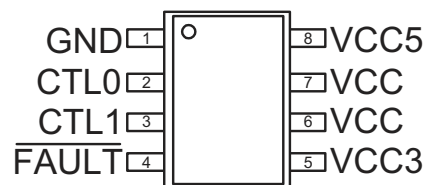


## Pin Descriptions

| Pin # | Symbol | Function   |
|-------|--------|--|
| 1     | GND    | Ground connection.                                 |
| 2     | CTL0   | Control input (see Control Logic Table below).     |
| 3     | CTL1   | Control input (see Control Logic Table below).     |
| 4     | FAULT  | Open drain output; signals over-current condition. |
| 5     | VCC3   | 3V supply.   |
| 6, 7  | VCC    | Output (see Control Logic Table below).            |
| 8     | VCC5   | 5V supply.   |

## Pin Configuration

**SOP-8 / TSSOP-8**  
(Top View)



## Control Logic Table

| CTL1 | CTL0 | Function | Result        |
|------|------|----------|---------------|
| 0    | OFF  | 5k       | VCC to GND    |
| 0    | 1    | 1 5V     | VCC = VCC5    |
| 1    | 0    | 3V       | VCC = VCC3    |
| 1    | 1    | HiZ      | Both FETs OFF |

## Absolute Maximum Ratings<sup>1</sup>

T<sub>A</sub> = 25°C, unless otherwise noted.

| Symbol                              | Description                              | Value           | Units |
|-------------------------------------|--|-----------------|-------|
| V <sub>CC3</sub> , V <sub>CC5</sub> | IN to GND                                | -0.3 to 6       | V     |
| V <sub>CC</sub>                     | OUT to GND                               | -0.3 to 6       | V     |
| I <sub>MAX</sub>                    | Maximum Continuous Switch Current        | Current Limited | A     |
| T <sub>J</sub>                      | Operating Junction Temperature Range     | -40 to 150      | °C    |
| T <sub>LEAD</sub>                   | Maximum Soldering Temperature (at Leads) | 300             | °C    |
| V <sub>ESD</sub>                    | ESD Rating <sup>2</sup> — HBM            | 4000            | V     |

## Thermal Characteristics<sup>3</sup>

| Symbol          | Description        | Value   | Units |
|-----------------|--------------------|---------|-------|
| Θ <sub>JA</sub> | Thermal Resistance | SOP-8   | 120   |
|                 |                    | TSSOP-8 | 150   |
| P <sub>D</sub>  | Power Dissipation  | SOP-8   | 1.0   |
|                 |                    | TSSOP-8 | 833   |

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.

2. Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

3. Mounted on an FR4 board.

## Electrical Characteristics

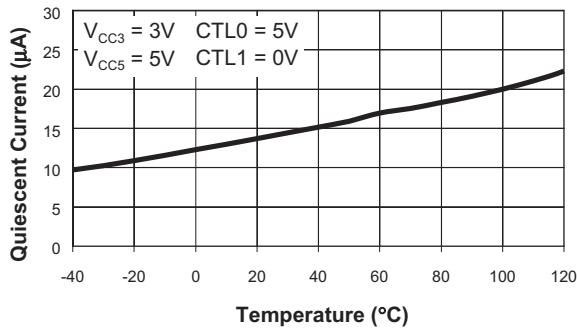
$V_{IN} = 5V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = 25^{\circ}C$ ; **bold** values designate full temperature range.

| Symbol   | Description                               | Conditions   | Min                      | Typ            | Max   | Units  |
|--|---|--|--------------------------|----------------|---|--------|
| <b>V<sub>CC</sub> Output</b>                             |   |  |                          |                |   |        |
| I <sub>CC</sub> Hi-Z                                     | High Impedance Output Leakage Current     | Off Mode, V <sub>CC</sub> = 0V   |                          |                | <b>1</b>  | μA     |
| I <sub>CCSC</sub>  | Short-Circuit Current Limit               | V <sub>CC</sub> = V <sub>CCIN</sub> - 0.5V, On Mode V <sub>CC3</sub> or V <sub>CC5</sub> Selected, T <sub>A</sub> = 25°C   | 1.0                      |                | 2.5   | A      |
| R <sub>DS(ON)</sub>                                      | On Resistance                             | V <sub>CC</sub> = 3.0V, T <sub>A</sub> = 25°C<br>V <sub>CC</sub> = 5.0V, T <sub>A</sub> = 25°C   |                          | 85<br>80       | 110<br>100                                      | mΩ     |
| T <sub>crds</sub>  | Switch Resistance Temperature Coefficient |  |                          | 2800           |   | ppm/°C |
| <b>V<sub>CC</sub> Switching Time (Refer to Figure 1)</b> |   |  |                          |                |   |        |
| t1   | Output Turn-On Delay Time                 | V <sub>CC</sub> = 0V to 10% of 3.3V, R <sub>OUT</sub> = 10Ω  |                          | 500            | <b>2000</b>                                     | μs     |
| t2   | Output Turn-On Delay Time                 | V <sub>CC</sub> = 0V to 10% of 5.0V, R <sub>OUT</sub> = 10Ω  |                          | 500            | <b>1500</b>                                     |        |
| t3   | Output Rise Time                          | V <sub>CC</sub> = 10% to 90% of 3.3V, R <sub>LOAD</sub> = 10Ω  | <b>300</b>               | 1000           | <b>3000</b>                                     |        |
| t4   | Output Rise Time                          | V <sub>CC</sub> = 10% to 90% of 5.0V, R <sub>LOAD</sub> = 10Ω  | <b>300</b>               | 1000           | <b>3000</b>                                     |        |
| t5   | Output Turn-Off Delay Time                | V <sub>CC</sub> = 3.3V to 90% of 3.3V, R <sub>LOAD</sub> = 10Ω   |                          |                | <b>400</b>                                      |        |
| t6   | Output Turn-Off Delay Time                | V <sub>CC</sub> = 5.0V to 90% of 5.0V, R <sub>LOAD</sub> = 10Ω   |                          |                | <b>400</b>                                      |        |
| t7   | Output Fall Time to Off State             | V <sub>CC</sub> = 90% to 10% of 3.3V, R <sub>LOAD</sub> = 10Ω  |                          |                | <b>200</b>                                      |        |
| t8   | Output Fall Time to Off State             | V <sub>CC</sub> = 90% to 10% of 5.0V, R <sub>LOAD</sub> = 10Ω  |                          |                | <b>200</b>                                      |        |
| t9   | Output Fall Time to HiZ State             | V <sub>CC</sub> = 90% to 10% of 3.3V, R <sub>LOAD</sub> = 10Ω  |                          |                | <b>1500</b>                                     |        |
| t10  | Output Fall Time to HiZ State             | V <sub>CC</sub> = 90% to 10% of 5.0V, R <sub>LOAD</sub> = 10Ω  |                          |                | <b>2000</b>                                     |        |
| <b>Power Supply</b>                                      |   |  |                          |                |   |        |
| V <sub>CC3</sub>   | V <sub>CC3</sub> Operation Voltage        |  | 2.7                      |                | 5.5   | V      |
| V <sub>CC5</sub>   | V <sub>CC5</sub> Operation Voltage        |  | 2.7                      |                | 5.5   | V      |
| I <sub>CC3</sub>   | V <sub>CC3</sub> Supply Current           | V <sub>CC</sub> = 5V or HiZ or Off, V <sub>CC3</sub> < V <sub>CC5</sub> , I <sub>CC</sub> Out = 0<br>V <sub>CC</sub> = 3.3V, V <sub>CC3</sub> < V <sub>CC5</sub> , I <sub>CC</sub> Out = 0   |                          | 5              | <b>1</b><br><b>20</b>                           | μA     |
| I <sub>CC5</sub>   | V <sub>CC5</sub> Supply Current           | V <sub>CC</sub> = Off, V <sub>CC5</sub> > V <sub>CC3</sub> , I <sub>CC</sub> Out = 0<br>V <sub>CC</sub> = HiZ, V <sub>CC5</sub> > V <sub>CC3</sub> , I <sub>CC</sub> Out = 0<br>V <sub>CC</sub> = 3.3V, V <sub>CC5</sub> > V <sub>CC3</sub> , I <sub>CC</sub> Out = 0<br>V <sub>CC</sub> = 5V, V <sub>CC5</sub> > V <sub>CC3</sub> , I <sub>CC</sub> Out = 0 |                          | 10<br>10<br>15 | <b>1</b><br><b>40</b><br><b>40</b><br><b>40</b> | μA     |
| <b>Parallel Interface</b>                                |   |  |                          |                |   |        |
| V <sub>CTLLOW</sub>                                      | CTL Input Low Voltage                     |  |                          |                | <b>0.8</b>                                      | V      |
| V <sub>CTLHI</sub>                                       | CTL Input High Voltage                    | V <sub>CC3</sub> or V <sub>CC5</sub> = 2.7V to 3.6V<br>V <sub>CC3</sub> or V <sub>CC5</sub> = 4.5V to 5.5V   | <b>2.0</b><br><b>2.4</b> |                |   | V      |
| I <sub>SINKCTL</sub>                                     | CTL Input Leakage                         | V <sub>CTL</sub> = 5.5V  |                          | 0.01           | <b>1</b>  | μA     |
| V <sub>FAULTLOW</sub>                                    | FAULT Logic Output Low Voltage            | I <sub>SINK</sub> = 1mA  |                          |                | <b>0.4</b>                                      | V      |
| I <sub>SINKFAULT</sub>                                   | FAULT Logic Output High Leakage Current   | V <sub>FAULT</sub> = 5.5V  |                          | 0.05           | <b>1</b>  | μA     |
| <b>Other</b>   |   |  |                          |                |   |        |
| OTMP   | Over-Temperature Shutdown                 |  |                          | 125            |   | °C     |

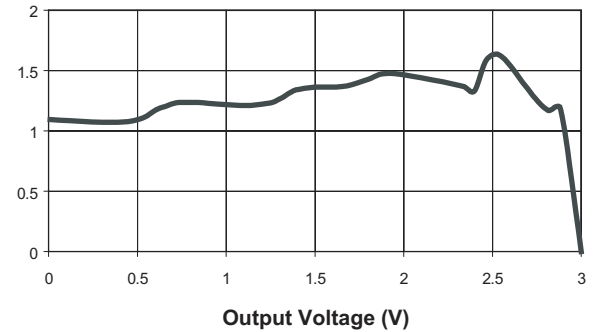
## Typical Characteristics

Unless otherwise noted,  $T_A = 25^\circ\text{C}$ .

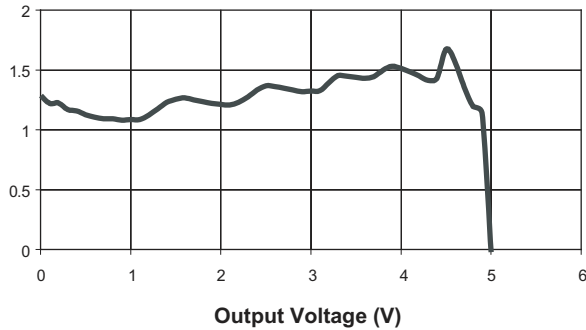
**Quiescent Current vs. Temperature**  
( $I_{CC5}$ )



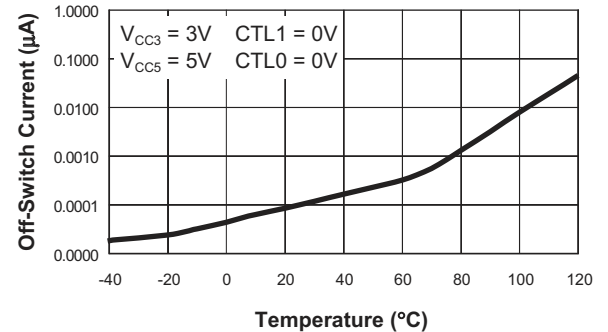
**Current Limit**  
( $V_{CC} = V_{CC3}$ )



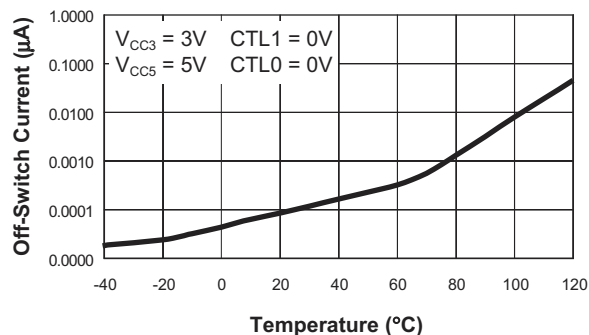
**Current Limit**  
( $V_{CC} = V_{CC5}$ )



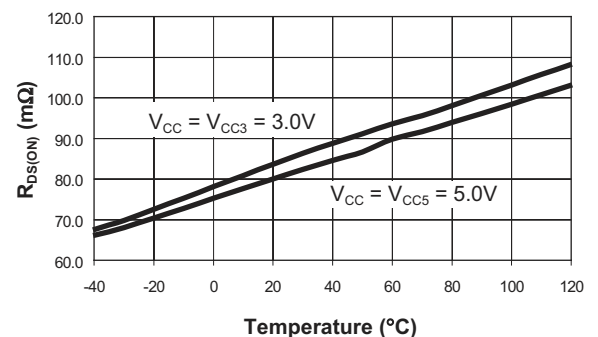
**Off-Switch Current vs. Temperature**  
( $I_{CC3}$ )



**Off-Switch Current vs. Temperature**  
( $I_{CC5}$ )



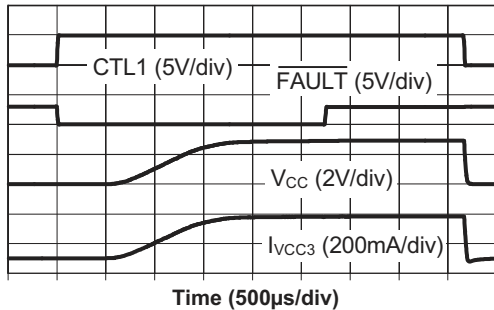
**$R_{DS(ON)}$  vs. Temperature**



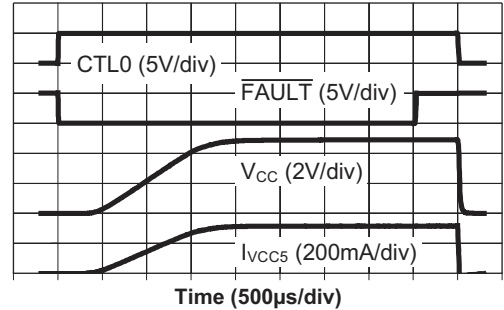
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Unless otherwise noted,  $T_A = 25^\circ\text{C}$ .

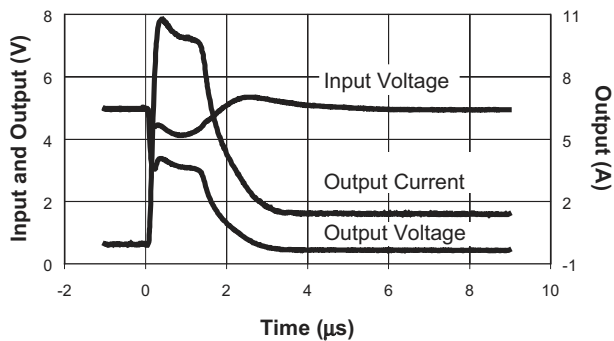
**Turn-On/Off Response**  
(10 $\Omega$ , 1 $\mu\text{F}$  Load)



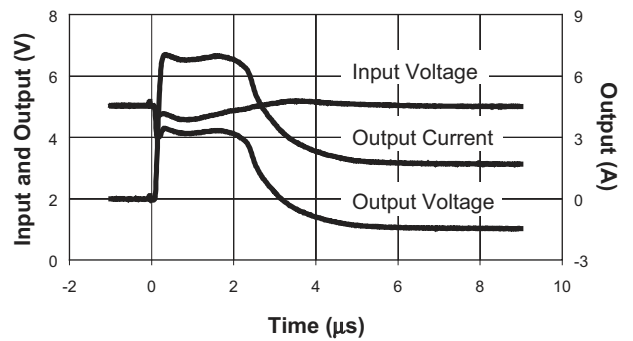
**Turn-On/Off Response**  
(15 $\Omega$ , 1 $\mu\text{F}$  Load)



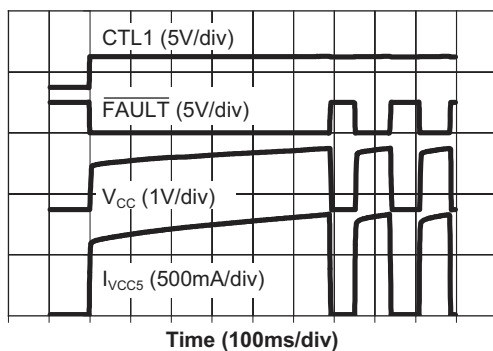
**Short Circuit Through 0.3 $\Omega$**



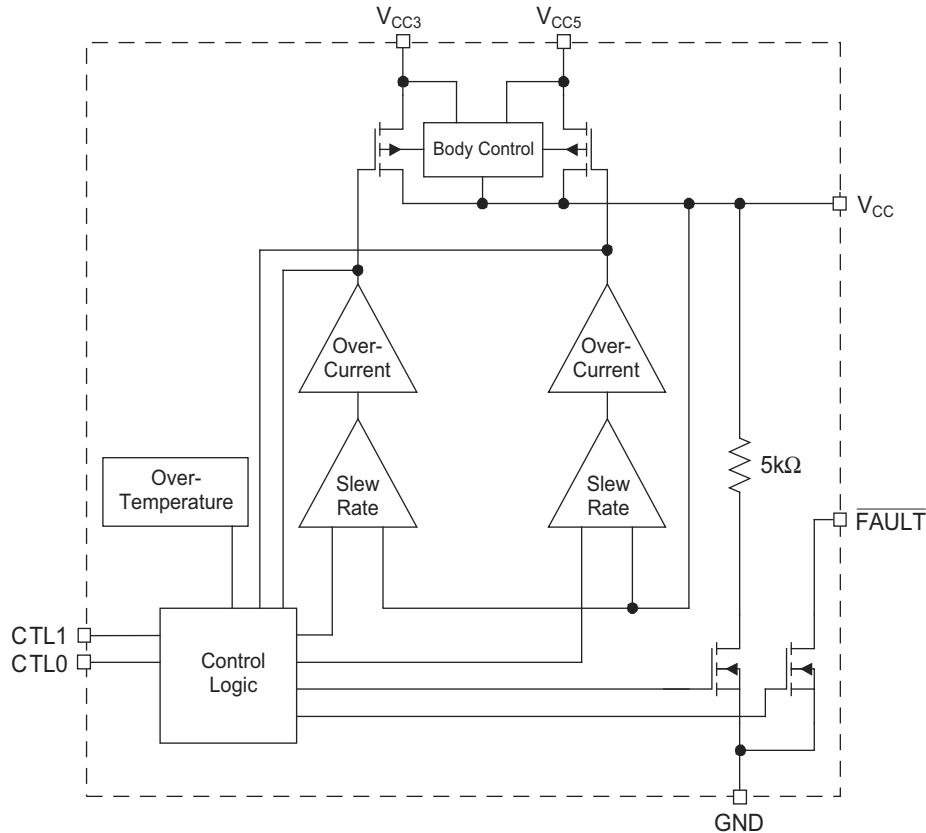
**Short Circuit Through 0.6 $\Omega$**



**Thermal Shutdown Response**



## Functional Block Diagram



## Functional Description

The AAT4650 is a single channel power switch that can be used in any application where dual power supply multiplexing is required. Typical applications include PC card applications not requiring a 12V power supply, or applications where power is switched, for example, between 5V for operation and 3.3V for standby mode. The AAT4650 operates with input voltages ranging from 2.7V to 5.5V in any combination and automatically powers its internal circuitry off of whichever input voltage is higher. Two identical low  $R_{DS(ON)}$  P-channel MOSFETs serve as the power multiplexing circuit with a common drain as the  $V_{CC}$  output and independent sources as the two  $V_{CC3}$  and  $V_{CC5}$  inputs. A 2-bit parallel interface determines the state of the multiplexer:  $V_{CC} = V_{CC3}$ ,  $V_{CC} = V_{CC5}$ ,  $V_{CC}$  with resistive pull down to ground, or  $V_{CC}$  high impedance. When the state is set to either of the two inputs, the multiplex-

ing circuit will slowly slew the  $V_{CC}$  output to the new voltage level which protects the upstream power supply from sudden load transients. When the resistive pull down is chosen for  $V_{CC}$ , the  $V_{CC}$  output is quickly discharged by the resistive pull down. The AAT4650 always serves as an electronic fuse by limiting the load current if it exceeds the current limit threshold. During power-up into a short, the current will gradually increase until the current limit is reached. During a sudden short circuit on the output, the current limit will respond in 1 $\mu$ s to isolate and protect the upstream power supply from the load short circuit. In most applications, because the response time is so fast, a short circuit to  $V_{CC}$  will not affect the upstream supply, so system functionality will not be affected. In the case of an over-current condition, an open drain  $\overline{FAULT}$  flag output will signal the event. The  $\overline{FAULT}$  output is also active during output voltage slew, and becomes inactive once the output is within regulation.

## Applications Information

### Input Capacitor

A 1μF or larger capacitor is typically recommended for C<sub>IN</sub>. A C<sub>IN</sub> capacitor is not required for basic operation; however, it is useful in preventing load transients from affecting up-stream circuits. C<sub>IN</sub> should be located as close to the device VIN pin as practically possible. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C<sub>IN</sub>. There is no specific capacitor equivalent series resistance (ESR) requirement for C<sub>IN</sub>. However, for higher current operation, ceramic capacitors are recommended for C<sub>IN</sub> due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

### Output Capacitor

A 0.1μF or greater capacitor is generally required between V<sub>CC</sub> and GND. Likewise, with the output capacitor, there is no specific capacitor ESR requirement. If desired, C<sub>OUT</sub> may be increased to accommodate any load transient condition.

### Parallel Interface / Break Before Make

A 2-bit parallel interface determines the state of the V<sub>CC</sub> output. The logic levels are compatible with CMOS or TTL logic. A logic low value must be less than 0.8V, and a logic high value must be greater than 2.4V. In cases where the interface pins rapidly change state directly from 3V to 5V (or vice versa), internal break-before-make circuitry prevents any back flow of current from one input power supply to the other. In addition, the body connections of the internal P-channel MOSFET switches are always set to the highest potential of V<sub>CC3</sub>, V<sub>CC5</sub>, or V<sub>CC</sub>, which prevents any body diode conduction, power supply backflow, or possible device damage.

### FAULT Output

The FAULT output is pulled to ground by an open drain N-channel MOSFET during an over-current or output slew condition. It should be pulled up to the reference power supply of the controller IC via a nominal 100kΩ resistor.

### Voltage Regulation

The PC card specification calls for a regulated 5V supply tolerance of ±5%. Of this, a typical power supply will drop less than 2% and the PCB traces will drop another

1%. This leaves 2% for the AAT4650 as the PC card switch. In the PC card application, the maximum allowable current for the AAT4650 is dominated by voltage regulation, rather than by thermal considerations, and is set by either the current limit or the maximum R<sub>DS(ON)</sub> of the P-channel MOSFET. The maximum R<sub>DS(ON)</sub> at 85°C is calculated by applying the R<sub>DS</sub> temperature coefficient to the maximum room temperature R<sub>DS(ON)</sub>:

$$R_{DS(ON)(MAX)} = R_{DS(ON)25} \cdot (1 + [TC \cdot \Delta T])$$

-or-

$$R_{DS(ON)(MAX)} = 100m\Omega \cdot (1 + [0.0028 \cdot 60]) = 116.8m\Omega$$

The maximum current is equal to the 2% tolerance of the 5V supply (100mV) across the AAT4650 divided by R<sub>DS(ON)(MAX)</sub>. Or:

$$I_{MAX5} = \frac{100mV}{116.8m\Omega} = 856.2mA$$

For the 3.3V supply in the PC card application, the conditions are a bit relaxed, with the allowable voltage regulation drop equal to 300mV. With a 2% supply and 1% PCB trace regulation, the PC card switch can have a 200mV drop. So:

$$I_{MAX3} = \frac{200mV}{134m\Omega} = 1.5A$$

Since 1.5A is the nominal current limit value, the AAT4650 will current limit before I<sub>MAX3</sub> is reached.

Thermal issues are not a problem in the SOP-8 package since θ<sub>JA</sub>, the package thermal resistance, is only 120°C/W. At any given ambient temperature (T<sub>A</sub>) the maximum package power dissipation can be determined by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Constants for the AAT4650 are maximum junction temperature, T<sub>J(MAX)</sub> = 125°C, and package thermal resistance, θ<sub>JA</sub> = 120°C/W. Worst case conditions are calculated at the maximum operating temperature where T<sub>A</sub> = 85°C. Typical conditions are calculated under normal ambient conditions where T<sub>A</sub> = 25°C. At T<sub>A</sub> = 85°C, P<sub>D(MAX)</sub> = 333mW. At T<sub>A</sub> = 25°C, P<sub>D(MAX)</sub> = 833mW.

Maximum current is given by the following equation:

$$I_{OUT(MAX)} = \sqrt{\frac{P_{D(MAX)}}{R_{DS(ON)}}}$$



For the AAT4650 at 85°C,  $I_{OUT(MAX)} = 1.65A$ , a value greater than the internal minimum current limit specification.

### **Over-Current and Over-Temperature Protection**

Because many AAT4650 applications provide power to external devices, it is designed to protect its host device from malfunctions in those peripherals through slew rate control, current limiting, and thermal limiting. The AAT4650 current limit and thermal limit serve as an immediate and reliable electronic fuse without any increase in  $R_{DS(ON)}$  for this function. Other solutions, such as a poly fuse, do not protect the host power supply and system from mishandling or short circuiting peripherals; they will only prevent a fire. The AAT4650 high-speed current limit and thermal limit not only prevent fires, they also isolate the power supply and entire system from any activity at the external port and report a mishap by means of a  $\overline{FAULT}$  signal.

Over-current and over-temperature go hand in hand. Once an over-current condition exists, the current supplied to the load by the AAT4650 is limited to the over-current threshold. This results in a voltage drop across the AAT4650 which causes excess power dissipation and a package temperature increase. As the die begins to heat up, the over-temperature circuit is activated. If the temperature reaches the maximum level, the AAT4650 automatically switches off the P-channel MOSFETs. While they are off, the over-temperature circuit remains active. Once the temperature has cooled by approximately 10°C, the P-channel MOSFETs are switched back on. In this manner, the AAT4650 is thermally cycled on and off until the short circuit is removed. Once the short is removed, normal operation automatically resumes.

To save power, the full high-speed over-current circuit is not activated until a lower threshold of current (approximately 500mA) is exceeded in the power device. When the load current exceeds this crude threshold, the AAT4650 quiescent current increases from 15µA to 200µA. The high-speed over-current circuit works by linearly limiting the current when the current limit is reached. As the voltage begins to drop on  $V_{CC}$  due to current limiting, the current limit magnitude varies and generally decreases as the  $V_{CC}$  voltage drops to 0V.

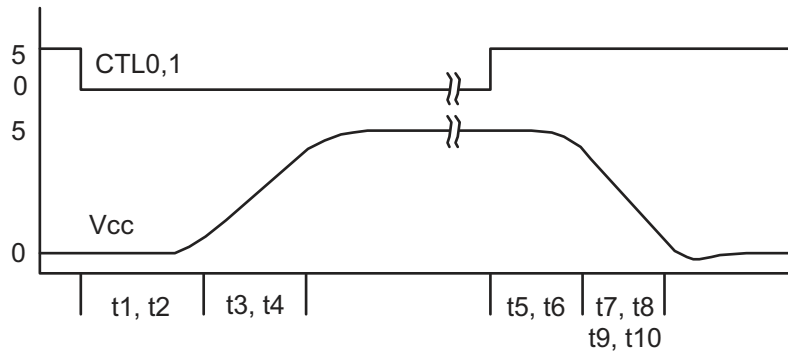
### **Switching $V_{CC}$ Voltage**

The AAT4650 meets PC card standards for switching the  $V_{CC}$  output by providing a ground path for  $V_{CC}$ , as well as a high impedance state. The PC card protocol for determining low voltage operations is to first power the peripheral with 5V and poll for 3.3V operation. When transitioning from 5V to 3.3V,  $V_{CC}$  must be discharged to less than 0.8V to provide a hard reset. The resistive ground state ( $CTL1 = 0$ ,  $CTL0 = 0$ ) will accommodate this. The ground state will also guarantee the  $V_{CC}$  voltage to be discharged within the specified amount of time (100ms).

### **Printed Circuit Board Layout Recommendations**

For proper thermal management, to minimize PCB trace resistance, and to take advantage of the low  $R_{DS(ON)}$  of the AAT4650, a few circuit board layout rules should be followed:  $V_{CC3}$ ,  $V_{CC5}$ , and  $V_{CC}$  should be routed using wider than normal traces; the two  $V_{CC}$  pins (Pins 6 and 7) should be connected to the same wide PCB trace; and GND should be connected to a ground plane. For best performance,  $C_{IN}$  and  $C_{OUT}$  should be placed close to the package pins.

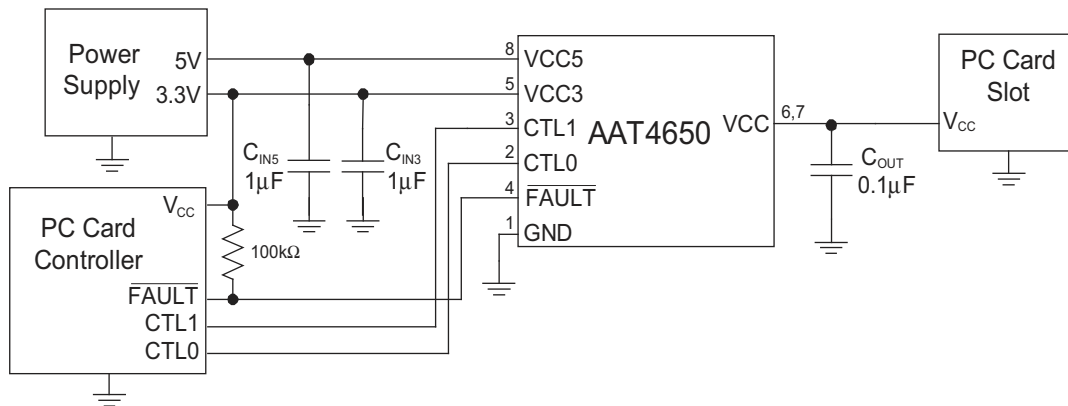
## Timing Diagram



**Figure 1: V<sub>CC</sub> Switching Time Diagram.**

Refer to V<sub>CC</sub> Switching Time specifications in the Electrical Characteristics section for definitions of t1 to t10.

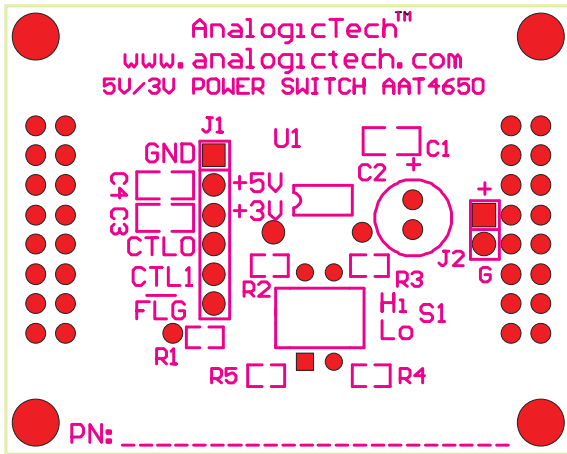
## Typical PC Card Application Circuit



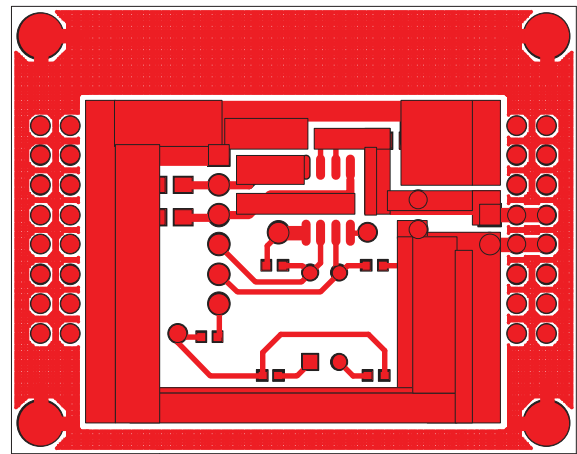
## Evaluation Board Layout

The AAT4650 evaluation board layout follows the printed circuit board layout recommendations and can be used for good applications layout.

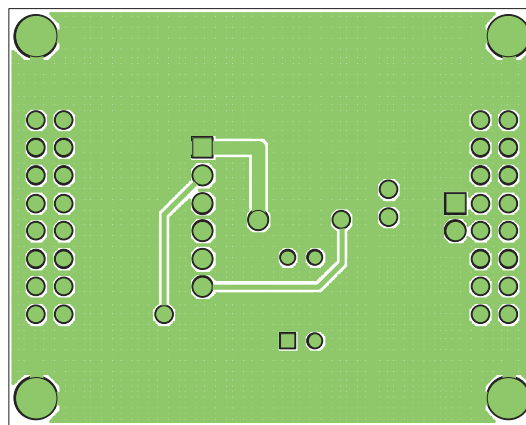
Note: Board layout shown is not to scale.



**Figure 2: Evaluation Board Top Side Silk Screen Layout / Assembly Drawing.**



**Figure 3: Evaluation Board Component Side Layout.**



**Figure 4: Evaluation Board Solder Side Layout.**

## Ordering Information

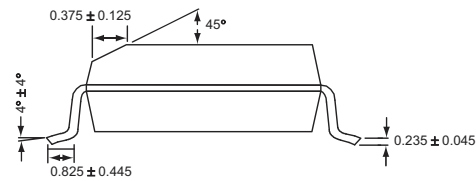
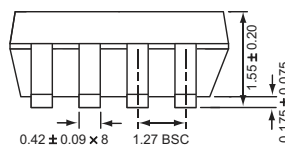
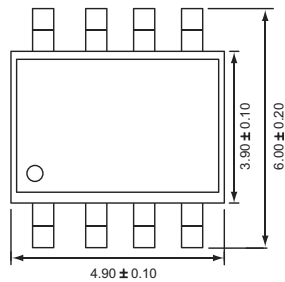
| Package | Marking | Part Number (Tape and Reel) <sup>1</sup> |
|---------|---------|--|
| SOP-8   | 4650    | <b>AAT4650IAS-T1</b>                     |
| TSSOP-8 | 4650    | <b>AAT4650IHS-T1</b>                     |



All AnalogicTech products are offered in Pb-free packaging. The term “Pb-free” means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at <http://www.analogictech.com/aboutus/quality.php>.

## Package Information

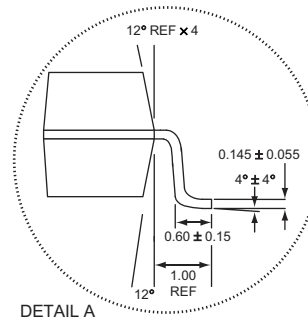
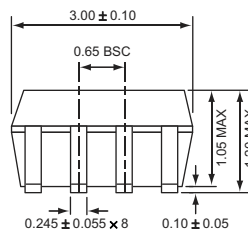
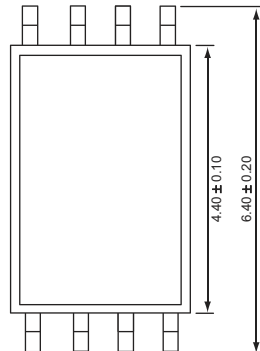
### SOP-8



All dimensions in millimeters.

1. Sample stock is generally held on all part numbers listed in **BOLD**.

**TSSOP-8**



All dimensions in millimeters.

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