AAT2688

SystemPower™ 4.5A PMIC Solution for 12V Adapter Systems with 2-Output High Performance Step-Down Converters

General Description

The AAT2688 provides two independently regulated DC outputs: a high voltage synchronous step-down (Buck) regulator and a low input voltage step-down low dropout (LDO) regulator. The PMIC is optimized for low cost 12V adapter inputs, making the device the ideal system-on-a-chip power solution for consumer communications equipment.

Channel 1 is a step-down regulator with an input voltage range of 6.0V to 24V, providing up to 4.5A output current. 490kHz fixed switching frequency allows small L/C filtering components. Channel 1 utilizes voltage mode control configured for optimum performance across the entire output voltage and load range.

Channel 2 is a low-dropout (LDO) regulator providing up to 600mA output current. The device provides low output noise, low quiescent current, and excellent transient response.

The step-down regulator includes integrated over-current, soft-start and over-temperature protection. Independent input and enable pins provide maximum design flexibility.

The AAT2688 is available in the Pb-free 4mm x 5mm 24-pin TQFN package. The rated operating temperature range is -40°C to 85°C.

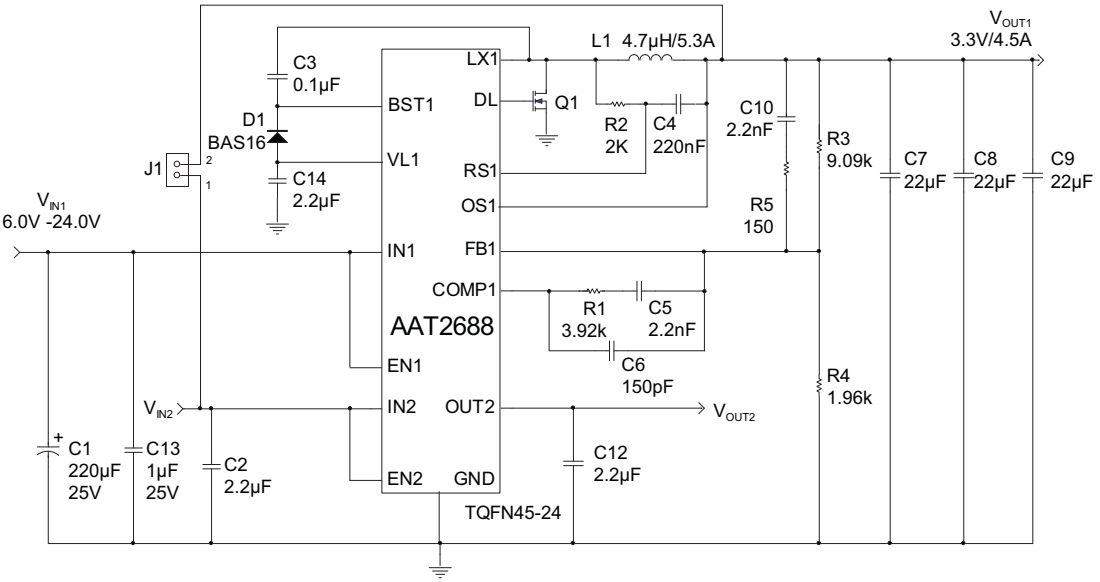
Features

- 2-Output Step-Down Converters:
- Channel 1 (Buck): V_{IN1} = 6.0 to 24.0V
  - V_{OUT1} Adjustable from 0.8V to 5.5V
  - I_{OUT1} up to 4.5A
  - High Switching Frequency
  - Voltage Mode Control
  - High Accuracy ±1.5%
  - PWM Fixed Frequency for Low Ripple
- Channel 2 (LDO): V_{IN2} = 2.7V to 5.5V
  - I_{OUT2} up to 600mA
  - 1V Dropout Voltage at 600mA I_{OUT}
- Small Solution Size
- System on a Chip
- Ultra-small External L/C
- Shutdown Current <35µA
- Independent Enable Pins
- Over-Current and Over-Temperature Protection
- Internal Soft Start
- 4x5mm 24-Pin TQFN Low Profile Package
- -40°C to 85°C Temperature Range

Applications

- DSL and Cable Modems
- Notebook Computers
- Satellite Set-top Boxes
- Wireless LAN Systems

Typical Application

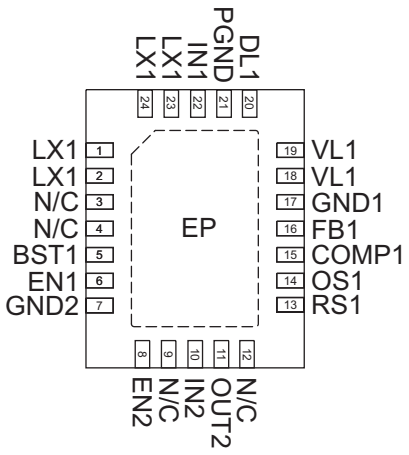


Pin Descriptions

Pin #	Symbol	Function
1, 2, 23, 24	LX1	Channel 1 step-down (Buck) converter switching pin. Connect output inductor to this pin. Connect both LX1 pins together.
3, 4, 9, 12	N/C	No connect. For optional routing reasons, pins 3 and 4 can be connected to V_{IN}, pin 9 to pin 10 (IN2), and pin 12 to pin 11 (OUT2).
5	BST1	Channel 1 step-down regulator boost drive input pin. Connect the cathode of fast rectifier from this pin and connect a 100nF capacitor from this pin to the channel 1 switching node (LX1) for internal hi-side MOSFET gate drive.
6	EN1	Channel 1 step-down regulator enable input pin. Active high enables internal linear regulator and channel 1 output.
7	GND2	Ground pin for Channel 2. Power return pin for channel 2. Connect return of channel 2 input and output capacitors close to this pin for best noise performance.
8	EN2	Channel 2 low dropout (LDO) enable input pin. Active high.
10	IN2	Input supply voltage pin for channel 2 linear low dropout (LDO) regulator. Connect 2.2µF ceramic input capacitor close to this pin.
11	OUT2	Output of channel 2 of linear low dropout (LDO) regulator. Connect a 2.2µF ceramic capacitor from this pin to GND pin.
13	RS1	Channel 1 output current sense pin. Connect a small signal resistor from this pin to switching node (LX1) to enable over-current sense for step-down converter. The current limit threshold varies with sense resistor sizing.
14	OS1	Channel 1 output sense voltage pin. Connect to the output capacitor to enable over-current sense for step-down converter.
15	COMP1	Compensation pin for channel 1 step-down regulator. Connect a series resistor, capacitor network to compensate the voltage mode control loop.
16	FB1	Feedback input pin for channel 1 step-down converter. Connect an external resistor divider to this pin to program the output voltage to the desired value.
17	GND1	Ground pin for channel 1. Power return pin for channel 1. Connect return of channel 1 input and output capacitors close to this pin for best noise performance.
18, 19	VL1	Internal linear regulator. Connect a 2.2µF capacitor from this pin to GND pin.
20	DL1	Channel 1 gate drive for low side MOSFET. Connect to the gate pin of an external N type MOSFET (see the "MOSFET Selection" section of this product datasheet).
21	PGND	Ground pin for both channels. Power return pin for both channels. Connect returns of both channels' input and output capacitors close to this pin for best noise performance.
22	IN1	Input supply voltage pin for channel 1 step-down regulator. Connect both IN1 pins together. Connect the input capacitor close to this pin for best noise performance.
EP	EP	Exposed Paddle. Tie to IN1. Connect to PCB heatsink for optimum thermal performance.

Pin Configuration

TQFN45-24
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
$V_{IN(HI)}$	IN1, EN1, LX1 to GND	-0.3 to 30.0	V
$V_{IN(LO)}$	IN2, VL1 to GND	-0.3 to 6.0	V
$V_{BST1-LX1}$	BST1 to LX1	-0.3 to 6.0	V
$V_{CONTROL}$	FB1, COMP1, RS1, OS1, OUT2, DL1 to GND	-0.3 to $V_{IN(LO)}$ + 0.3	V
V_{EN2}	EN2 to GND	-0.3 to V_{IN2} + 0.3	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation[2]	3.0	W
Θ_{JA}	Thermal Resistance[3]	33	°C/W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board with exposed paddle connected to ground plane.
3. Derate 30mW/°C above 25°C ambient temperature.

Electrical Characteristics[1]

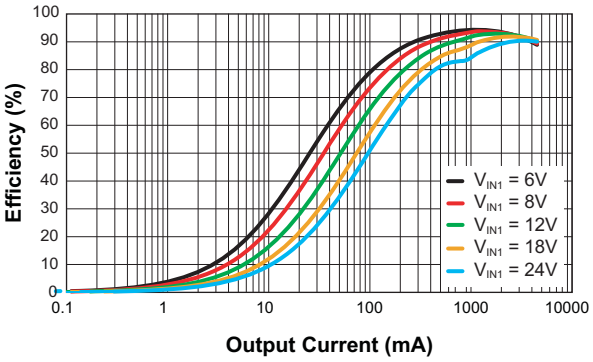
V_{IN1} = 12.0V, V_{IN2} =3.3V; T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions		Min	Typ	Max	Units
Channel 1: 4.5A Step-Down (Buck) Converter							
V_{IN1}	Input Voltage			6.0		24.0	V
V_{UVLO1}	UVLO Threshold	V_{IN1} Rising				5.0	V
		V_{IN1} Hysteresis			300		mV
		V_{IN1} Falling		3.0			V
V_{OUT1}	Output Voltage Range			0.8		5.5	V
V_{FB1}	Feedback Pin Voltage			0.576	0.585	0.594	V
V_{OUT}	Output Voltage Accuracy	I_{OUT1} = 0 to 4.5A		-3.0		+3.0	%
$(\Delta V_{OUT}/V_{OUT})/\Delta V_{IN}$	Line Regulation	V_{IN1} = 6V to 24V, V_{OUT1} = 3.3V, I_{OUT1} = 4.5A			0.05		%/V
$(\Delta V_{OUT}/V_{OUT})/\Delta I_{OUT}$	Load Regulation	V_{IN1} = 12V, V_{OUT1} = 3.3V, I_{OUT1} = 0A to 4.5A			0.2		%/A
I_{Q1}	Quiescent Current	V_{EN1} = Low, No load, V_{FB1} = 1.2V			600		µA
I_{SHDN1}	Shutdown Current	V_{EN1} = High, V_{L1} = 0V				35	µA
V_{OCP1}	Over-Current Offset Voltage	V_{EN1} = Low, V_{IN1} = 6.0V to 24.0V, T_A = 25°C		80	100	120	mV
I_{LX1}	LX1 Pin Leakage Current	V_{IN1} = 24.0V, V_{EN1} = 5.0V		-1.0		1.0	µA
D_{MAX}	Maximum Duty Cycle				85		%
R_{DL1}	Low Side Drive Source Resistance	Pull-Up, V_{L1} = 4.5V			5.0		Ω
		Pull-Down, V_{L1} = 4.5V			1.7		
$R_{DSON(H)}$	Hi Side On-Resistance	V_{L1} = 4.5V			35		mΩ
F_{OSC1}	Oscillator Frequency			350	490	650	kHz
$F_{FOLDBACK1}$	Short Circuit Foldback Frequency	Current Limit Triggered			100		kHz
t_{S1}	Start-Up Time	From Enable Channel 1 to Output Regulation			2.5		ms
Channel 2: 600mA Low Dropout (LDO) Regulator							
V_{IN2}	Input Voltage			2.7		5.5	V
V_{DO2}	Dropout Voltage	98% · $V_{OUT2(NOM)}$, I_{OUT2} = 600mA			1000	1300	mV
I_{Q2}	Quiescent (Ground) Current	No load			70	125	µA
I_{SHDN2}	Shutdown Current	V_{EN2} = GND				1.0	µA
$V_{OUT2(TOL)}$	Output Voltage Tolerance	I_{OUT2}= 1mA to 600mA, V_{IN2} = 2.7 to 5.5V, T_A = 25°C		-2.0		+2.0	%
		I_{OUT2}= 1mA to 600mA, V_{IN2} = 2.7 to 5.5V, T_A = -40°C to 85°C		-3.5		+3.5	%
e_N	Output Noise	BW = 300Hz to 50kHz			250		μV_{RMS}
PSRR	Power Supply Rejection Ratio	I_{OUT2} = 10mA	1kHz		67		dB
			10kHz		47		
			1MHz		45		
I_{LIMIT2}	Current Limit			700	800		mA
t_{S2}	Enable Start-Up Delay	From Enable Channel 2 to Output Regulation			15		µs
Over-Temperature, EN Logic							
$T_{SD1,2}$	Over-Temperature Shutdown Threshold				135		°C
	Over-Temperature Shutdown Hysteresis				15		°C
$V_{EN1,EN2(L)}$	Enable Threshold Low					0.6	V
$V_{EN1(H)}$	Enable Threshold High			2.5			V
$V_{EN2(H)}$				1.4			
$I_{EN1,EN2}$	Input Low Current			-1.0		1.0	µA

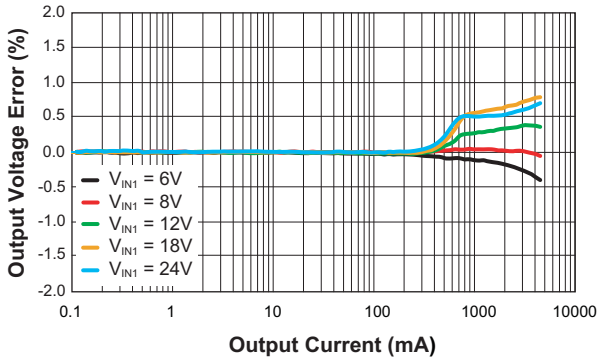
1. The AAT2688 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range and is assured by design, characterization and correlation with statistical process controls.

Typical Characteristics–Channel 1

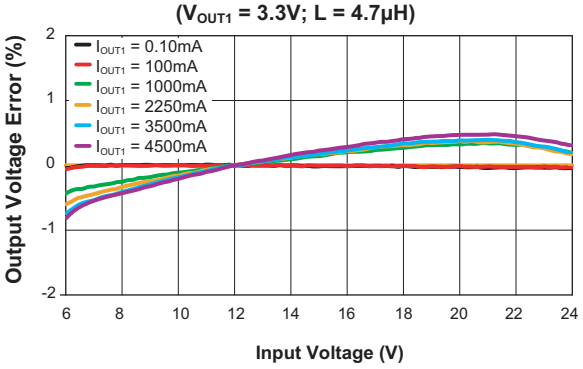
Step-Down Converter Efficiency vs. Output Current
(V_{OUT1} = 3.3V; L = 4.7µH)



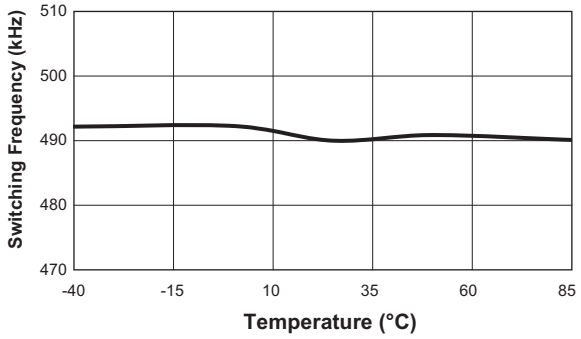
Step-Down Converter DC Regulation
(V_{OUT1} = 3.3V; L = 4.7µH)



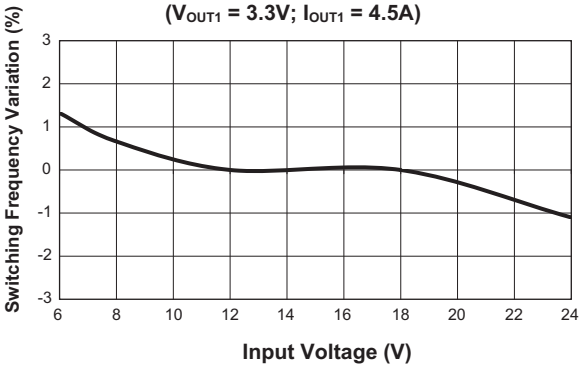
Step-Down Converter Output Voltage Error vs. Input Voltage
(V_{OUT1} = 3.3V; L = 4.7µH)



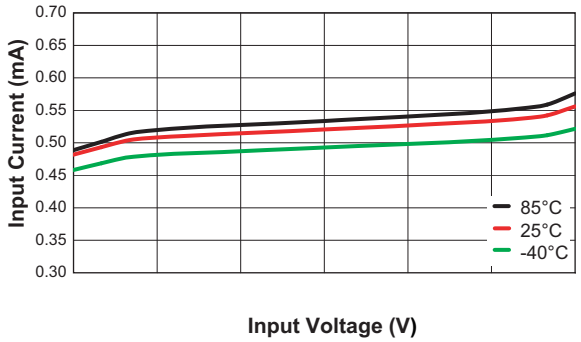
Step-Down Converter Switching Frequency vs. Temperature
(V_{IN1} = 12V; V_{OUT1} = 3.3V; I_{OUT1} = 4.5A)



Step-Down Converter Switching Frequency vs. Input Voltage
(V_{OUT1} = 3.3V; I_{OUT1} = 4.5A)

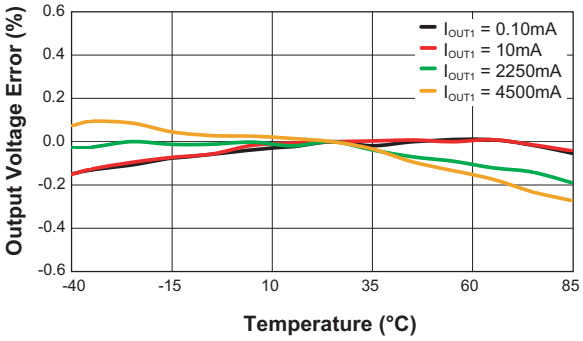


No Load Step-Down Converter Input Current vs. Input Voltage
(V_{EN1} = V_{IN1})

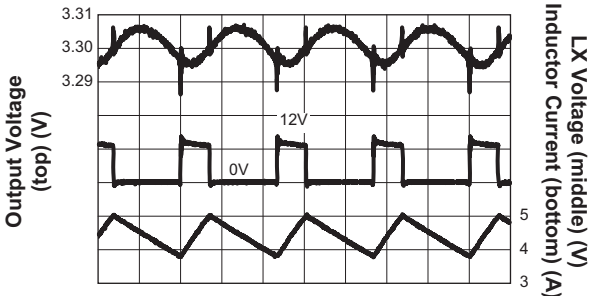


Typical Characteristics–Channel 1

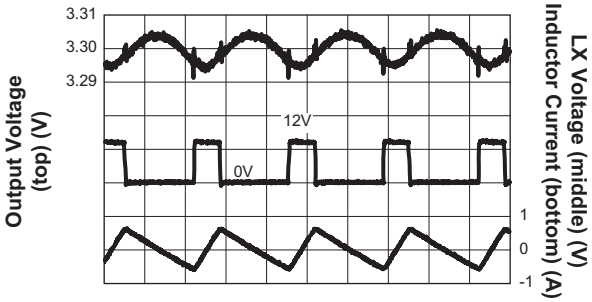
Step-Down Converter Output Voltage Error vs. Temperature
(V_{IN1} = 12V; V_{OUT1} = 3.3V)



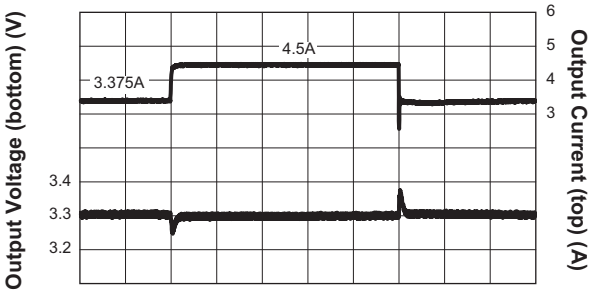
Step-Down Converter Output Ripple
(V_{IN1} = 12V; V_{OUT1} = 3.3V; I_{OUT1} = 4.5A)



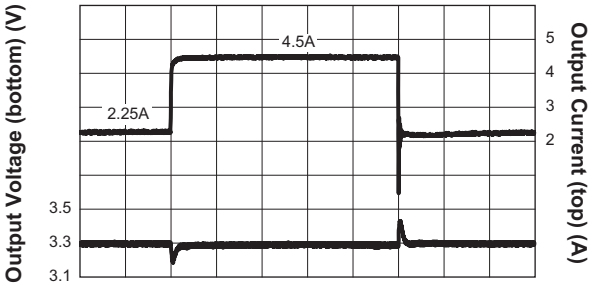
Step-Down Converter Output Ripple
(V_{IN1} = 12V; V_{OUT1} = 3.3V; I_{OUT1} = 1mA)



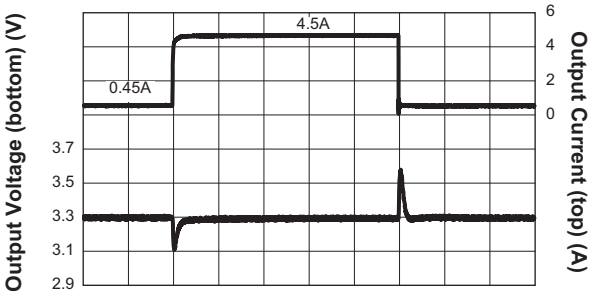
Step-Down Converter Load Transient Response
(I_{OUT1} = 3.375A to 4.5A; V_{IN1} = 12V; C_{OUT1} = 3x22µF)



Step-Down Converter Load Transient Response
(I_{OUT1} = 2.25 to 4.5A; V_{IN1} = 12V; C_{OUT1} = 3x22µF)

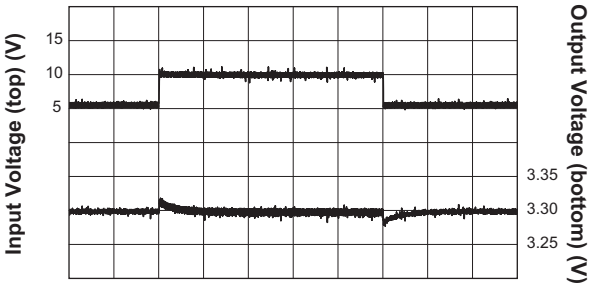


Step-Down Converter Load Transient Response
(I_{OUT1} = 0.45A to 4.5A; V_{IN1} = 12V; C_{OUT1} = 3x22µF)

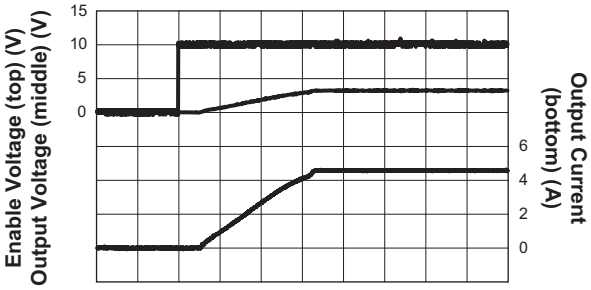


Typical Characteristics–Channel 1

Step-Down Converter Line Transient Response
(V_{IN1} = 6V to 10V; V_{OUT1} = 3.3V; I_{OUT1} = 4.5A)

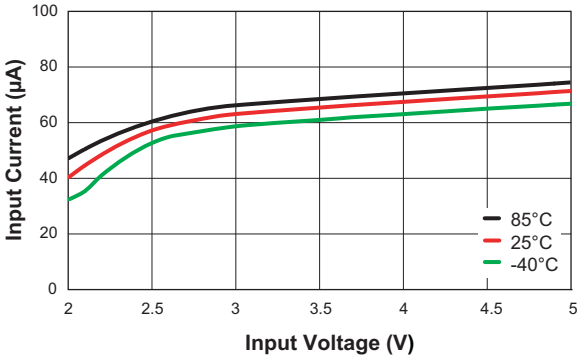


Step-Down Converter Soft Start
(V_{IN1} = 12V; V_{OUT1} = 3.3V; I_{OUT1} = 4.5A)

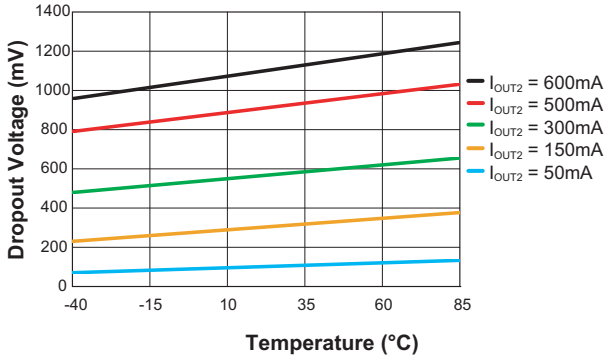


Typical Characteristics–Channel 2

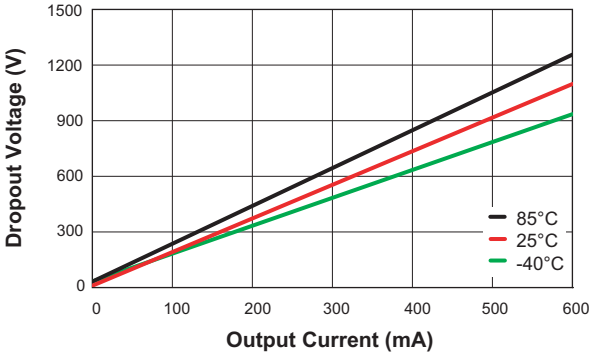
LDO Input Current vs. Input Voltage
(V_{EN1} = 0V; V_{EN2} = V_{IN2})



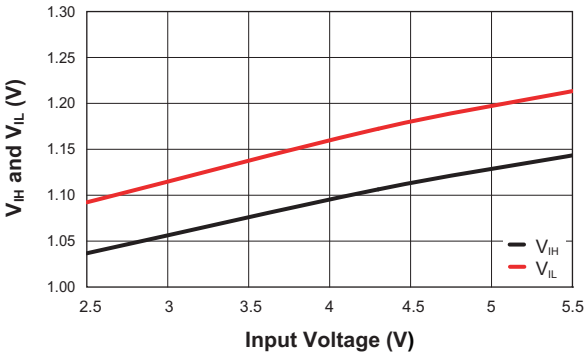
LDO Dropout Voltage vs. Temperature



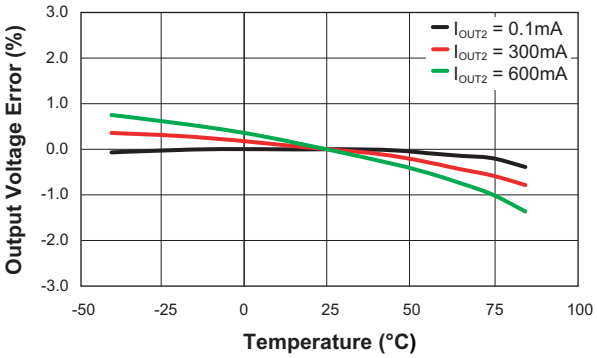
LDO Dropout Voltage vs. Output Current



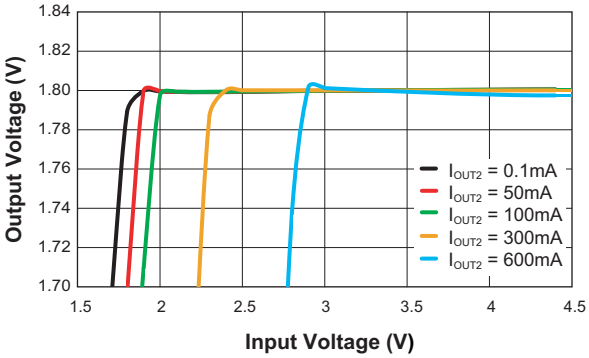
LDO V_{IH} and V_{IL} vs. Input Voltage



LDO Output Voltage Error vs. Temperature
(V_{IN2} = 3.3V; V_{OUT2} = 1.8V; I_{OUT2} = 600mA)

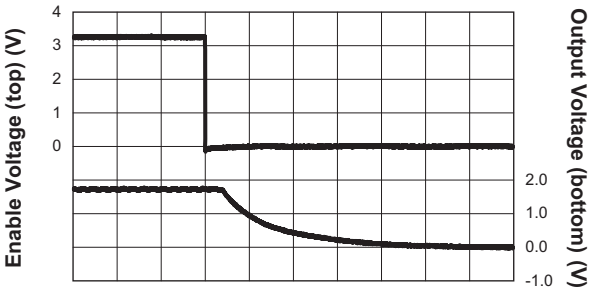


LDO Dropout Characteristics
(V_{OUT2} = 1.8V)



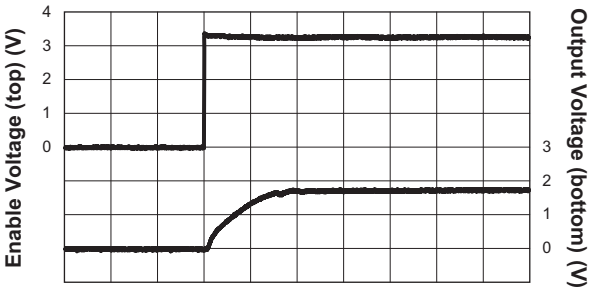
Typical Characteristics–Channel 2

LDO Turn-Off Response Time
(V_{IN2} = 3.3V; V_{EN2} = 3.3V; V_{OUT2} = 1.8V; I_{OUT2} = 600mA)



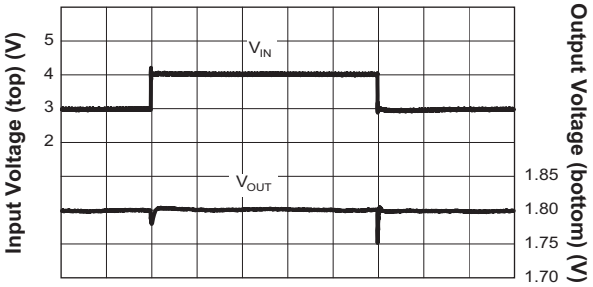
Time (5µs/div)

LDO Turn-On Time from Enable
(V_{IN2} = 3.3V; V_{EN2} = 3.3V; V_{OUT2} = 1.8V; I_{OUT2} = 600mA)



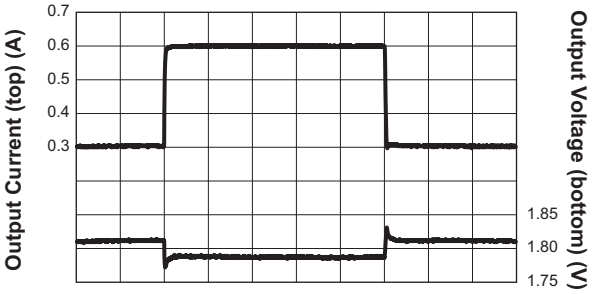
Time (5µs/div)

LDO Line Transient Response
(V_{IN2} = 3V to 4V; V_{OUT2} = 1.8V; I_{OUT2} = 600mA; C_{OUT2} = 2.2µF)



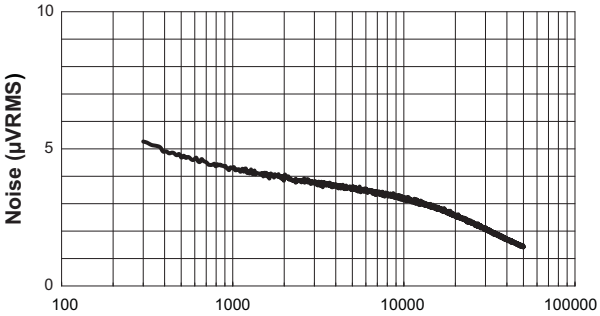
Time (200µs/div)

LDO Load Transient Response
(I_{OUT2} = 0.3 to 0.6A; V_{IN2} = 3.3V; V_{OUT2} = 1.8V; C_{OUT2} = 2.2µF)

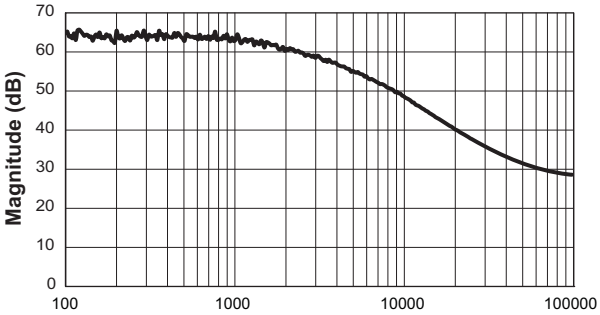


Time (40µs/div)

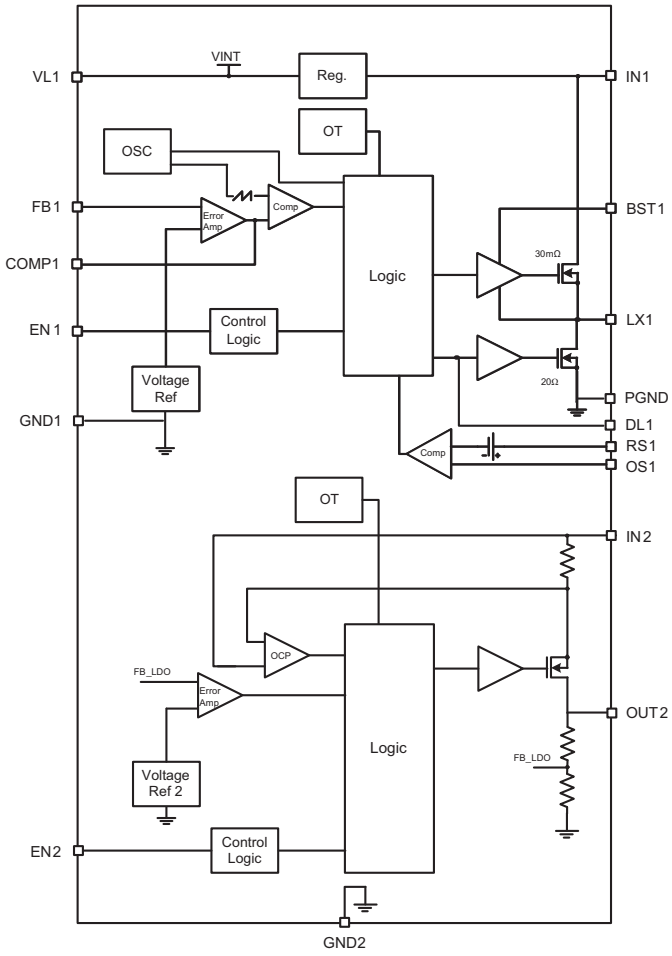
LDO Output Voltage Noise
(I_{OUT2} = 10mA; Power BW: 300~50KHz)



LDO Power Supply Rejection Ratio, PSRR
(I_{OUT2} = 10mA; BW: 100KHz to 300KHz)



Functional Block Diagram



Functional Description

The AAT2688 provides two independently regulated DC outputs; consisting of a high voltage synchronous step-down (Buck) regulator and a low input voltage linear low dropout (LDO) regulator. The PMIC is optimized for low cost 12V adapter inputs, making the device the ideal system-on-a-chip power solution for consumer communications equipment.

Channel 1 is a step-down (Buck) regulator with an input voltage range 6.0 to 24V; providing up to 4.5A output current. 490kHz fixed switching frequency allows small L/C filtering components.

Channel 1 utilizes voltage mode control configured for optimum performance across the entire output voltage and load range. The regulator includes integrated over-current, soft-start and over-temperature protection. Over-current is sensed through the output inductor DC winding resistance. An external resistor network adjusts the current limit according to the DC winding resistance of the desired inductor and the desired output current limit. Frequency reduction limits over-current stresses during short-circuit events. The operating frequency returns to the nominal setting when over-current conditions are removed.

Channel 2 is a low-dropout (LDO) regulator providing up to 600mA output current at a factory set output voltage. The device provides low output noise, low quiescent current, and excellent transient response.

The regulators include integrated over-current, soft-start and over-temperature protection. Independent input and enable pins provide maximum design flexibility.

The AAT2688 is available in the Pb-free 4x5 mm 24-pin TQFN package. The rated operating temperature range is -40°C to 85°C.

Applications Information

Output 1 is a high voltage DC/DC step-down converter providing an output voltage from 0.8V to 5.5V. The integrated high-side N-channel MOSFET device provides up to 4.5A output current. Input voltage range is 6.0V to 24.0V. The step-down converter utilizes constant frequency (PWM-mode) voltage mode control to achieve high operating efficiency while maintaining extremely low output noise across the operating range. High 490kHz (nominal) switching frequency allows small external filtering components, achieving minimum cost and solution size. External compensation and an optional feed forward capacitor allows the designer to optimize the transient response while achieving stability across the operating range.

Output 2 is a low voltage low dropout (LDO) linear regulator providing 1.8V with up to 600mA output current. The input voltage range is 2.7V to 5.5V. The LDO provides very low noise output which can be derived directly from Output 1.

Output Voltage—Channel 1[1]

The output voltage is set using an external resistor divider as shown in Table 1. Minimum output voltage is 0.8V and maximum output voltage is 5.5V. Typical maximum duty cycle is 85%. Example: with R4 = 1.96KΩ,

$$R3 = \frac{(V_{OUT} - 0.585) \cdot R4}{0.585}$$

V_{OUT}[1] (V)	R3 (kΩ)
0.8	0.715
1.0	1.37
1.2	2.05
1.5	3.09
1.8	4.02
2.0	4.75
2.5	6.49
3.0	8.06
3.3	9.09
5.0	14.7

Table 1: External Resistor Values (Standard 1% Resistors are Substituted for Calculated Values).

Channel 1 Regulator Output Capacitor Selection

Three 22µF ceramic output capacitors are required to filter the inductor current ripple and supply the load transient current for I_{OUT} = 4.5A. The 1206 package with 10V minimum voltage rating is recommended for the output capacitors to maintain a minimum capacitance drop with DC bias.

Channel 1 Output Inductor Selection

The step-down converter utilizes constant frequency (PWM-mode) voltage mode control. A 4.7µH inductor value is selected to maintain the desired output current ripple and minimize the converter's response time to load transients. The peak switch current should not exceed the inductor saturation current or the MOSFETs.

Channel 1 MOSFET Selection

The step-down (buck) converter utilizes synchronous rectification (Q1) for constant frequency (PWM mode) voltage mode control. The synchronous rectifier is selected based on the desired $R_{DS(ON)}$ value and Q_G (total gate charge), these two critical parameters are weighed against each other. To get a low $R_{DS(ON)}$ value, the MOSFET must be of a very large size and a larger MOSFET will have a large Q_G. Conversely to get a low Q_G, the MOSFET must be small and thus have a large $R_{DS(ON)}$ value. In addition to the trade off between $R_{DS(ON)}$ and Q_G, the maximum voltage rating for the external synchronous MOSFET must exceed the maximum application input voltage value ($V_{DS[MAX]} > V_{IN[MAX]}$).

The Q_G affects the turn-on/turn-off time of the synchronous MOSFET, the longer the turn-on/turn-off time the more likely the step-down converter will have "shoot through" current issues. "Shoot through" current occurs when the AAT2688 internal top-side MOSFET and the external synchronous MOSFET are conducting current at the same time. This will result in a low impedance path to ground from the input voltage through the two MOSFETs, and the current may exceed the maximum current rating of the AAT2688 and external synchronous MOSFET. Exceeding the maximum current ratings will lead to the destructive derating of the AAT2688 and external synchronous MOSFET.

1. The R3 and R4 feedback resistors are separate from the compensation network. When changing either R3 and/or R4, the compensation network will have to be altered. Contact the Applications Engineering department for compensation network recommendations for specific output voltages.

The critical parameter recommendations for the external synchronous minimum 25V MOSFET are as follows:

Q_G (Total Gate Charge) = 5nC to 15nC (max) (V_{GS}: 4.5V to 5V)

$R_{DS(ON)}$ = 10mΩ to 30mΩ (max) (V_{GS}: 4.5V to 5V)

Channel 1 Input Capacitor Selection

For low cost applications, a 220µF/25V electrolytic capacitor is selected to control the voltage overshoot across the high side MOSFET. A small ceramic capacitor with voltage rating at least 1.05 times greater than the maximum input voltage is connected as close as possible to the input pin (Pin 14) for high frequency decoupling.

Channel 1 Feedback and Compensation Networks

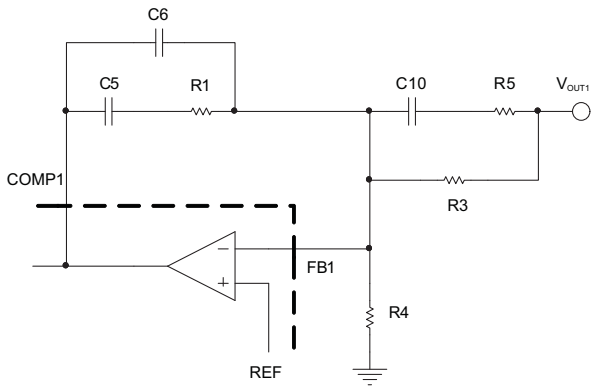


Figure 1: AAT2688 Feedback and Compensation Networks for Type III Voltage-Mode Control Loop.

The transfer function of the Error Amplifier is dominated by the DC Gain and the L C_{OUT} output filter of the regulator. This output filter and its equivalent series resistor (ESR) create a double pole at F_{LC} and a zero at F_{ESR} in the following equations:

$$\textbf{Eq. 1: } F_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}}$$

$$\textbf{Eq. 2: } F_{ESR} = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{OUT}}$$

The feedback and compensation networks provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin for system stability. Equation 3, 4, 5 and 6 relate the compensation network's poles and zeros to the components R1, R3, R5, C5, C6, and C10:

$$\textbf{Eq. 3: } F_{Z1} = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_5}$$

$$\textbf{Eq. 4: } F_{Z2} = \frac{1}{2 \cdot \pi \cdot (R_3 + R_5) \cdot C_{10}}$$

$$\textbf{Eq. 5: } F_{P1} = \frac{1}{2 \cdot \pi \cdot R_1 \cdot \left(\frac{C_5 \cdot C_6}{C_5 + C_6}\right)}$$

$$\textbf{Eq. 6: } F_{P2} = \frac{1}{2 \cdot \pi \cdot R_5 \cdot C_{10}}$$

Components of the feedback, feed forward, compensation, and current limit networks need to be adjusted to maintain the systems stability for different input and output voltage applications as shown in Table 2.

Network	Components	V_{OUT} =3.3V V_{IN}=6V-24V
Feedback	R4	1.96kΩ
	R3	9.09kΩ
Feed Forward	C10	2.2nF
	R5	150Ω
Compensation	C5	2.2nF
	C6	150pF
	R1	3.92kΩ
Current Limit	C4	220nF
	R2	2kΩ
	R6	Open
	R7	0
	R8	Open

Table 2: AAT2688 Feedback, Compensation, and Current Limit Components for V_{OUT} =3.3V.

Channel 1 Thermal Protection

The AAT2688 has an internal thermal protection circuit which will turn on when the device die temperature exceeds 135°C. The internal thermal protection circuit will actively turn off the high side regulator output device to prevent the possibility of over temperature damage. The Buck regulator output will remain in a shutdown state until the internal die temperature falls back below the 135°C trip point. The combination and interaction between the short circuit and thermal protection systems allows the Buck regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.

Over-Current Protection

The regulator provides true-load DC output current sensing which protects the load and limits component stresses. The output current is sensed through the DC resistance in the output inductor. The regulator reduces the operating frequency when an over-current condition is detected; limiting stresses and preventing inductor saturation. This allows the smallest possible inductor for the given application. A small resistor divider may be necessary to adjust the over-current threshold and compensate for variation in inductor DC resistance.

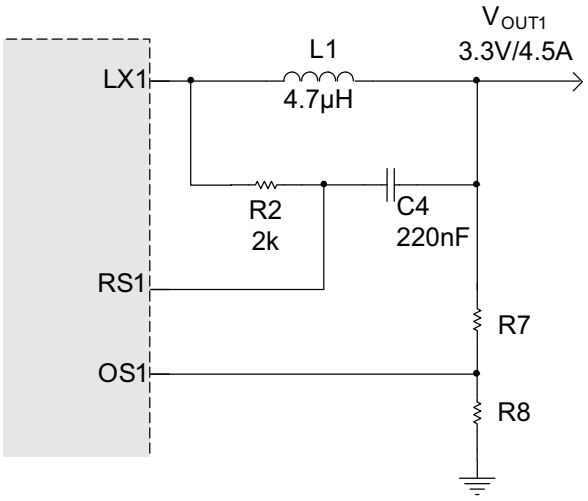


Figure 2: Resistor Network to Adjust the Current Limit Less than the Pre-Set Over-Current Threshold (Add R7, R8).

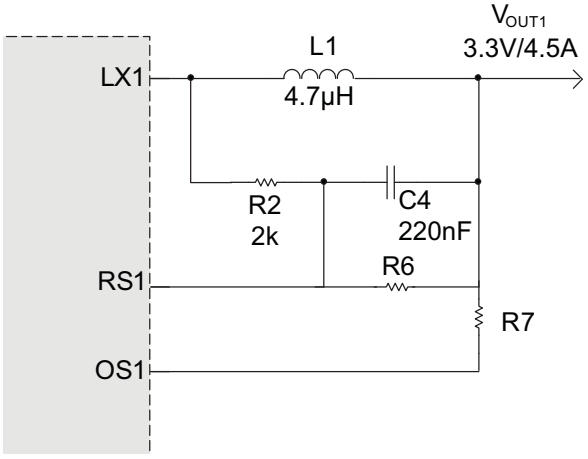


Figure 3: Resistor Network to Adjust the Current Limit Greater than the Pre-Set Over-Current Level (Add R6, R7).

Channel 2 Input Capacitor

Typically, a 1µF or larger capacitor is recommended for C_{IN} in most applications. A C_{IN} capacitor is not required for basic LDO regulator operation. However, if the AAT2688 is physically located more than three centimeters from an input power source, a C_{IN} capacitor will be needed for stable operation.

C_{IN} should be located as close to the device V_{IN} pin as possible. C_{IN} values greater than 1µF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor ESR requirement for C_{IN}. However, for 150mA LDO regulator output operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources, such as batteries in portable devices.

Channel 2 Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins VOUT and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be connected as close as possible for maximum device performance. The AAT2688 LDO has been specifically designed to function with very low ESR ceramic capacitors. For best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1µF to 10µF. Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection characteristics of the channel 2 should use 2.2µF or greater for C_{OUT}. If desired, C_{OUT} may be increased without limit. In low output current applications where output load is less than 10mA, the minimum value for C_{OUT} can be as low as 0.47µF.

Channel 2 Enable Function

The AAT2688 features an LDO regulator enable/disable function. This pin (EN) is active high and is compatible with CMOS logic. To assure the LDO regulator will switch on, the EN turn-on control level must be greater than 1.5V. The LDO regulator will go into the disable shutdown mode when the voltage on the EN pin falls below 0.6V. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state. When the LDO regulator is in shut-

down mode, an internal 1.5kΩ resistor is connected between V_{OUT} and GND. This is intended to discharge C_{OUT} when the LDO regulator is disabled. The internal 1.5kΩ has no adverse effect on device turn-on time.

Channel 2 Short-Circuit Protection

The AAT2688 LDO contains an internal short-circuit protection circuit that will trigger when the output load current exceeds the internal threshold limit. Under short-circuit conditions, the output of the LDO regulator will be current limited until the short-circuit condition is removed from the output or LDO regulator package power dissipation exceeds the device thermal limit.

Channel 2 Thermal Protection

The AAT2688 LDO has an internal thermal protection circuit which will turn on when the device die temperature exceeds 135°C. The internal thermal protection circuit will actively turn off the LDO regulator output pass device to prevent the possibility of over temperature damage. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back below the 135°C trip point. The combination and interaction between the short circuit and thermal protection systems allows the LDO regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.

Channel 2 No-Load Stability

The AAT2688 is designed to maintain output voltage regulation and stability under operational no load conditions. This is an important characteristic for applications where the output current may drop to zero.

Channel 2 Reverse Output-to-Input Voltage Conditions and Protection

Under normal operating conditions, a parasitic diode exists between the output and input of the LDO regulator. The input voltage should always remain greater than the output load voltage, maintaining a reverse bias on the internal parasitic diode. Conditions where V_{OUT} might exceed V_{IN} should be avoided since this would forward bias the internal parasitic diode and allow excessive current flow into the V_{OUT} pin, possibly damaging the LDO regulator. In applications where there is a possibility of V_{OUT} exceeding V_{IN} for brief amounts of time during normal operation, the use of a larger value C_{IN} capacitor is highly recommended. A larger value of C_{IN} with respect to C_{OUT} will affect a slower C_{IN} decay rate during shutdown, thus preventing V_{OUT} from exceeding V_{IN}. In applications where there is a greater danger of V_{OUT} exceeding V_{IN} for extended periods of time, it is recommended to place a Schottky diode across V_{IN} to V_{OUT} (connecting the cathode to V_{IN} and anode to V_{OUT}). The Schottky diode forward voltage should be less than 0.45V.

Thermal Calculations

There are three types of losses associated with the AAT2688 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the synchronous step-down converter and LDO losses is given by:

$$P_{TOTAL} = \frac{I_{OUT1}^2 \cdot (R_{DS(ON)H} \cdot V_{OUT1} + R_{DS(ON)L} \cdot [V_{IN1} - V_{OUT1}])}{V_{IN1}}$$

$$+ (t_{SW} \cdot F_S \cdot I_{OUT1} + I_{Q1}) \cdot V_{IN1} + (V_{IN2} - V_{OUT2}) \cdot I_{OUT2}$$

I_{Q1} and I_{Q2} are the step-down converter and LDO quiescent currents respectively. The term t_{SW} is used to estimate the full load step-down converter switching losses.

For a synchronous Step-Down converter, the power dissipation occurs in the internal high side MOSFET during the on time and the external low side MOSFET during the off time. When the internal high side switch is off, the power dissipates on the external low side switch. The total package losses for AAT2688 reduce to the following equation:

$$P_{TOTAL} = I_{OUT1}^2 \cdot R_{DS(ON)H} \cdot D + (t_{SW} \cdot F_S \cdot I_{OUT1} + I_{Q1}) \cdot V_{IN} + (V_{IN2} - V_{OUT2}) \cdot I_{OUT2}$$

Where: $D = \frac{V_{OUT}}{V_{IN}}$ is the duty cycle.

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

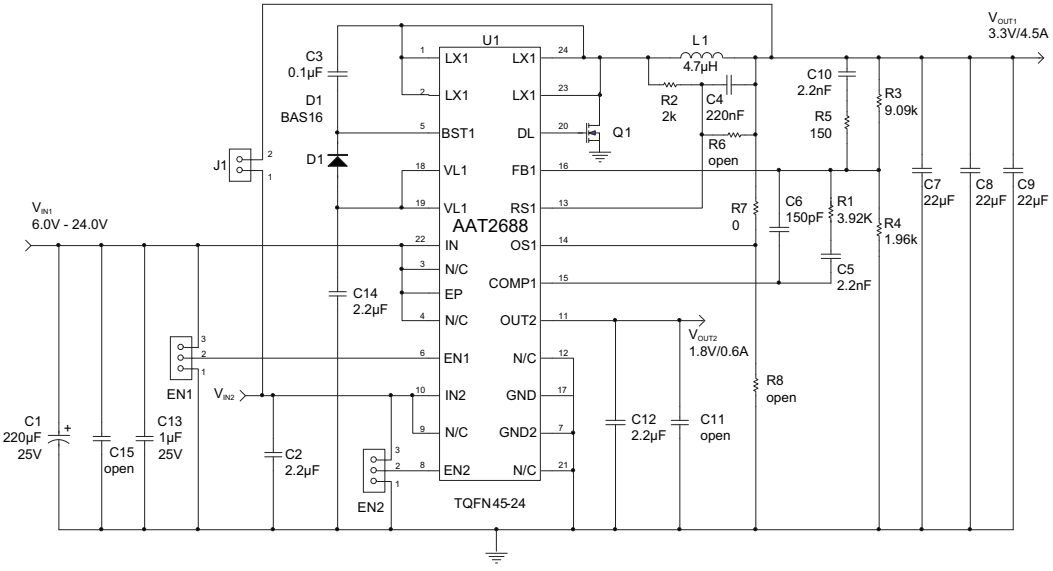
Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the TQFN45-24 package, which is 33°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \theta_{JA} + T_{AMB}$$

Layout Considerations

The suggested PCB layout for the AAT2688 is shown in Figures 5 through 8. The following guidelines should be used to help ensure a proper layout.

1. The power input capacitors (C1 and C15) should be connected as close as possible to high voltage input pin (IN1) and power ground.
2. C1, L1, Q1, C7, C8, and C9 should be place as close as possible to minimize any parasitic inductance in the switched current path which generates a large voltage spike during the switching interval. The connection of inductor to switching node should be as short as possible.
3. The feedback trace or FB1 pin should be separated from any power trace and connected as close as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
4. The resistance of the trace from the load returns to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. Connect unused signal pins to ground or input to avoid unwanted noise coupling.
6. The critical small signal components include feedback components, and compensation components should be placed close to the FB1 and COMP1 pins. The feedback resistors should be located as close as possible to the FB1 pin with its ground tied straight to the signal ground plane which is separated from power ground plane.
7. C4 should be connected close to the RS1 and OS1 pins, while R2 should be connected close to the inductor.
8. R7 should be connected directly to the output pin of inductor L1 to sense precisely its DCR.
9. For good thermal coupling, a 4-layer PCB layout is recommended and PCB vias are required from the exposed pad (EP) for the TQFN45-24 paddle to the middle plans and bottom plane. The EP is internally connected to IN.



U1	AAT2688 Analogic Technologies, Hi-Voltage Buck/LDO, TQFN45-24
C1	Cap, MLC, 220µF/25V, Electrolytic cap
C2, C12, C14	Cap, MLC, 2.2µF, 6.3V, 0805
C3	Cap, MLC, 0.1µF/6.3V, 0603
C4	Cap, MLC, 220nF/6.3V, 0402
C5, C6, C10, C11	Cap, MLC, misc, 0603
C7, C8, C9	Cap, MLC, 22µF/10V, 1206
C13	Cap, MLC, 1µF, 25V, 0805
D1	BAS16, Generic, Rectifier, 0.2A/85V, Ultrafast, SOT23
Q1	SOP8 MOSFET, Si4686DY, Vishay or FDS8884, Fairchild
L1	RCH108NP-4R7M, Sumida, 4.7µH, I_{SAT} = 5.7A, DCR = 11.7mΩ; Unshielded or Wurth 744 771 004, 4.7µH, I_{SAT} = 6.8A, DCR = 11mΩ, Shielded
R1-R5	Carbon film resistor, 0402

Figure 4: AAT2688 Evaluation Board Schematic for V_{IN} = 6V-24V and V_{OUT} = 3.3V.

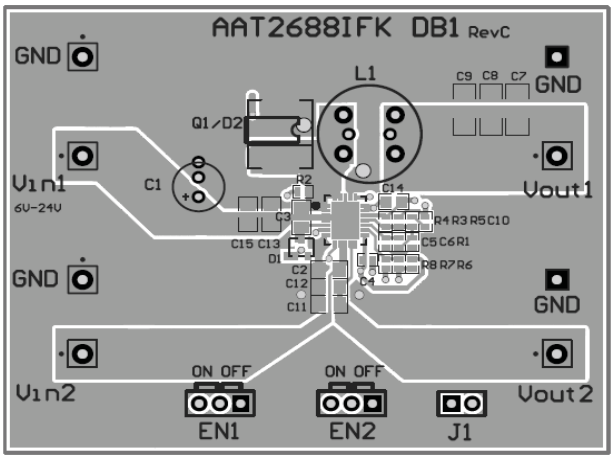


Figure 5: AAT2688IFK Evaluation Board Top Layer.

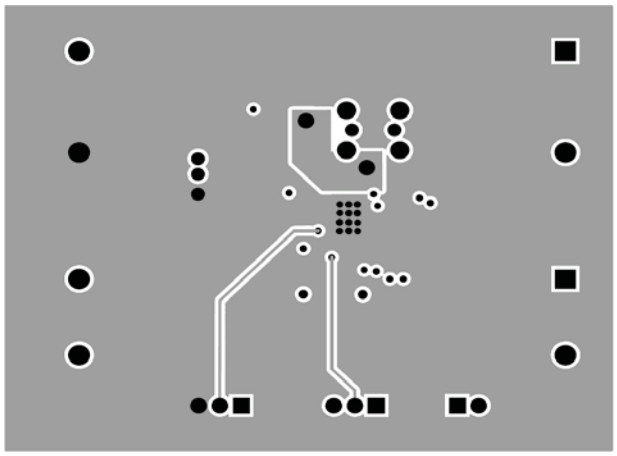


Figure 6: AAT2688IFK Evaluation Board Mid1 Layer.

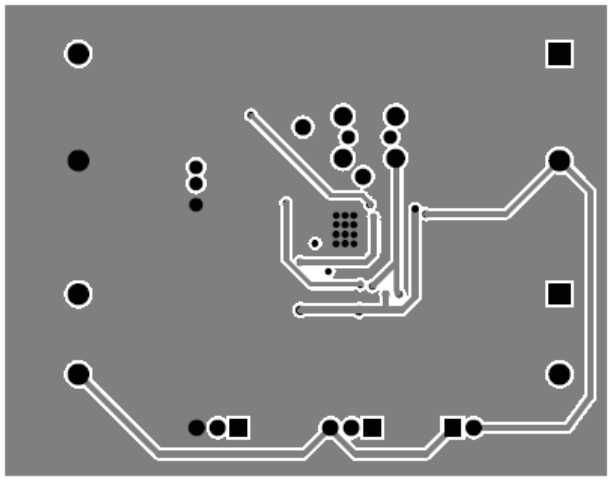


Figure 7: AAT2688IFK Evaluation Board Mid2 Layer.

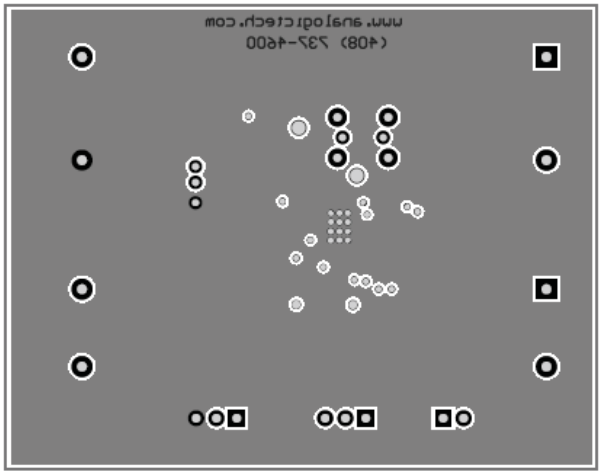


Figure 8: AAT2688IFK Evaluation Board Bottom Layer.

AAT2688 Design Example

Specifications

V_{O1} = 3.3V @ 4.5A, Pulsed Load ΔI_{LOAD} = 4.5A
V_{O2} = 1.8V @ 600mA
V_{IN1} = 12V
F_S = 490kHz
T_{AMB} = 85°C in TQFN45-24 package

Channel 1 Output Inductor

For Sumida inductor RCH108NP-4R7M, 4.7µH, DCR = 11.7mΩ max.

$$\Delta I = \frac{V_{OUT1}}{L_1 \cdot F_S} \cdot \left(1 - \frac{V_{OUT1}}{V_{IN1}}\right) = \frac{3.3V}{4.7\mu H \cdot 490kHz} \cdot \left(1 - \frac{3.3V}{12V}\right) = 1A$$

$$I_{PK1} = I_{OUT1} + \frac{\Delta I}{2} = 4.5A + 1A = 5.5A$$

$$P_{L1} = I_{OUT1}^2 \cdot DCR = 5.5A^2 \cdot 11.7m\Omega = 354mW$$

Channel 1 Output Capacitor

V_{DROOP} = 0.4V

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 4.5A}{0.4V \cdot 490kHz} = 69\mu F; \text{ use } 3x22\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT1} \cdot (V_{IN(MAX)} - V_{OUT1})}{L \cdot F_S \cdot V_{IN1(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{3.3V \cdot (24V - 3.3V)}{4.7\mu H \cdot 490kHz \cdot 24V} = 357mA_{RMS}$$

$$P_{RMS} = ESR \cdot I_{RMS}^2 = 5m\Omega \cdot (357mA)^2 = 0.6W$$

Channel 1 Input Capacitor

Input Ripple V_{PP} = 33mV

$$C_{IN1} = \frac{1}{\left(\frac{V_{PP}}{I_{OUT1}} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{33mV}{4.5A} - 5m\Omega\right) \cdot 4 \cdot 490kHz} = 219\mu F$$

For low cost applications, a 220µF/25V electrolytic capacitor in parallel with a 1µF/25V ceramic capacitor is used to reduce the ESR.

$$I_{RMS} = \frac{I_{OUT1}}{2} = 2.25A$$

$$P = ESR \cdot (I_{RMS})^2 = 5m\Omega \cdot (2.25A)^2 = 25.3mW$$

Channel 1 Current Limit

Voltage sense V_S = 100mV
Total trace parasitic resistor and inductor DCR = 10mΩ

$$I_{PRESET} = \frac{V_S}{DCR} = \frac{100mV}{10m\Omega} = 10A > I_{LIMIT}$$

$$R_8 = \frac{V_{OUT} \cdot R_2}{V_S - I_{LIMIT} \cdot DCR} = \frac{3.3V \cdot 2k\Omega}{0.1V - 6A \cdot 10m\Omega} = 165k\Omega$$

$$R_7 = \frac{R_2 \cdot R_8}{R_8 - R_2} = \frac{2k\Omega \cdot 165k\Omega}{165k\Omega - 2k\Omega} = 2k\Omega$$

AAT2688 Losses

All values assume 25°C ambient temperature and thermal resistor of 50°C/W in the TQFN45-24 package.

$$P_{TOTAL} = I_{OUT1}^2 \cdot R_{DS(ON)H} \cdot D + (t_{SW} \cdot F_S \cdot I_{OUT1} + I_Q) \cdot V_{IN} + (V_{IN2} - V_{OUT2}) \cdot I_{OUT2}$$

$$P_{TOTAL} = \frac{4.5A^2 \cdot 70m\Omega \cdot 3.3V}{12V} + (5ns \cdot 490kHz \cdot 4.5A + 70\mu A) \cdot 12V + (3.3 - 1.8) \cdot 600mA$$

$$P_{TOTAL} = 1.42W$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (33°C/W) \cdot 1.42W = 131°C$$

Ordering Information

Package	Voltage		Marking[1]	Part Number (Tape and Reel)[2]
	Channel 1	Channel 2		
TQFN45-24	Adjustable	1.8	3WXYY	**AAT2688IFK-AI-T1**

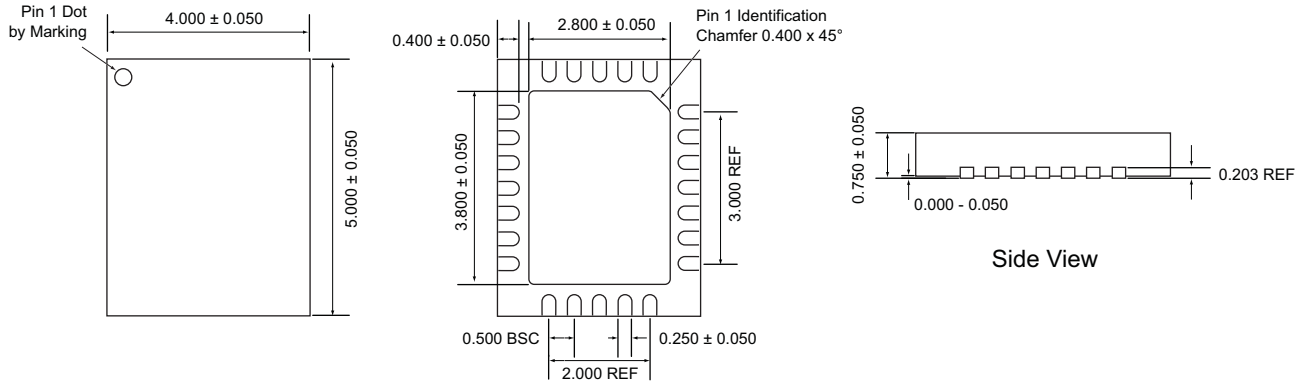
Pb-free

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.

Legend	
Voltage	Code
Adjustable	A
1.8	I

Package Information

TQFN45-24[3]



Top View

Bottom View

All dimensions in millimeters.

1. XYY = Assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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