ANALOGIC TECH™

AAT4702

SmartSwitch™　　**Auto-Restarting Current Limiting Load Switch with LDO Regulator**

General Description

The AAT4702 SmartSwitch™ is a member of AnalogicTech's Application Specific Power MOSFET™ (ASPM™) product family. This device integrates a high side P-channel MOSFET current limiting load switch with a nanopower low dropout (LDO) linear voltage regulator, making the AAT4702 ideal for use in load current protected applications that also require a system power supply. The load switch operates with input voltages ranging from 2.4V to 5.5V, making it ideal for 2.5V, 3V, and 5V systems. A fault flag is provided to alert the system to an over-current event. The fault flag has a 5ms blanking time to prevent from reporting false events such as inrush currents during system startup.

The load switch current limit is 150mA by default or programmed up to 1A through an external set resistor.

The AAT4702 LDO linear regulator is designed to deliver a regulated 1.8V supply voltage for load levels up to 100mA. The regulator section may be powered directly from an input source supply or from the load switch output.

The AAT4702 is offered in a Pb-free, space-saving 8-pin 2x2mm FTDFN22 package, and is specified for operation over the -40°C to +85°C ambient temperature range.

Features

Load Switch:
- 2.4V-5.5V Input Voltage Range
- 150mA Default Current Limit Level
- 270mΩ Typical $R_{DS(ON)}$ at 2.4V
- 400ns Response to Short Circuit
- Reverse Voltage Protection
- Current Limit Shutdown with Output Pull Down
- Auto Restart with 40ms Timer
- 5ms Fault Blanking Timeout
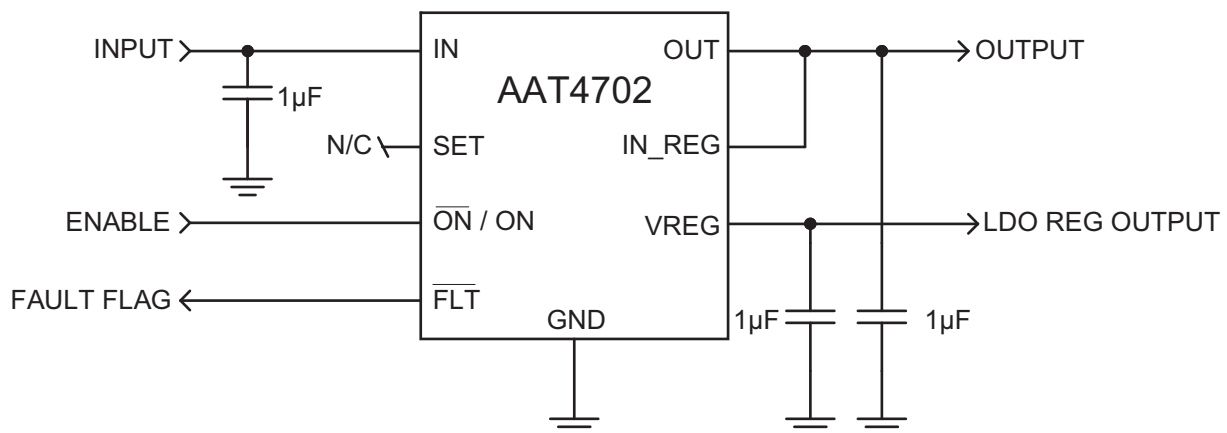- Under-Voltage Lockout Protection

LDO Regulator:
- Output Current up to 100mA
- 1.8V Output Voltage with ±2% Accuracy
- Thermal and Short Circuit Protection
- Active Shutdown Output Pull-Down
- Low Quiescent Current 15µA Typical for Switch and LDO
- Less than 1µA Shutdown Current
- Only 1µF Ceramic Output Capacitor Required
- Available in FTDFN22-8L Package.

Applications

- Cell Phones
- Device Peripheral Ports
- Fingerprint Sensors
- Hot Swap Supplies
- Media Players
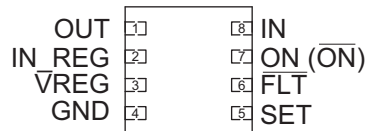- Notebook Computers

Typical Application

SmartSwitch™   ***Auto-Restarting Current Limiting Load Switch with LDO Regulator***

Pin Descriptions

Pin #	Symbol	Description
1	OUT	Current limited P-channel MOSFET load switch output. A 0.47µF to 1µF ceramic capacitor connected from OUT to GND is recommended for best circuit response.
2	IN_REG	LDO regulator power input. Connect to IN to power from a common input supply with the load switch, in which case, bypass with a 1µF ceramic capacitor connected between this pin and ground. Alternatively, this pin may be powered from the load switch output by connecting IN_REG to OUT; a 1µF or greater ceramic capacitor should be placed between the OUT pin and ground for this application
3	VREG	LDO regulator output. Connect a 1µF or larger capacitor from VREG to GND for best operating performance.
4	GND	IC ground pin.
5	SET	Current limit set input. Connect a resistor from SET to ground to program current limit set point for the load switch. Or leave open for 150mA default current limit level.
6	$\overline{FLT}$	Fault flag, open drain output. Pull to a logic high level through an external resistor for normal operation. Pulled low when fault is present. Leave open if unused.
7	ON ($\overline{ON}$)	Enable input for load switch and LDO regulator. AAT4702 -1: Active low; pull to a logic low level to enable. AAT4702 -2: Active high; pull to a logic high level to enable.
8	IN	Input to the P-channel MOSFET source. Connect a 1µF capacitor from IN to GND.

Pin Configuration

FTDFN22-8L
(Top View)

OUT	1	8	IN
IN_REG	2	7	ON ($\overline{ON}$)
$\overline{VREG}$	3	6	$\overline{FLT}$
GND	4	5	SET

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Absolute Maximum Ratings[1]

T_A = 25°C unless otherwise noted.

Symbol	Description	Value	Units
$V_{IN, FAULT}$	IN, IN_REG, FAULT to GND	-0.3 to 6	
V_{ON}	ON to GND	-0.3 to V_{IN} + 0.3	V
V_{OUT}	OUT to GND	-0.3 to V_{IN} + 0.3	
I_{OUT}	Maximum Output Current[2]	Internally Limited	A
V_{ESD}	ESD Rating, HBM	4000	V
T_J	Maximum Junction Operating temperature	-40 to +150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	

Thermal Information[3]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance	116.3	°C/W
P_D	Maximum Power Dissipation[4] (T_A = 25°C)	860	mW

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Based on long-term current density limitations.
3. Mounted on 1oz. copper clad FR4 material printed circuit board.
4. Derate 8.6mW/°C above 25°C.

Electrical Characteristics[1]

V_{IN}=3.6V; T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
General						
$V_{IN(SW)}$	Input Voltage Range	Load Switch Section	2.4		5.5	V
$V_{IN(REG)}$	Input Voltage Range	Stable Output	2.4		5.5	
		For V_{OUT} Within Regulation Tolerance	$V_{OUT} + V_{DO}$		5.5	%
I_Q	Operation Quiescent Current	V_{IN} = 5V, $\overline{ON}$ = 0V, I_{OUT} = 0		15	30	μA
$I_{SD(OFF)}$	Shutdown Supply Current	$\overline{ON}$ = IN = 5.5V, V_{OUT} = 0			1	μA
Load Switch						
$R_{DS(ON)}$	PMOS On-Resistance	V_{OUT} = 5V, T_A = 25°C		180	280	mΩ
		V_{OUT} = 3.6V, T_A = 25°C		220	320	
		V_{OUT} = 2.4V, T_A = 25°C		270	360	
$I_{D(OFF)}$	Switch Off-Leakage	$\overline{ON}$ = V_{IN}			1	μA
I_{LIM}	Current Limit	Rising edge; R_{SET} = open	100	150	200	mA
RSET_INT	Current Limit Internal Set Resistor			50		kΩ
V_{UVLO}	Under-Voltage Lockout Threshold	Rising edge		1.8	2.4	V
V_{UVLO_HYS}	Under-Voltage Lockout Hysteresis			0.2		V
LDO Regulator						
V_{OUT}	DC Output Voltage	V_{IN} = 3.6V, I_{OUT} = 10mA	1.764	1.8	1.836	V
I_{OUT}	Output Current	V_{OUT} = 1.8V			100	mA
I_{SC}	Short-Circuit Current	V_{OUT} < 0.4V		350		mA
$\Delta V_{OUT}/$ $V_{OUT}*\Delta V_{IN}$	Line Regulation	V_{IN} = 4.0 to 5.5V, T_A = 25°C		0.14	0.4	%/V
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	I_{OUT} = 1mA to 100mA, V_{OUT} = 1.8V, T_A = 25°C		1.0	1.65	%
V_{DO}	Dropout Voltage	I_{OUT} = 100mA, V_{OUT} = 1.8V		300		mV
$R_{DS(REG)}$	Regulator Pass Element On-Resistance	V_{IN_REG} = 3.6V		3.0		Ω
PSRR	Power Supply Rejection Ratio	100Hz		50		dB
T_C	Output Voltage Temperature Coefficient			80		PPM/°C
Logic						
$V_{EN(L)}$	$\overline{ON}$ Input Low Voltage				0.4	V
$V_{EN(H)}$	$\overline{ON}$ Input High Voltage	2.4V < V_{IN} ≤ 4.2V	2.0			V
		4.2V < V_{IN} < 5.5V	2.4			
I_{EN}	$\overline{ON}$ Input Leakage	V_{EN} = 5.5V or 0V		0.5	2.0	μA
t_{AUTO}	Auto-Restart Time		20	40	80	ms
t_{BLANK}	Over-Current Blanking Time		2	5	10	ms
t_{RESP}	Current Limit Response Time	V_{IN} = 5V		0.4		μs
t_{ON}	Load Switch Turn On Time	V_{IN} = 5V; R_O = 10Ω; C_O = 1μF		18	35	μs
t_{OFF}	Load Switch Turn Off Time	V_{IN} = 5V; R_O = 10Ω; C_O = 1μF		3	10	μs
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			20		°C

1. The AAT4702 is guaranteed to meet performance over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
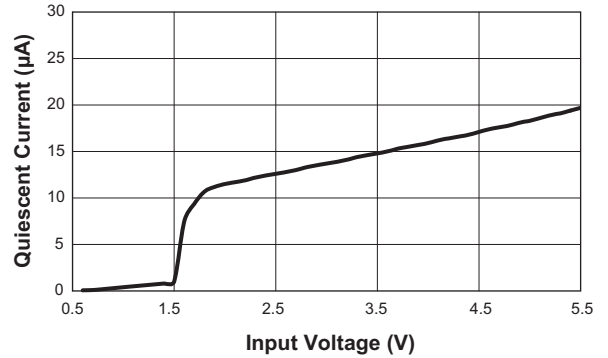
ANALOGIC TECH

SmartSwitch™   *Auto-Restarting Current Limiting Load Switch with LDO Regulator*

Typical Characteristics−General

Unless otherwise noted, V_{IN}= 3.6V, C_{IN} = 1µF, C_{OUT} = 1µF, $C_{OUT-LDO}$ = 1µF ,T_A = 25°C.
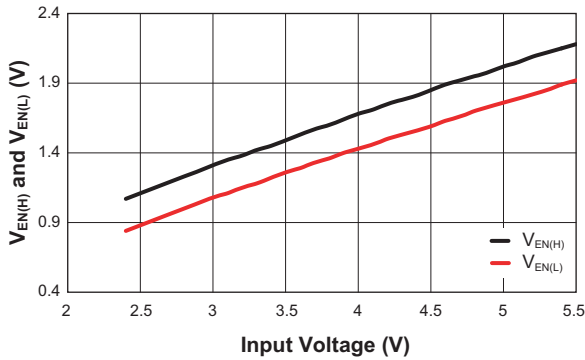
Quiescent Current vs. Temperature
(Load Switch + LDO)
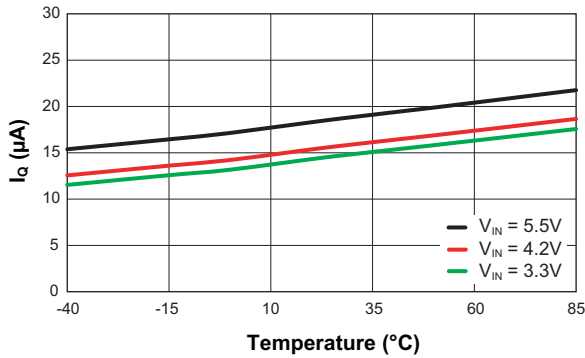
Quiescent Current vs. Input Voltage
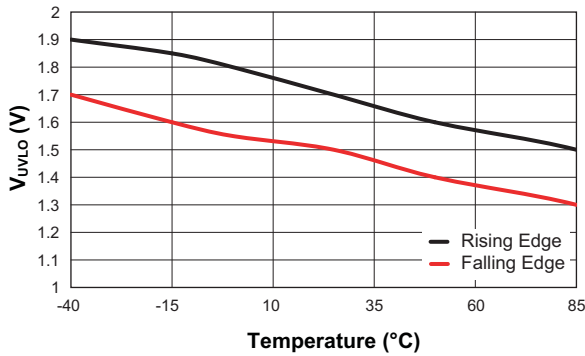**(Load Switch + LDO)**
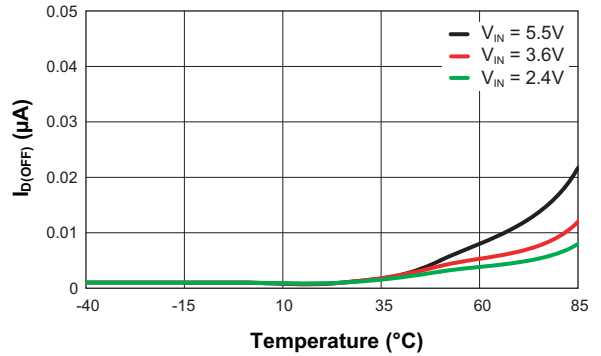
$V_{EN(H)}$ and $V_{EN(L)}$ vs. Input Voltage

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SmartSwitch™   *Auto-Restarting Current Limiting Load Switch with LDO Regulator*

Typical Characteristics–Load Switch

Unless otherwise noted, V_{IN}= 3.6V, C_{IN} = 1µF, C_{OUT} = 1µF, $C_{OUT-LDO}$ = 1µF ,T_A = 25°C.

V_{UVLO} vs. Temperature
(Rising and Falling)

Switch Off-Leakage Current
vs. Temperature

$R_{DS(ON)}$ vs. Input Voltage
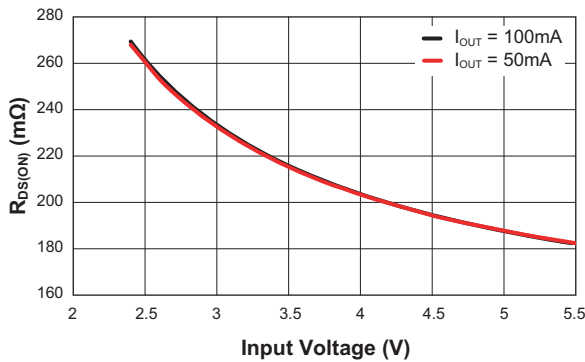
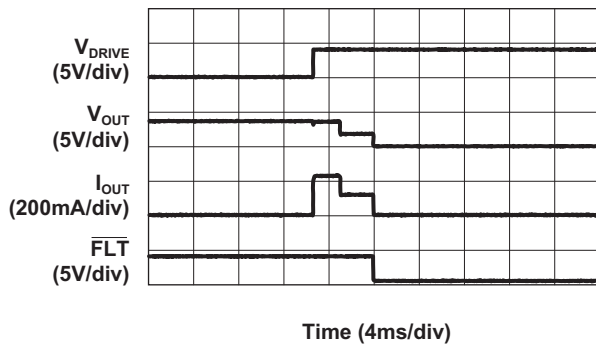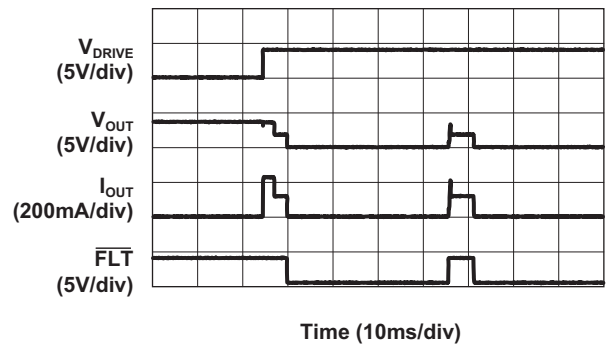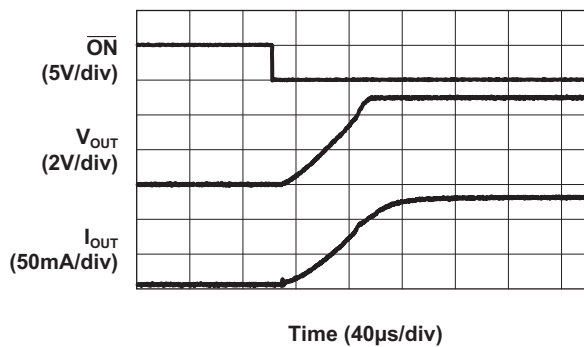**$R_{DS(ON)}$ vs. Temperature**
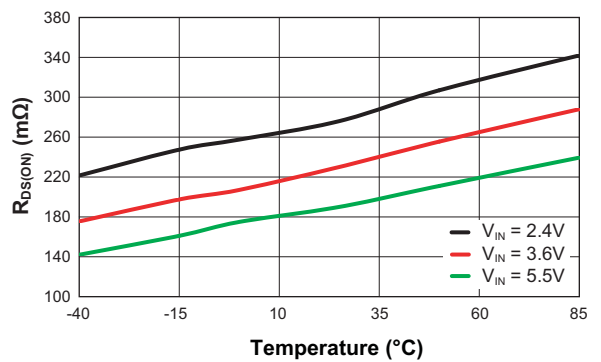
Current Limit vs. Output Voltage
(R_{SET} = Open)
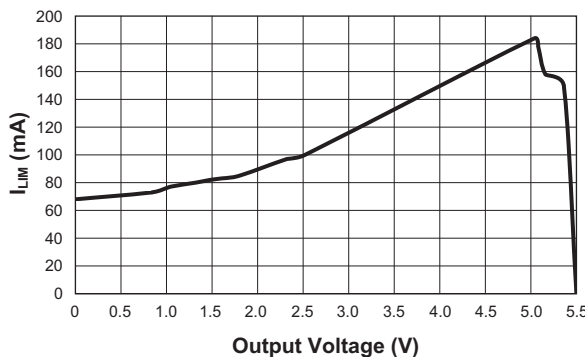
R_{SET} vs. I_{LIM}
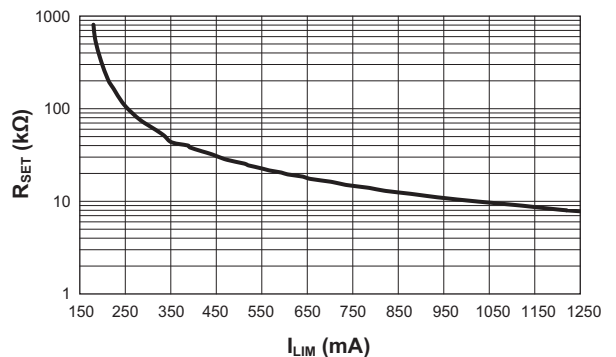
Typical Characteristics–Load Switch

Unless otherwise noted, V_{IN}= 3.6V, C_{IN} = 1µF, C_{OUT} = 1µF, $C_{OUT-LDO}$ = 1µF ,T_A = 25°C.

T_{BLANK} Response
(V_{IN} = 4V; R_{SET} = Open)

V_{DRIVE}
(5V/div)

V_{OUT}
(5V/div)

I_{OUT}
(200mA/div)

$\overline{FLT}$
(5V/div)

Time (4ms/div)

T_{AUTO} Response
(V_{IN} = 4V; R_{SET} = Open)

V_{DRIVE}
(5V/div)

V_{OUT}
(5V/div)

I_{OUT}
(200mA/div)

$\overline{FLT}$
(5V/div)

Time (10ms/div)

T_{ON} Response
(V_{IN} = 5V; R_L = 40Ω; C_L = 0.1µF)

$\overline{ON}$
(5V/div)

V_{OUT}
(2V/div)

I_{OUT}
(50mA/div)

Time (40µs/div)

T_{OFF} Response
(V_{IN} = 5V; R_L = 40Ω; C_L = 1µF)

$\overline{ON}$
(5V/div)

V_{OUT}
(2V/div)

I_{OUT}
(50mA/div)

Time (40µs/div)

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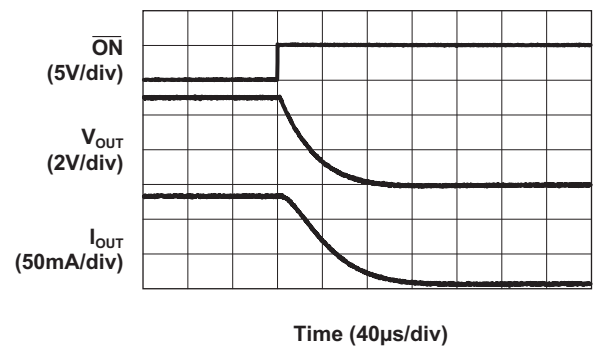
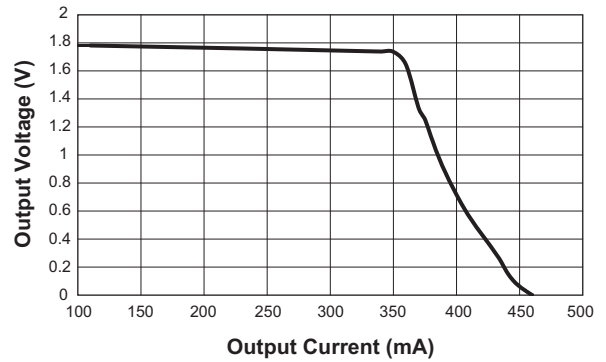## Typical Characteristics−LDO Regulator

Unless otherwise noted, V_{IN}= 3.6V, C_{IN} = 1µF, C_{OUT} = 1µF, $C_{OUT-LDO}$ = 1µF ,T_A = 25°C.
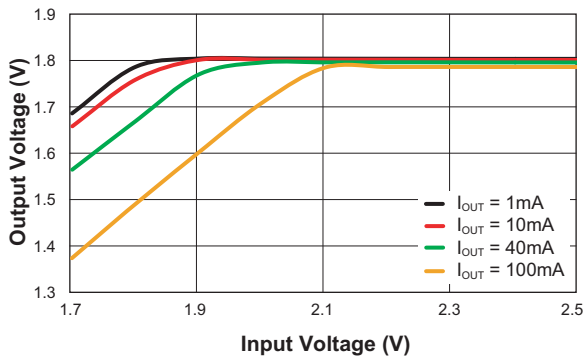
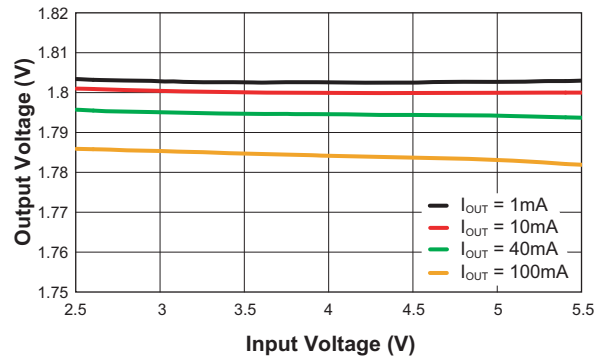**Output Voltage vs. Output Current**
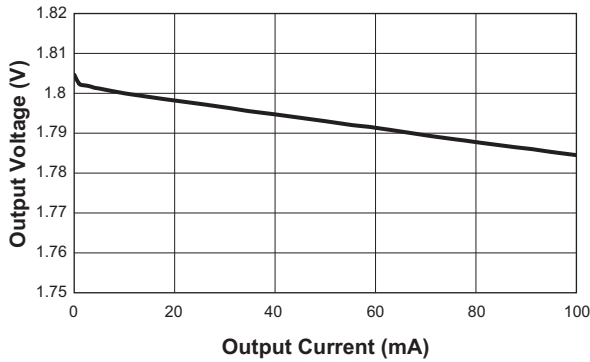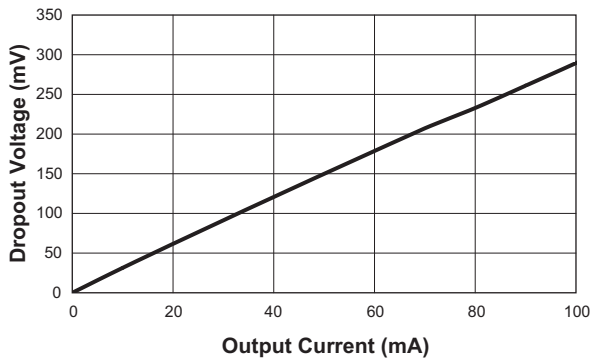
Output Voltage vs. Output Current

Output Voltage vs. Input Voltage

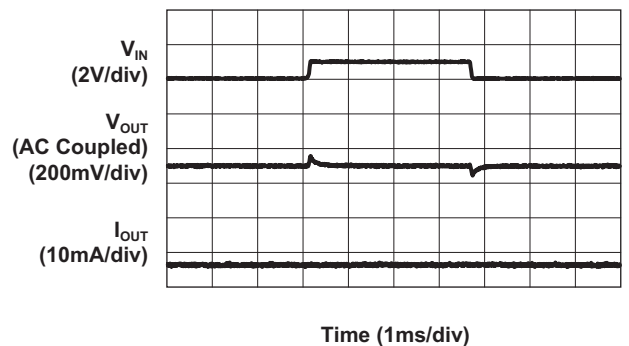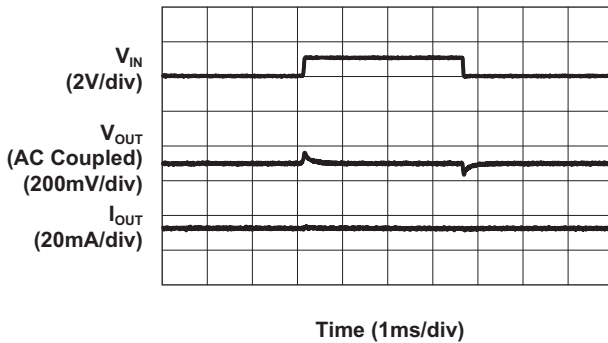**Output Voltage vs. Input Voltage**

Dropout Voltage vs. Output Current

Line Transient Response
(V_{IN} = 4V->5V->4V; I_{OUT} = 1mA)

V_{IN}
(2V/div)

V_{OUT}
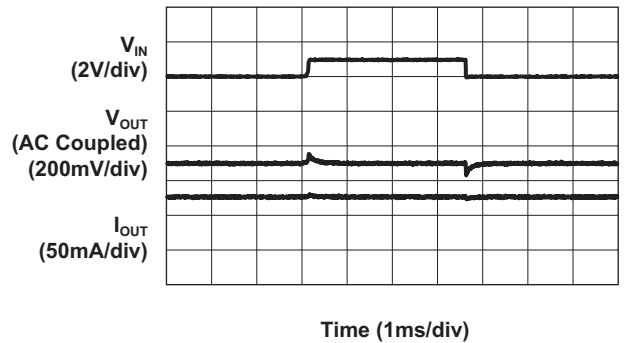(AC Coupled)
(200mV/div)

I_{OUT}
(10mA/div)

Time (1ms/div)

Typical Characteristics−LDO Regulator

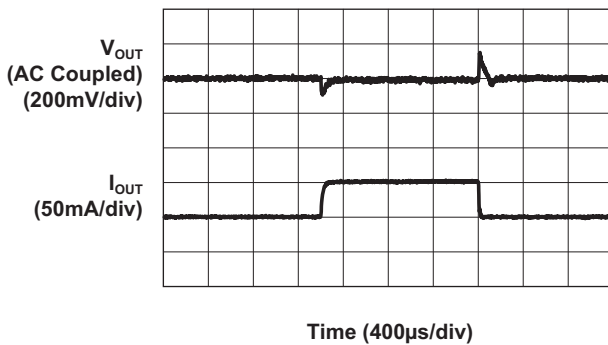Unless otherwise noted, V_{IN}= 3.6V, C_{IN} = 1µF, C_{OUT} = 1µF, $C_{OUT-LDO}$ = 1µF ,T_A = 25°C.

Line Transient Response
(V_{IN} = 4V->5V->4V; I_{OUT} = 20mA)

V_{IN} (2V/div)
V_{OUT} (AC Coupled) (200mV/div)
I_{OUT} (20mA/div)

Time (1ms/div)

Line Transient Response
(V_{IN} = 4V->5V->4V; I_{OUT} = 100mA)

V_{IN} (2V/div)
V_{OUT} (AC Coupled) (200mV/div)
I_{OUT} (50mA/div)

Time (1ms/div)

Load Transient Response
(V_{IN} = 4V; I_{OUT} = 1mA-50mA)

V_{OUT} (AC Coupled) (200mV/div)
I_{OUT} (50mA/div)

Time (400µs/div)

Load Transient Response
(V_{IN} = 4V; I_{OUT} = 1mA-100mA)

V_{OUT} (AC Coupled) (200mV/div)
I_{OUT} (50mA/div)

Time (400µs/div)

Power-Up with 1mA Load

$\overline{ON}$ (2V/div)
V_{OUT} (1V/div)

Time (200µs/div)

Power-Up with 100mA Load

$\overline{ON}$ (2V/div)
V_{OUT} (1V/div)

Time (200µs/div)
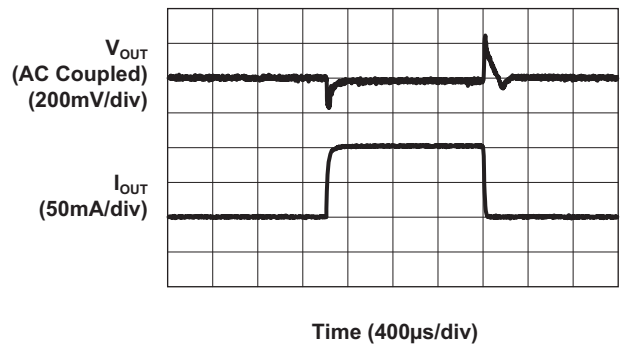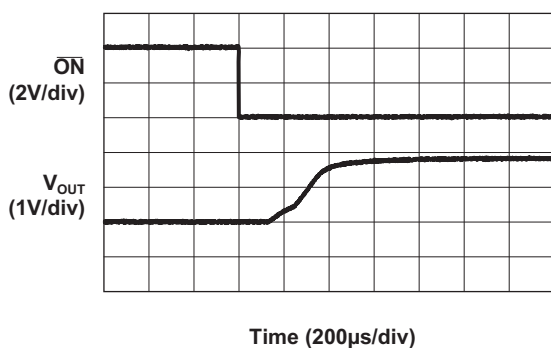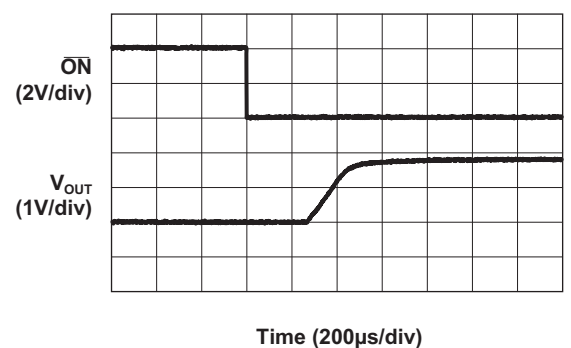
Functional Block Diagram
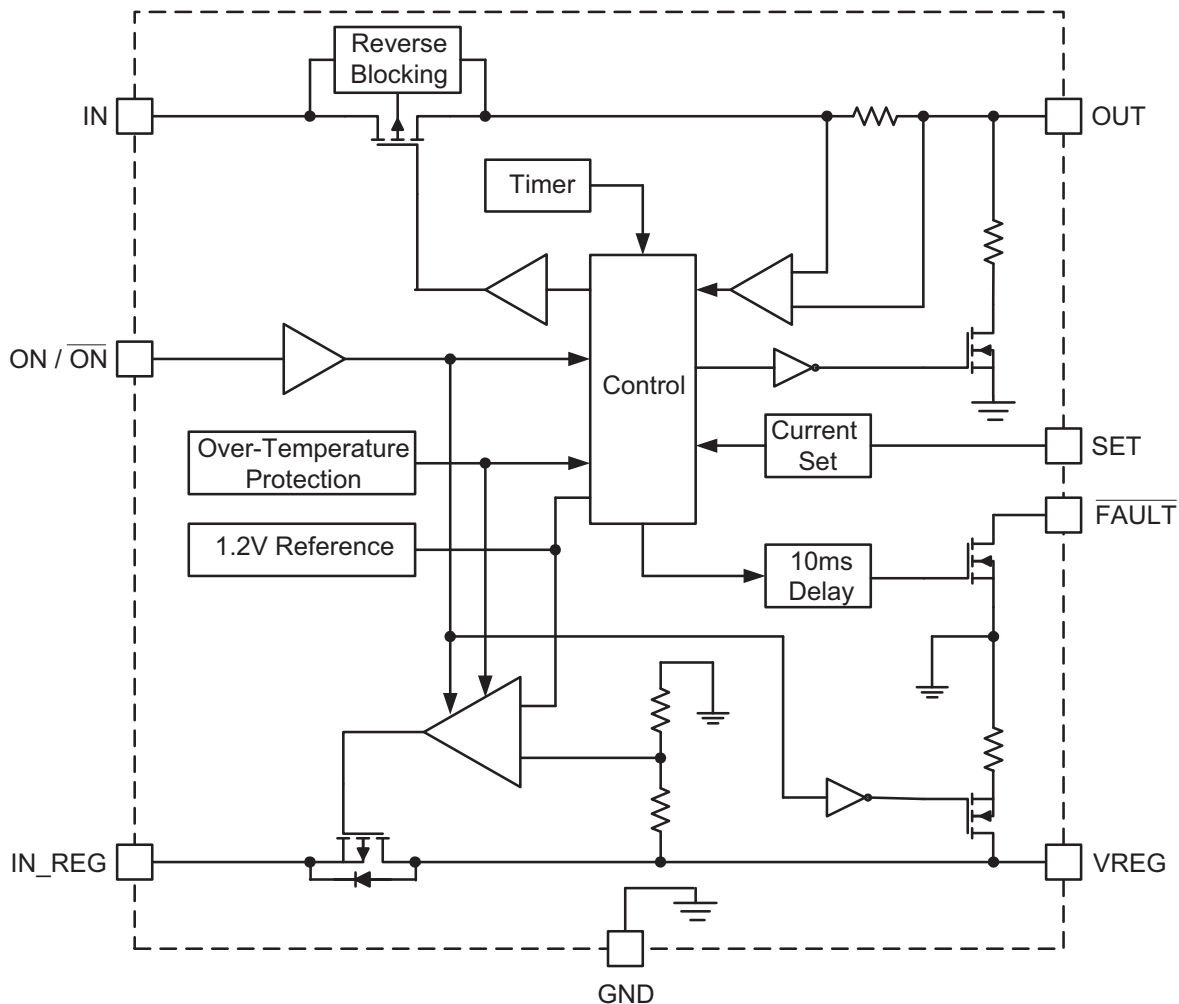
Functional Description

The AAT4702 is an auto-restarting current limiting load switch with an integrated low dropout linear voltage regulator. The combined function of this device serves to protect system loads or peripheral circuits from over-current conditions while simultaneously supplying an independent regulated voltage for the system.

Current Limiting Load Switch

The AAT4702 load switch provides an auto-restarting, reverse current blocking, programmable current limiting and shutdown function. If an applied load exceeds the programmed current limit level, the load switch pass element will be turned off to isolate the input source from the output and discharge the applied load to ground via an internal NMOS switch and a typical 100Ω resistor. The default current limit (I_{LIM}) set point is 150mA with a ±50mA tolerance when the SET pin is left open (no external resistor connected). The device may be user programmed to a higher current limit level up to 1A via an external resistor placed between the SET pin and ground.

When under an output over-current shutdown event, the AAT4702 has an auto-restart output polling function that will wake up and re-enable the device every 40ms to check for the continued existence of an over-current condition. If the over-current fault condition remains, the AAT4702 will remain in the shutdown state with both the load switch and LDO regulator output pulled low to

ground. When the over-current condition is removed, the AAT4702 will automatically resume normal operation.

The internal load switch controller provides a fault flag function to alert a system controller to any over current or temperature event. The fault flag output consists of an open drain NMOS switch that should be pulled to a logic high level externally through a 10kΩ or greater value resistor. The fault flag has a 5ms blanking time feature to guard against reporting false fault conditions, such events could happen during normal circuit start-up. If the fault flag function is not required, the $\overline{FLT}$ pin may be left unconnected.

When operating within the limits set by the default or user programmed current limit level, the device over-temperature protection will monitor the internal die temperature. If the internal die temperature exceeds 140°C, the thermal protection circuit will shut down the load switch to protect the loaded device and the system supply source.

The AAT4702 load switch and LDO regulator are enabled and disabled through common enable signal at the ON ($\overline{ON}$) pin. The AAT4702 provides options for both active low (default) and/or active high operation; refer to the Ordering Information table to select the desired enable polarity. If the device is operated in an always-on state, the enable function may be terminated to GND or IN respective to which active low or high option is selected.

The AAT4702 load switch has an under-voltage lockout (UVLO) function, which senses the voltage of the IN pin. Once $V_{IN} > V_{UVLO}$ rising edge (typical 1.8V), the AAT4702 will start to operate. For the LDO regulator input IN_REG pin, there is no UVLO.

Low Dropout Linear Regulator

The AAT4702 LDO linear regulator section has an independent input pin allowing the regulator to be powered by the load switch output or directly from an input supply. When the enable pin switches to an active state, the LDO regulator output will typically start up and stabilize regulation within 1ms after the load switch.

The LDO regulator output is designed and tested to maintain voltage regulation accuracy within a ±2% toler-

ance. Voltage regulation accuracy is maintained for input voltage ranges from 5.5V down to a minimum input level (V_{IN_MIN}) which is defined by the factory trimmed output voltage level (V_{OUT}) plus the specified regulator dropout voltage level (V_{DO}), by following the formula:

$$V_{IN\_MIN} = V_{OUT} + V_{DO}$$

Where:
V_{IN_MIN} = Minimum input voltage applied to the IN_REG pin to maintain regulation
V_{OUT} = Factory set LDO regulator output as measured at the VREG pin
V_{DO} = Specified LDO regulator dropout voltage

Should the LDO regulator input supply fall below the required V_{IN_MIN} level, the output is designed to track the input supply minus a nominal voltage drop across the regulator's high-side P-channel MOSFET caused by the device's on resistance. The regulator is designed to maintain a stable linear output level of 1.8V for an input supply level down to 2.4V at the specified load current level of 100mA.

During LDO regulator shutdown, the VREG output is internally connected to ground via a series resistor and a low-side NMOS switch which have a combined impedance of 100Ω. The LDO regulator has over-temperature and short-circuit protection independent to the load switch for comprehensive device protection.

Since the system enable is common to both the LDO regulator and load switch, the LDO regulator will shut down in the event of a fault occurring on the load switch output. For the case of LDO regulator shut down via a load switch fault, the LDO regulator automatically restarts along with the load switch auto-restart system with a 1ms delay. When the LDO regulator is shut down by either the enable function or a fault on the load switch output, the regulator output load will be discharged through the internal active output pull-down circuit.

The AAT4702 LDO regulator has high power supply ripple rejection (PSRR) in addition to fast load and line transient response characteristics. The LDO regulator output has been specifically optimized to function with low cost, low-ESR ceramic capacitors.

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Application Information

Setting the Load Switch Current Limit

With no external resistor at the SET pin, the default current limit is 150mA typically set by the internal 50kΩ resister. The current limit function is triggered when the load current reaches 150mA, the load switch and LDO output voltages are shut down; the AAT4702 would restart to check if the over-current condition is removed every 40ms. As illustrated in the "Current Limit I_{LIM} vs. Output Voltage" curve, the current limit level is kept lower when the output voltage drops; this is helpful to minimize the power dissipation at the load switch to provide safer operation at over-current or output short-circuit condition.

If a higher current limit is desired, an external resistor could be placed at the SET pin. To determine R_{SET}, multiply the maximum current drawn by the load by 1.33 (typical I_{LIM} = minimum I_{LIM}/0.75); this is the typical current limit value. Next, refer to the "R_{SET} vs. I_{LIM}" curve and find the R_{SET} that corresponds to the typical current limit value. The maximum current is derived by multiplying the typical current for the chosen R_{SET} in the chart by 1.25. Some resistor values are listed in Table 1.

R_{SET} (kΩ)	Current Limit Typ (mA)	Current Limit Min (mA)	Current Limit Max (mA)
205.1	200	150	250
80.9	250	188	313
49.6	300	225	375
39.6	350	263	438
32.2	400	300	500
27.6	450	338	563
24	500	375	625
20.8	550	413	688
17.6	600	450	750
13.3	700	525	875
10.8	800	600	1000
8.82	900	675	1125
7.88	1000	750	1250
6.87	1100	825	1375
6.17	1200	900	1500
5.54	1300	975	1625

Table 1: Current Limit vs. R_{SET} Values.

Example: A USB port requires 500mA. 500mA multiplied by 1.33 is 665mA. From the "R_{SET} vs. I_{LIM}" curve, R_{SET} should be less than 16.5kΩ. 14.9kΩ is a standard value that is a little less than 16.5kΩ but very close. The chart reads approximately 700mA as a typical I_{LIM} value for 14.9kΩ. Multiplying 700mA by 0.75 and 1.25 shows that the AAT4702 load switch will limit the load current to greater than 525mA but less than 875mA.

Load Switch Operation in Current Limit and Thermal Protection

When a heavy load is applied to the output of the AAT4702 load switch output, the current limit circuit is triggered when the load current reaches the value of I_{LIM} determined by R_{SET}. See Figure 1 for over-current operation and fault recovery. Since the load demands more current than I_{LIM}, the voltage at the output drops. When the output voltage drops, the load current is folded back to a lower level. When the overload condition continues for a period longer than the over-current blanking time t_{BLANK}, the output will be turned off and discharged through the internal N-channel MOSFET and resistor. After T_{AUTO} timeout 40ms, the AAT4702 turns on the load switch output to check if the overload condition is removed. If the overload still exists, the output turns off again after t_{BLANK} timeout. The AAT4702 load switch and LDO will continue to cycle on and off until the overload condition is removed. When the die temperature exceeds the over-temperature limit, the AAT4702 will shutdown until it has cooled sufficiently, at which point it will start up again.

Enable Input

The AAT4702 features a load switch and LDO common enable / disable function. This ON ($\overline{ON}$) pin is compatible with CMOS logic. Active high or active low options are available (see Ordering Information).

In many systems, power planes are controlled by integrated circuits which run at lower voltages than the power plane itself. The enable input ON ($\overline{ON}$) of the AAT4702 has low and high threshold voltages that accommodate this condition, which could be found in "$V_{EN(H)}$ and $V_{EN(L)}$ vs. Input Voltage" curve. The threshold voltages are compatible with 5V TTL and 2.4V to 5V CMOS. When enable is active, the load switch starts up, and the LDO starts up after 1ms. When it is disabled, the device shuts down and the LDO output capacitor is discharged through the internal N-channel MOSFET and 100Ω resistor; the load switch is also reverse blocked.
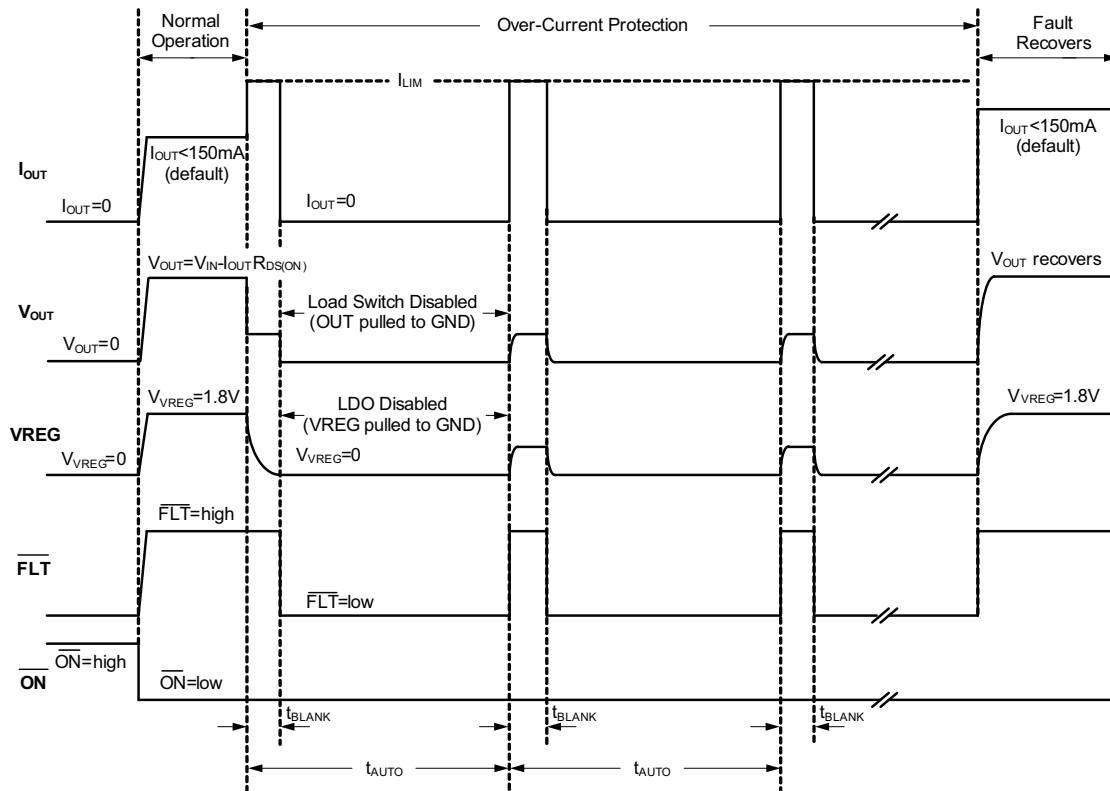
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Figure 1: AAT4702 Device Output and Logic Timing Diagram for a Fault Condition and Fault Recovery.

Reverse Voltage

The AAT4702 load switch is designed to control the current flowing from IN to OUT. If a voltage applied to OUT is greater than the voltage on IN, large current may flow if the enable is active. This could cause damage to the AAT4702. The ON ($\overline{ON}$) pin can be pulled to low to disable the device and prevent current flow from OUT to IN, as the AAT4702 load switch could be reverse blocked when ON ($\overline{ON}$) is disabled.

Input Capacitor

A 1µF or larger ceramic capacitor is typically recommended for C_{IN} in most applications. C_{IN} should be located as closely to the device IN pin as practically possible. C_{IN} value greater than 1µF will offer superior input line transient response and will assist in maximizing the power supply ripple rejection.

Ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

A 1µF or larger ceramic capacitor C_{OUT1} is typically recommended for the load switch output OUT pin in most applications.

For proper load voltage regulation and operational stability, a capacitor is required between pins VREG and GND. The C_{OUT2} capacitor connection to the LDO regulator output VREG pin and GND pin should be made as direct as practically possible for maximum device performance. The AAT4702 LDO has been specially designed to function with very low ESR ceramic capacitors. Although the device is intended to operate with these low ESR capacitors, it is stable over a wide range of capacitor ESR, thus it will also work with some higher ESR tantalum or aluminum electrolytic capacitors. However, for best performance, ceramic capacitors are recommended.

The value of C_{OUT2} typically ranges from 0.47µF to 10µF; however, 1µF is sufficient for most operating conditions.

If large output current steps are required by an application, then an increased value for C_{OUT2} should be consid-

ered. The amount of capacitance needed can be calculated from the step size of the change in output load current expected and the voltage excursion that the load can tolerate.

The total LDO output capacitance required can be calculated using the following formula:

$$C_{OUT2} = \frac{\Delta I}{\Delta V} \cdot 15\mu F$$

Where:

ΔI = maximum step in output current
ΔV = maximum excursion in voltage that the load can tolerate

Note that use of this equation results in capacitor values approximately two to four times the typical value needed for an AAT4702 at room temperature. The increased capacitor value is recommended if tight LDO output tolerance must be maintained over extreme operating conditions and maximum operational temperature excursions. If tantalum or aluminum electrolytic capacitors are used, the capacitor value should be increased to compensate for the substantial ESR inherent to these capacitor types.

Capacitor Characteristics

Ceramic composition capacitors are highly recommended over all other types of capacitors for use with the AAT4702. Ceramic capacitors offer many advantages over the tantalum and aluminum electrolytic counterparts. A ceramic capacitors typically has very low ESR 10mΩ, is lower cost, has a smaller PCB footprint, and is non-polarized. Line and load transient response of the LDO regulator is improved by using low-ESR ceramic capacitors. Since ceramic capacitors are non-polarized, they are less prone to damage if incorrectly connected.

Equivalent series resistance (ESR) is a very important characteristic to consider when selecting a capacitor. ESR is the internal series resistance associated with a capacitor, which includes lead resistance, internal connections, capacitor size and area, material composition, and ambient temperature. Typically, capacitor ESR is measured in milliohms for ceramic capacitors and can range to more than several ohms for tantalum or aluminum electrolytic capacitors.

Ceramic capacitors less than 0.1µF are typically made from NPO or C0G materials. NPO and C0G materials are typically tight tolerance and very stable over temperature. Larger capacitor values are typically composed of X7R, X5R, Y5U, and Z5V dielectric materials. Large ceramic capacitors, typically greater than 2.2µF, are often available in low-cost Y5V and Z5U dielectrics. These two materials types are not recommended for use with LDO regulators since the capacitor tolerance can vary more than ±50% over the operating temperature range of the device. A 2.2µF Y5V capacitor could be reduced to 1µF over the full operating temperature range. This can cause problems for circuit operation and stability. X7R and X5R dielectrics are much more desired. The temperature tolerance of X7R dielectric is better than ±15%.

Capacitor area is another contributor to ESR. Capacitors that are physically large in size will have a lower ESR when compared to a smaller sized capacitor of equivalent material and capacitor value. These larger device can also improve circuit transient response when compared to an equal value capacitor in a smaller package size.

Consult capacitor vendor datasheets carefully when selecting capacitors for use with LDO regulators.

LDO Short-Circuit Protection and Thermal Protection

The AAT4702 LDO regulator is protected by both current limit and over-temperature protection circuitry. The internal short-circuit limit is designed to active when the output load demand exceeds the maximum rated output current. If a short-circuit condition were to continually draw more than the current limit threshold, the LDO regulator's output voltage will drop to a level necessary to supply the current demanded by the load. Under short-circuit or other over-current operating conditions, the output voltage will drop and the AAT4702 die temperature will rapidly increase. Once the device's power dissipation capacity has been exceeded and the internal die temperature reaches approximately 140°C at the over-current condition, the LDO thermal protection circuit will actively turn off the LDO regulator output pass element to prevent the possibility of over-temperature damage. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back below the 140°C trip point.

The interaction between the short-circuit and thermal protection allows the LDO regulator to withstand indefinite short-circuit without sustaining permanent damage.

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LDO No-Load Stability

The AAT4702 LDO regulator is designed to maintain output voltage regulation and stability under operational no-load conditions. This is an important characteristic for applications where the output current may drop to zero. An output capacitor is required for stability under no-load operating conditions. Refer to the "Output Capacitor" section of this document for recommended typical output capacitor values.

Thermal Considerations and High Output Current Applications

The AAT4702 is designed to deliver a continuous output load current of 1A by the load switch, and 100mA by the LDO regulator under normal operating conditions. The limiting characteristics for the maximum output load safe operating area are essentially package power dissipation and the internal preset thermal limit of the device. In order to obtain high operating currents, careful device layout and circuit operating conditions need to be taken into account. The following discussions will assume the device is mounted on a printed circuit board utilizing the minimum recommended footprint and the printed circuit board is 0.062-inch thick FR4 material with one ounce copper.

At any given ambient temperature (T_A), the maximum package power dissipation can be determined by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Constants for the AAT4702 are $T_{J(MAX)}$, the maximum junction temperature for the device which is 125°C, and the package thermal resistance from junction to ambient θ_{JA} = 116.3°C/W for the FTDFN22-8L. Typically, maximum conditions are calculated at the maximum operating ambient temperature where T_A = 85°C. Given T_A = 85°C, from the above formula, the maximum FTDFN22-8L package power dissipation is 344mW at T_A = 85°C. At T_A = 25°C, the maximum package power dissipation is 860mW.

The maximum continuous output current for the AAT4702 is a function of the package power dissipation and the input-to-output voltage drop across the LDO regulator and the load switch power consumption. Refer to the following equation for the total power dissipation:

$$P_{D(MAX)} = (V_{IN} - V_{OUT}) \cdot I_{OUT-LDO(MAX)} + I^2_{OUT-SW(MAX)} \cdot R_{DS(ON)} + V_{IN} \cdot I_Q$$

Where:
V_{IN} = LDO input voltage
V_{OUT} = LDO output voltage
$I_{OUT-LDO(MAX)}$ = LDO maximum output current
$I_{OUT-SW(MAX)}$ = Load switch maximum output current
$R_{DS(ON)}$ = Load switch on-state resistance, 320mΩ maximum at V_{IN}=3.6V
I_Q = Operation Quiescent Current, maximum 30µA

For example, if V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT-SW} = 200mA and T_A = 85°C, then $I_{OUT-LDO(MAX)}$ = 103.5mA. The load switch output short-circuit protection threshold could be set between 150mA to 200mA. If the LDO output load current were to exceed 103.5mA or the ambient temperature were to increase, the internal die temperature would increase. If the conditions remained constant and the short-circuit protection did not active, there would be a potential damage hazard to the LDO regulator since the thermal protection circuit would only activate after a short-circuit event or over-current occurred on the LDO regulator output. One solution is to supply the LDO input from the load switch OUT pin; when the internal die temperature reaches the load switch thermal protection point, the load switch output will be disconnected.

High Peak Output Current Applications

Some applications require the LDO regulator or the load switch to operate at continuous nominal levels with short duration, high-current peaks. The duty cycles for both output current levels must be taken into account. To do so, one would first need to calculate the power dissipation at the nominal continuous level, then factor in the addition power dissipation due to the short duration, high-current peaks.

For example, a 1.8V system using an AAT4702 operates at a continuous 80mA LDO load current level and has short 150mA current peaks, the load switch load current is 200mA. The LDO current peak occurs for 378µs out of a 4.61ms period. It will be assumed the input voltage is 5.0V.

First, the current duty cycle percentage must be calculated:

Peak current duty cycle (%): = 100 · 378µs/4.61ms = 8.2%

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The LDO regulator will be under 80mA for 91.8% of the 4.61ms period and have 150mA peaks occurring for 8.2% of the time. Next, the continuous nominal power dissipation for the 80mA load should be determined, and then multiplied by the duty cycle to calculate the actual power dissipation over time.

$$P_{D(MAX)} = (V_{IN} - V_{OUT}) \cdot I_{OUT\text{-}LDO(MAX)} + I^2_{OUT\text{-}SW(MAX)} \cdot R_{DS(ON)} + V_{IN} \cdot I_Q$$

$$P_{D(80mA)} = (5.0V - 1.8V) \cdot 80mA = 256mW$$

$$P_{D(91.8\%\text{-}80mA)} = 0.918 \cdot P_{D(80mA)} = 0.918 \cdot 256mW = 235.01mW$$

The power dissipation for an 80mA LDO load occurring for 91.8% of the duty cycle will be 235.01mW. Now the power dissipation for the 8.2% of the duty cycle at the 150mA LDO load can be calculated:

$$P_{D(150mA)} = (5.0V - 1.8V) \cdot 150mA = 480mW$$

$$P_{D(8.2\%\text{-}150mA)} = 0.082 \cdot P_{D(150mA)} = 0.082 \cdot 480mW = 39.36mW$$

The power dissipation for a 150mA LDO load occurring for 8.2% of the duty cycle will be 39.36mW. The last portion is the load switch 200mA power dissipation:

$$P_{D(200mA)} = I^2_{OUT\text{-}SW(MAX)} \cdot R_{DS(ON)} = (200mA)^2 \cdot 320m\Omega = 12.8mW$$

The power dissipation of 200mA load switch current is 12.8mW. Finally, the three power dissipation levels can be summed to determine the total true power dissipation under the varied load:

$$P_{D(total)} = P_{D(91.8\%\text{-}80mA)} + P_{D(8.2\%\text{-}150mA)} + P_{D(200mA)}$$

$$= 235.01mW + 39.36mW + 12.8mW = 287.17mW$$

The maximum power dissipation for the FTDFN22-8L operating at an ambient temperature of 85°C is 344mW. The device in this example will have a total power dissipation of 287.17mW. This is within the thermal limits for safe operation of the device.

Printed Circuit Board Layout Recommendations

In order to obtain the maximum performance from the AAT4702, very careful attention must be considered in regard to the printed circuit board layout. If grounding connections are not properly made, power supply ripple rejection and LDO regulator transient response can be compromised.

The load switch and LDO external capacitor C_{IN} and C_{OUT} should be connected as directly to the ground pin. For maximum performance with the AAT4702, the ground pin connection should then be made directly back to the ground or common of the source power supply. If a direct ground return path is not possible due to printed circuit board layout limitations, the LDO ground pin should then be connected to the common ground plane in the application layout.
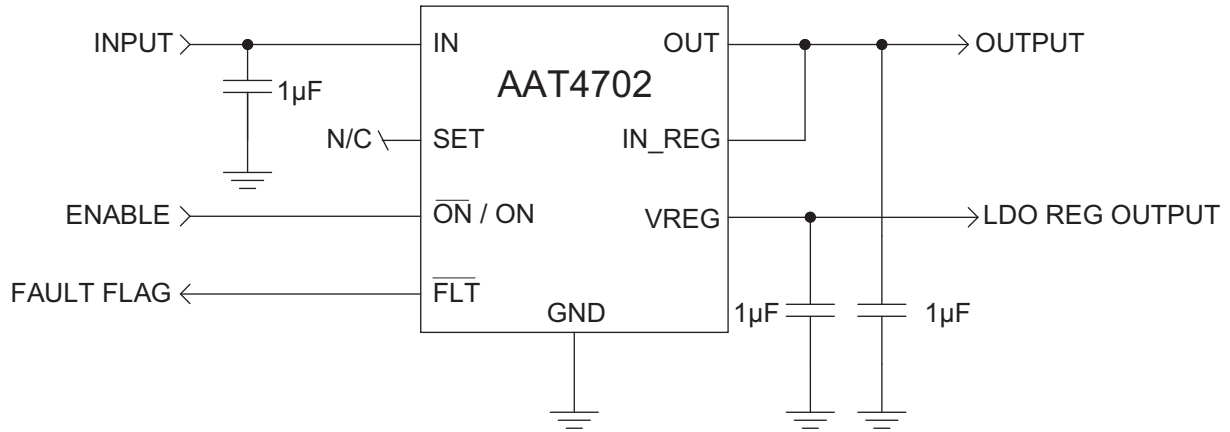
Application Circuits

**Figure 2: AAT4702 Application Circuit with the Load Switch
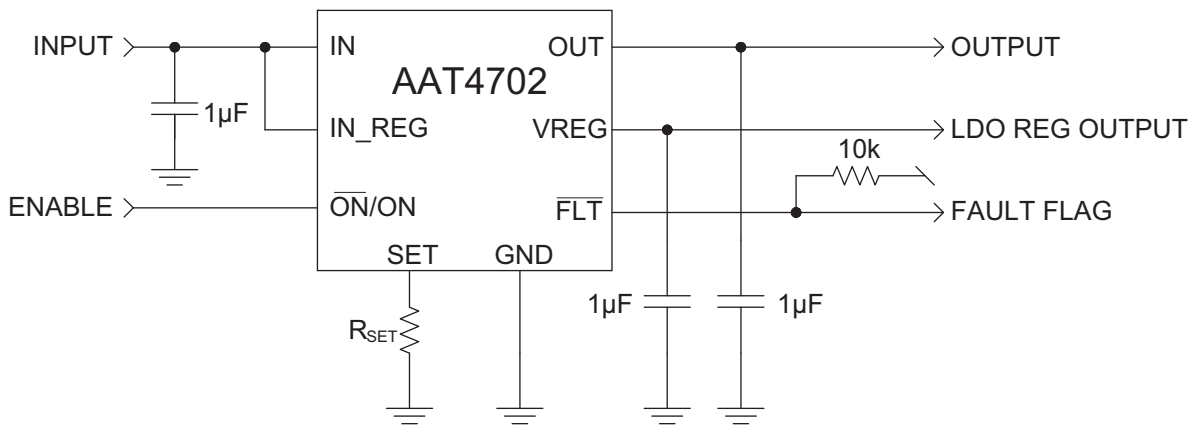and LDO Regulator Powered from a Common Input.**

Figure 3: AAT4702 Application Circuit with User Set (R_{SET}) Current Limit and Fault Flag Pull-Up Resistor.
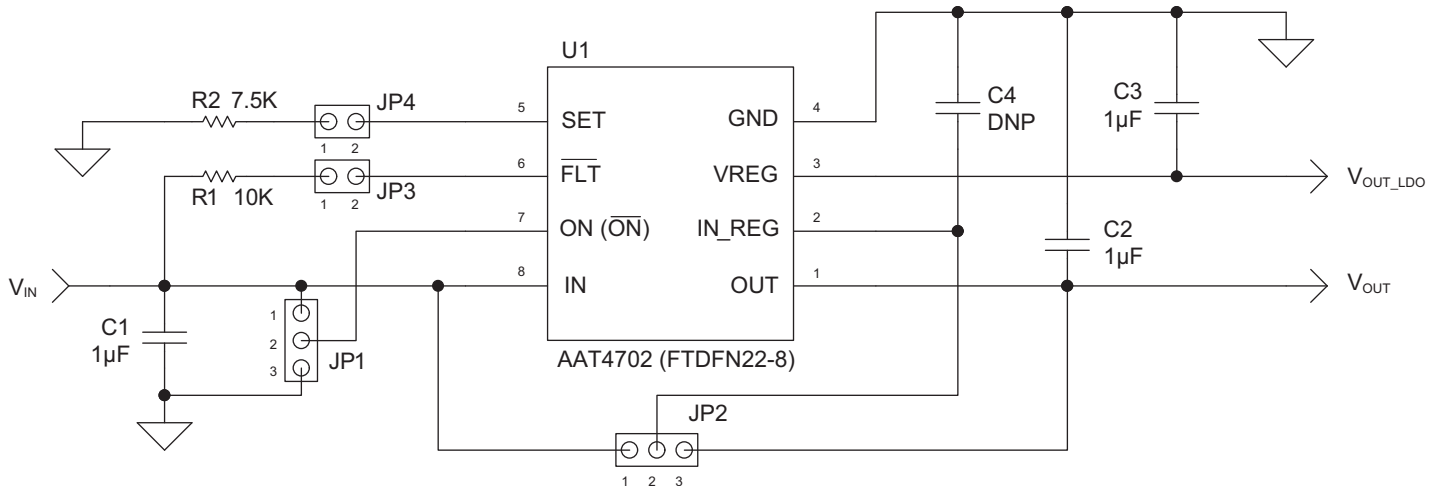
Evaluation Board Schematic

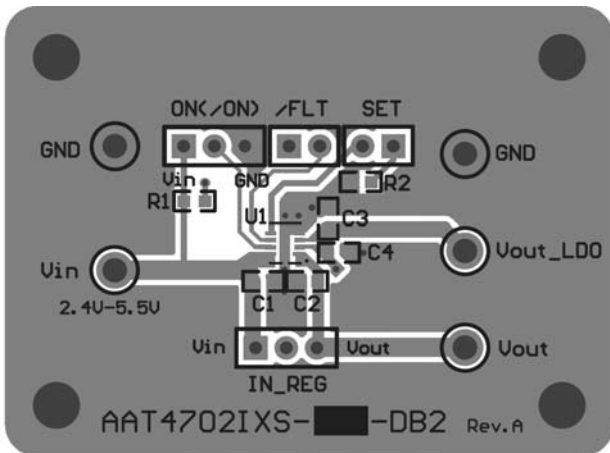**Figure 4: AAT4702 Evaluation Board Schematic.**

Evaluation Board Layout

**Figure 5: AAT4702 Evaluation Board
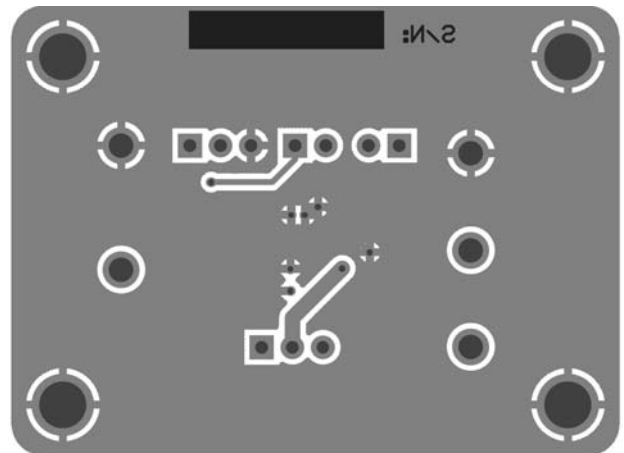Top Layer (not to scale).**

**Figure 6: AAT4702 Evaluation Board
Bottom Layer (not to scale).**

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Component	Part Number	Description	Manufacturer
U1	AAT4702	Auto Restarting Current Limiting Load Switch with LDO regulator	AnalogicTech
C1, C2, C3	GRM188R61A105KA61	SMD, Cap ceramic 1µF 0603 X5R 10V 10%	Murata
C4	DNP	DNP, Do Not Place	
R1	Chip Resistor	SMD, 10kΩ, 5%, 150mW, 0603	Vishay
R2	Chip Resistor	SMD, 7.5kΩ, 5%, 150mW, 0603	Vishay
JP1, JP2	Connector	Header 3 pins, pitch 75mil	Any
JP3, JP4	Connector	Header 2 pins, pitch 75mil	Any
	Shunt	Shunt for connector	Any
	PCB	AAT4702 Evaluation board PCB	AnalogicTech

Table 2: AAT4702 Evaluation Board Bill of Materials (BOM).

ANALOGIC TECH

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Ordering Information

Package	Voltage Regulator Output	Enable	Marking[1]	Part Number (Tape and Reel)[2]
FTDFN22-8L	1.8V	Active Low	7CXYY	**AAT4702IXS-1-T1**
FTDFN22-8L	1.8V	Active High		AAT4702IXS-2-T1

Pb-free

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.

Package Information

FTDFN22-8L

Index Area

2.000 ± 0.050

2.000 ± 0.050

Top View

0.400 ± 0.050

Detail "A"

Bottom View

0.750 ± 0.050

0.230 ± 0.050

0.000 +0.100 −0.000

Side View

0.500 ± 0.050

0.450 ± 0.050

0.250 ± 0.050

Pin 1 Identification

Detail "A"
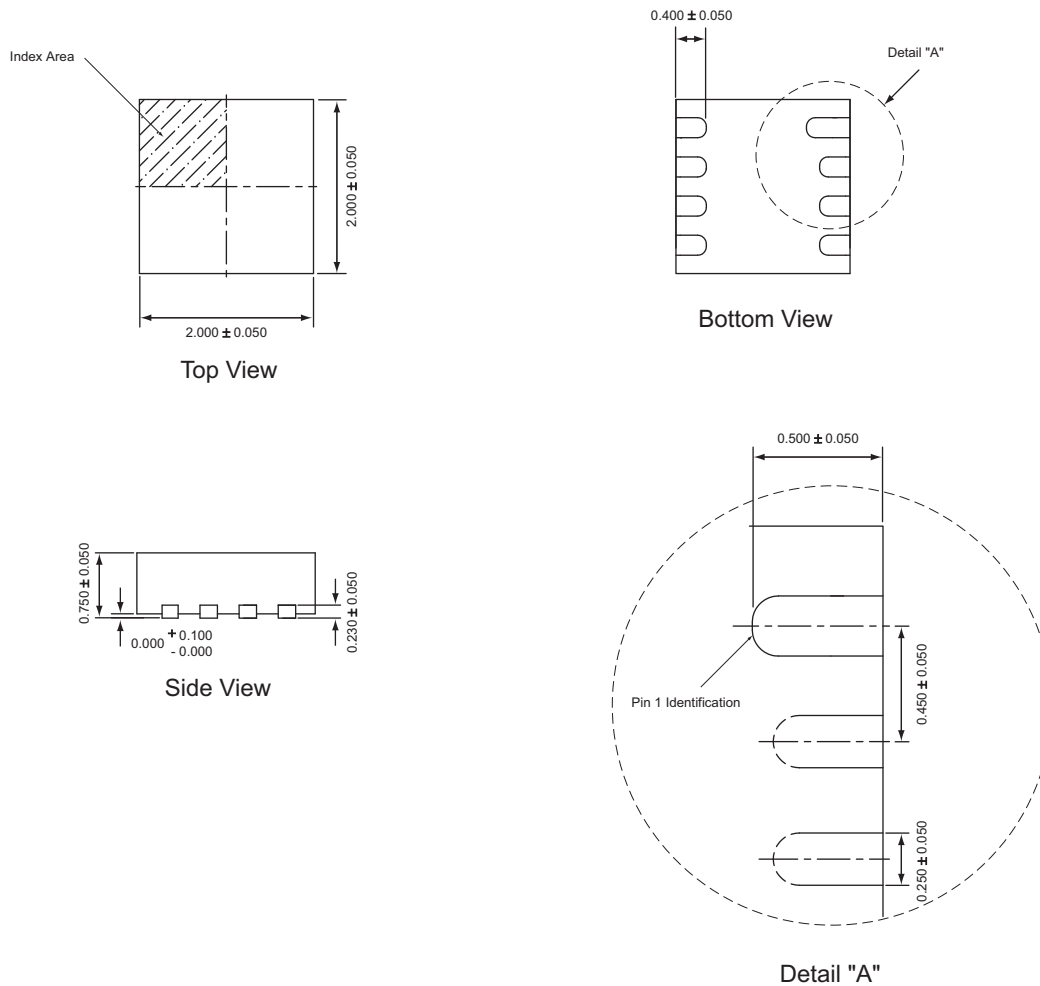
All dimensions in millimeters.

1. XYY= assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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