



High-performance,
full NFC Forum-
compliant frontend
PN5180

The best full NFC frontend on the market

Offering high output power, Dynamic Power Control, multiple power-saving features, this advanced, multi-protocol NFC frontend delivers efficient, robust, and reliable operation, even in harsh conditions.

KEY FEATURES

- ▶ Full compliance with all standards relevant to NFC, contactless operation and EmVCo
- ▶ Automatic EMD handling for faster design of payment terminals
- ▶ Onboard Dynamic Power Control (DPC) for optimized RF performance, even under detuned conditions
- ▶ Low-power card detection minimizes current consumption during polling
- ▶ Active load modulation supports smaller antenna with Card Emulation Mode
- ▶ Small, industry-standard packages
- ▶ NFC Cockpit GUI: software-independent register settings
- ▶ Development kit with 32-bit NXP LPC1769 MCU and antenna
- ▶ NFC Reader Library with source code ready for EMVCo L1 and NFC Forum compliance

KEY BENEFITS

- ▶ Best RF performance
- ▶ PCI-compliant payment terminals
- ▶ Full interoperability with the latest NFC devices
- ▶ Standard and proprietary implementations
- ▶ Long battery life
- ▶ Fast time-to-market

APPLICATIONS

- ▶ Payment terminals
- ▶ Physical-access readers
- ▶ eGov readers
- ▶ Industrial readers
- ▶ High-performance readers

The NXP PN5180 NFC frontend, equipped with unique features that improve performance, save energy, and maximize efficiency, enables best-in-class readers that conform to the requirements for EMVCo and NFC Forum specifications, for the broadest possible interoperability.

ROBUST PERFORMANCE

A new feature, called Dynamic Power Control (DPC), controls antenna current, RF power, and the related waveforms to deliver optimized RF performance, even under detuned conditions. It maximizes transmitter current during detuned conditions and thereby compensates for any negative effects generated by nearby metal, cards, or phones.



It also controls the field strength along the operating range, so it stays within ISO/EMVCo requirements. It ensures robust communication with smartcards and smartphones, without using any additional external components.

FLEXIBLE OPERATION

The PN5180 uses the SPI interface to connect with a host controller, and accepts flexible RF configurations from the host to support standard and proprietary card formats. Optimized 32-bit commands make it easy to use the PN5180 with the latest microcontrollers. In TFBGA package, the PN5180 can also drive LEDs.

LOW POWER

Multiple power-saving features help extend battery life, making the PN5180 an excellent choice for access and other applications that rely on battery power. The frontend supports low-power card detection.

EASY CERTIFICATION

Several features, including the DPC, strong RF power generation, RF wave shaping, and hardware-based EMD error handling, ease EMVCo and NFC-reader certification, while the TFBGA package simplifies PCI certification. What's more, having the EMVCo L1 (analog and digital) library in source code makes it easier to add ICs in designs that target payment applications.

FAST DEPLOYMENT

The PN5180 is supported by advanced tools that make it easier than ever to develop a design. The NFC Cockpit, an intuitive graphical user interface (GUI), streamlines development by separating the tasks associated with HW and SW. It supports SW-independent tuning of the antenna's register settings, so HW designers can optimize antenna parameters while SW designers work on other aspects.

The NFC Cockpit works seamlessly with the PN5180 development kit, which includes a CE/FCC-compliant development board with a 32-bit NXP LPC1769 microcontroller and an antenna. The NFC Reader Library is an ideal SW companion for application development, since it offers easy porting to standard microcontroller cores and is fully compliant with EMVCo L1 and digital certifications from the NFC Forum. Full documentation and pre-certified SW stacks are available on www.nxp.com.

TECHNICAL HIGHLIGHTS

- ▶ Host interface: 1.8 or 3.3 V, 7 Mbit/s SPI, IRQ & busy signals (improved host communication, task scheduling)
- ▶ RF driver supply voltage: 2.7 to 5.5 V
- ▶ Max. transmitter current: 250 mA
- ▶ Low-power card detection, supported by LDO wakeup signal
- ▶ 4 Multi-purpose outputs on TFGA, 1 multi-purpose output on HVQFN
- ▶ Packages: HVQFN40 for easy PCB design, TFBGA64 with extra GPIO and added security for PCI compliance
- ▶ HW support for EMVCo EMD handling
- ▶ Operating temperature: -30 to +85 °C
- ▶ Fast SPI host interface with optimized commands for use with 32-bit host controllers

SUPPORTED RF PROTOCOLS

Read/Write Mode

- ▶ ISO/IEC 14443 Type A&B R/W support up to 848 kbit/s
- ▶ FeliCa R/W support up to 424 kbit/s
- ▶ R/W support for MIFARE 1K, 4K
- ▶ NFC Forum tag type 1, 2, 3, 4, 5 reader
- ▶ NFC Forum compliance for R/W – analog and digital
- ▶ ISO/IEC 15693 reader (ICODE)
- ▶ ISO/IEC 18000 EPC-HF reader (ICODE ILT)
- ▶ EMVCo 2.3.1 and 2.5 ready (L1) with integrated EMD handling
- ▶ R/W support MIFARE Ultralight, MIFARE Classic 1K/4K, MIFARE DESFire EV1/EV2, MIFARE Plus cards
- ▶ MIFARE CRYPTO in hardware for R/W of MIFARE cards
- ▶ Includes intellectual-property licensing rights for NXP ISO/IEC 14443-A, Innovatron ISO/IEC 14443-B, and NXP MIFARE CRYPTO1

Peer-to-Peer Mode

- ▶ Passive and active communication (Initiator/Target)
- ▶ P2P supported for types: A (106 kbit/s), F (212,424 kbit/s)

Card Emulation Mode

- ▶ ISO/IEC 14443 Type A (up to 848 kbit/s) with Active and Passive Load Modulation
- ▶ ISO/IEC 14443 Type A Host Card Emulation with Active Load Modulation for longer communication distances